

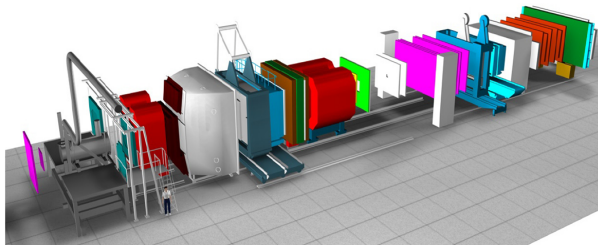
Development of new data acquisition system for COMPASS experiment

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&
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COMPASS experiment

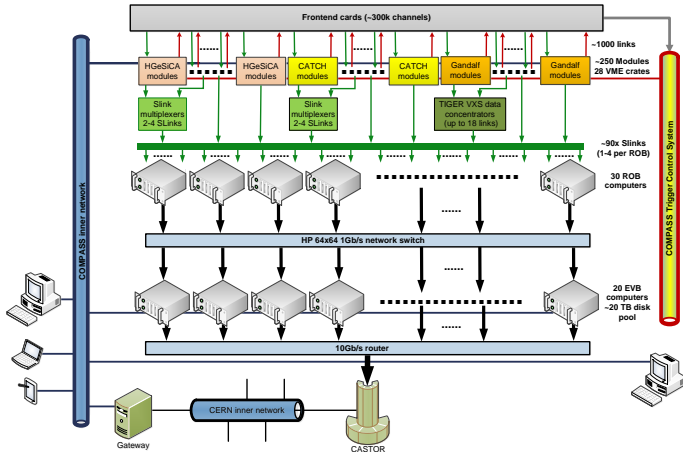
- ▶ fixed target experiment at SPS accelerator at CERN
- ▶ study of hadron structure and hadron spectroscopy with high intensity muon and hadron beams
- ▶ data-taking started in 2002
- ▶ trigger rate up to 30 kHz, average event size up to 50 kB
- ▶ in spill data rate 1.5 GB/s and sustained data rate 500 MB/s



Hardware/Software structure of the old DAQ

Network based E.B.

- ▶ ~ 300k channels
- ▶ ~ 1000 links to ~ 250 modules
- ▶ ~ 90 S-links to 30 ROB's
- ▶ **50 online computers**
= 30 ROB+ 20 EB
- ▶ DAQ built in 2000
- ▶ sustained rate only of 500 MB/s
- ▶ Software event building

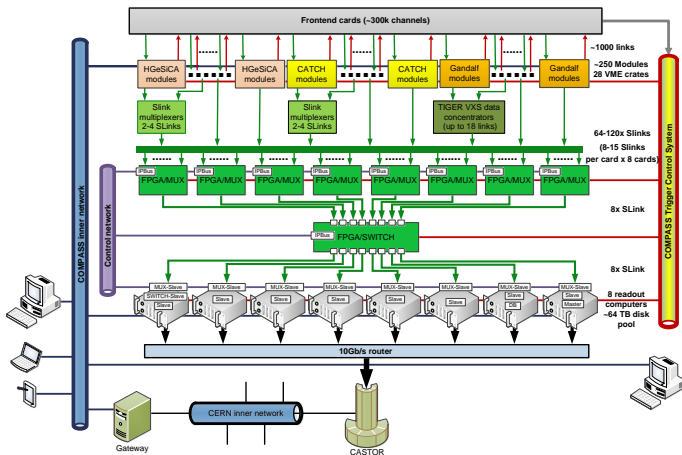


Hardware/Software design of the new DAQ

Hardware/Software structure of the new DAQ

Hardware based E.B.

- ▶ 8 new DAQ modules as multiplexer
- ▶ 1 new DAQ modules as switch
- ▶ 8 readout computers
- ▶ 64 TB disk pool using RAID 10
- ▶ less components
- ▶ full events received by servers
- ▶ consistency check at many layer



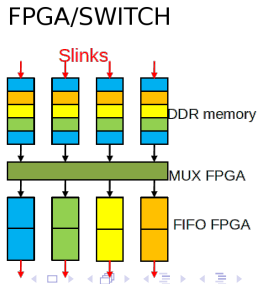
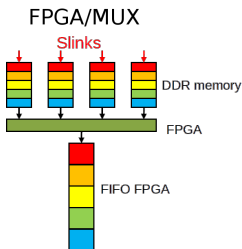
Hardware based event building

HW event building in history

- ▶ CDF - Fermilab [11]
- ▶ NA48 - CERN [12],[13]

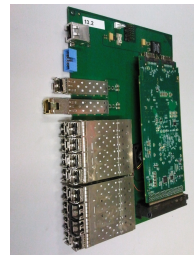
HW event building now with new FPGAs

- ▶ faster - high speed serial links
- ▶ more flexible
- ▶ cheaper and more reliable

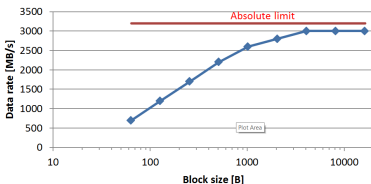


DAQ unit

- ▶ TCS (Trigger Control System) receiver - synchronization information
- ▶ 1 Gb Ethernet - control system link (IPbus)
- ▶ 16xSerial links - data links
 - ▶ Slink (2 Gbps)
 - ▶ Aurora (6.25 Gbps)
- ▶ 6 U VME form factor module → New DAQ fits in one 6 U VME crate



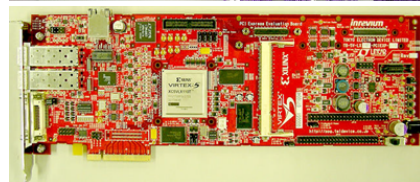
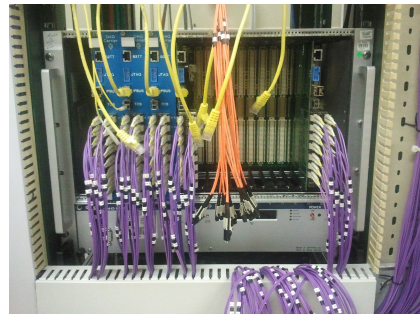
Memory Throughput



- ▶ AMC module, ATCA standard
- ▶ VIRTEX6 XC6VLX130T FPGA - middle sized FPGA and relatively cheap (500 Euro/chip)
- ▶ 4 GB DDR3
- ▶ Module programmed as MX 15:1 or SW 8x8 (can be recompiled to any NxM configuration)

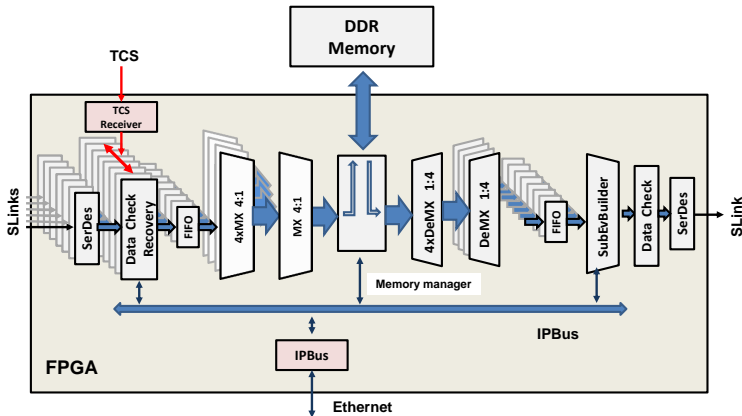
New hardware parts

- ▶ 10 AMC cards + adapter cards
- ▶ 12 PCIe cards + 14 TCS receivers
- ▶ 6 TCS encoders/controllers
 - ▶ Substitute obsolete and not available TTC encoders
 - ▶ Wave length adapter from 1300 nm to 830 nm
 - ▶ IPbus for control and monitoring, VME is only for power and cooling



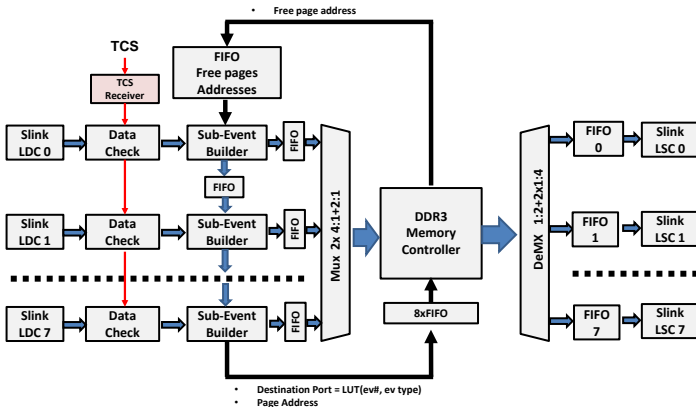
MX firmware

- ▶ buffering - enough memory to store one spill
- ▶ sub-event building



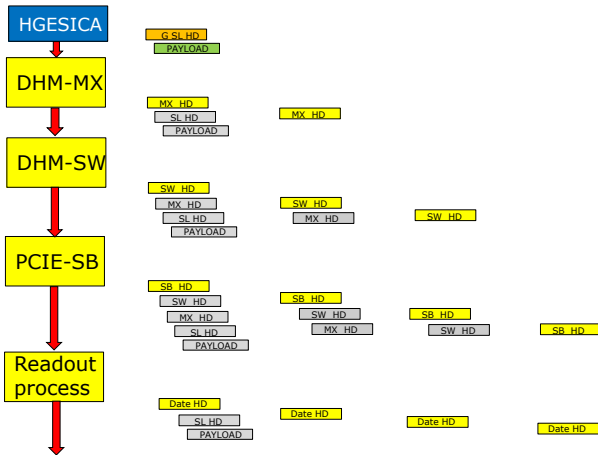
SW firmware

- ▶ DDR memory divided to 8k pages of 500kB each (bigger than maximum event size)
- ▶ Memory address is attached to data block header



Example of Data Flow and Data encapsulation

- ▶ Each step controls data and adds new header
- ▶ Data with errors thrown away and header generated

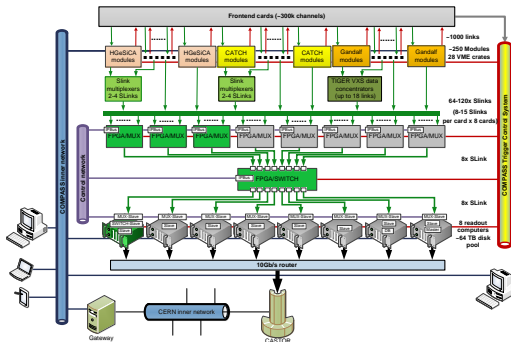


Used software technologies

- ▶ C++, Python
- ▶ Qt framework
- ▶ DIM (Distributed Information Management System)
- ▶ IPbus suite for communication with FPGAs
- ▶ MySQL
- ▶ PHP, javascript
- ▶ Zabbix package used for computer resources monitoring

Present status

- ▶ preparation for commissioning
- ▶ fraction of detectors connected
- ▶ testing of links, data transmission and data handling



Present status - sub-DAQ tests

Run control GUI

The screenshot displays the Run Control - CMAD interface, which is divided into several functional areas:

- Info:** A field for 'Run Number' and a 'Spill count' field.
- Run Control:** A vertical stack of buttons including 'Turned off', 'Slaves started', 'Configured', 'Run', and 'Stop Run'.
- TCSinfo:** A table showing channel information with columns for channel, incount, outcount, divide, and new setting.

channel	incount	outcount	divide	new setting
0	77993	0	0	0
1	0	0	0	0
2	0	0	0	0
3	0	0	0	0
4	0	0	0	0
5	0	0	0	0
6	0	0	0	0
7	0	0	0	0
8	0	0	0	0
9	0	0	0	0
10	77993	7800	10	10
11	0	0	0	0
- Configuration:** A panel with dropdown menus for 'Run type' (set to 8887e5tstp), 'Run Number', 'Number of spills', 'Trigger settings', and 'Firmware'. It includes buttons for 'Configure run', 'Configure links', and 'Load Firmware'.
- FGA status:** A detailed status window for 'SPILL92' showing FPGA firmware version, source ID, event number (121), current spill number (206), and various hardware and software parameters like 'header enable', 'error mask', and 'max event size allowed'.
- Mean event size:** A bar chart showing event sizes over time, with the x-axis labeled from 887,700 to 887,850 and the y-axis from 0 to 6,000.
- Computer Status:** A section at the bottom left of the main panel.
- Status Window:** A table at the bottom right showing the status of various modules:

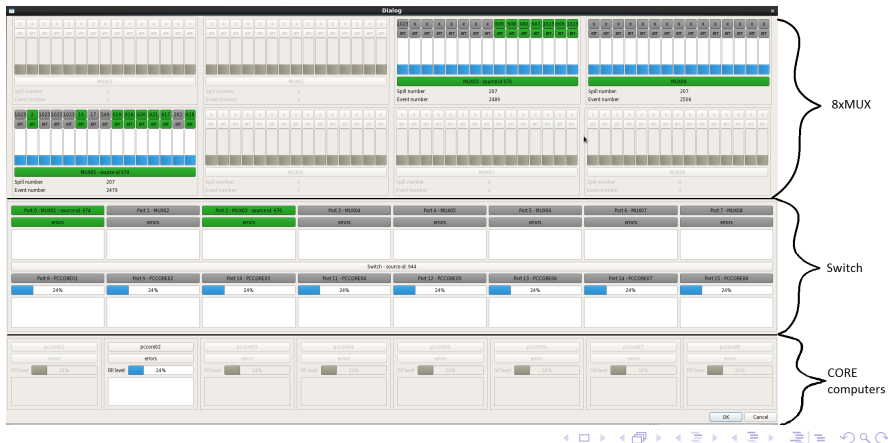
names	status
▶ master	Byzno
▶ SC_BELL	Byzno
▶ SMC01_BELL	Byzno
▶ SMC02_BELL	Byzno
▶ SMC03_BELL	Byzno
▶ SMC04_BELL	Byzno
▶ SR_BELL	Byzno



Present status - sub-DAQ tests

DAQ system main window

- ▶ component status overview and configuration



Present status - sub-DAQ tests

MessageBrowser

The screenshot displays the MessageBrowser application interface. At the top, there are several filter buttons: **Column filter** (with checkboxes for id, tm, dt, sender, severity, runNum, spillNum, eventNum, text) and **Filters** (with buttons for Check All, Uncheck All, Hide filters, and APPLY FILTER).

The main area contains a table of log messages with the following columns: id, tm, dt, sender, severity, runNum, spillNum, eventNum, and text. The messages are color-coded by severity: red for FATAL and ERROR, yellow for WARNING, and green for INFO.

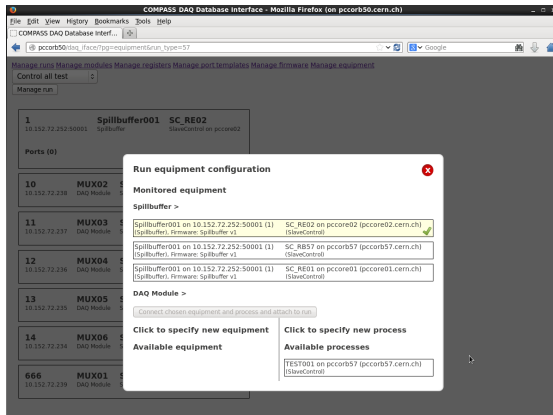
id	tm	dt	sender	severity	runNum	spillNum	eventNum	text
1	12:30 AM	11/11/11	8	FATAL ERROR	1000	5	5	Random text 2 6
2	1:00 AM	11/11/11	9	ERROR	1004	7	9	Random text 2 9
3	1:01 AM	11/11/11	9	ERROR	1004	13	3	Random text 2 9
4	1:01 AM	11/11/11	9	INFO	1004	13	12	Random text 0 9
5	1:02 AM	11/11/11	8	WARNING	1004	15	17	Random text 1 6
6	1:02 AM	11/11/11	7	INFO	1004	14	6	Random text 0 7
7	1:03 AM	11/11/11	8	WARNING	1004	22	9	Random text 1 8
8	2:02 AM	11/11/11	6	WARNING	1005	5	5	Random text 1 6
9	2:03 AM	11/11/11	2	FATAL ERROR	1005	14	4	Random text 2 2
10	2:04 AM	11/11/11	7	INFO	1005	14	7	Random text 0 7
11	2:04 AM	11/11/11	1	INFO	1005	14	14	Random text 0 1
12	2:04 AM	11/11/11	10	FATAL ERROR	1005	18	18	Random text 0 10
13	2:04 AM	11/11/11	8	WARNING	1005	14	22	Random text 1 6
14	2:05 AM	11/11/11	10	FATAL ERROR	1005	24	7	Random text 2 10
15	2:06 AM	11/11/11	8	FATAL ERROR	1005	21	2	Random text 2 8
16	2:06 AM	11/11/11	3	WARNING	1005	31	7	Random text 1 3
17	2:06 AM	11/11/11	7	WARNING	1005	31	10	Random text 1 7
18	3:06 AM	11/11/11	6	ERROR	1014	7	1	Random text 2 6
19	3:07 AM	11/11/11	10	WARNING	1014	12	9	Random text 1 10
20	3:08 AM	11/11/11	1	INFO	1014	19	10	Random text 0 1
21	3:09 AM	11/11/11	9	WARNING	1014	25	3	Random text 1 9
22	3:08 AM	11/11/11	9	ERROR	1014	25	10	Random text 2 9
23	3:09 AM	11/11/11	7	ERROR	1014	25	14	Random text 2 7
24	3:10 AM	11/11/11	4	INFO	1014	31	2	Random text 0 4
25	3:11 AM	11/11/11	9	ERROR	1014	37	4	Random text 2 9
26	3:12 AM	11/11/11	8	FATAL ERROR	1014	30	2	Random text 1 8
27	4:12 AM	11/11/11	7	ERROR	1016	12	10	Random text 2 7
28	4:12 AM	11/11/11	9	ERROR	1016	12	13	Random text 2 9
29	4:13 AM	11/11/11	10	WARNING	1016	17	9	Random text 1 10
30	4:14 AM	11/11/11	4	ERROR	1016	19	3	Random text 2 4
31	4:14 AM	11/11/11	2	WARNING	1016	38	4	Random text 1 2
32	4:15 AM	11/11/11	2	WARNING	1016	21	5	Random text 1 2
33	4:15 AM	11/11/11	3	FATAL ERROR	1016	21	20	Random text 2 3
34	4:15 AM	11/11/11	9	ERROR	1016	21	19	Random text 2 9
35	5:15 AM	11/11/11	5	INFO	1023	10	6	Random text 0 5
36	6:15 AM	11/11/11	9	INFO	1027	8	6	Random text 0 9
37	6:16 AM	11/11/11	9	ERROR	1027	15	4	Random text 2 9
38	6:16 AM	11/11/11	4	FATAL ERROR	1027	4	11	Random text 2 4
39	7:16 AM	11/11/11	3	INFO	1036	7	7	Random text 0 3
40	7:16 AM	11/11/11	3	ERROR	1036	7	11	Random text 2 3
41	8:15 AM	11/11/11	1	ERROR	1041	10	7	Random text 2 1
42	8:17 AM	11/11/11	5	FATAL ERROR	1043	17	8	Random text 2 5
43	8:18 AM	11/11/11	1	INFO	1041	19	5	Random text 0 1
44	8:18 AM	11/11/11	9	INFO	1041	19	14	Random text 0 9
45	9:18 AM	11/11/11	9	WARNING	1043	3	6	Random text 1 9

On the right side, there is a **Message filter** panel with sections for **Severity** (Info, Warning, Error), **Sender** (test001, test002, test003), **Run number** (Exact, Current, 1000, Range, From, To, 1500), **Spill number** (Exact, 55, Range, From, To, 25, % 55), **Event number** (Exact, 5, Range, From, To, 3, % 6), **Data - time** (From: 11/11/2011 00:00, To: 11/11/2011 00:00), and **Error text**.



Configuration interface

- ▶ new configuration interface -> system fully configurable through web interface



Present status - sub-DAQ tests

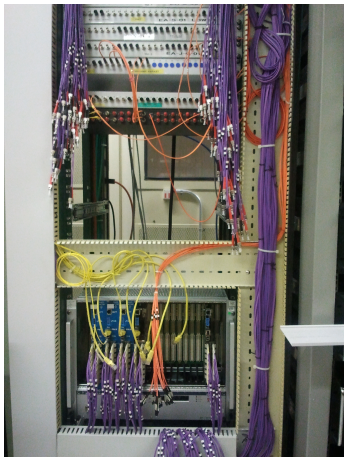
- ▶ XML description of DAQ structure and FPGA registers automatically generated from DB
- ▶ used for IPbus communication, event consistency checks, parsing of information from registers

```
1 <?xml version="1.0" encoding="UTF-8"?>
2 <structure>
3   <hardware>
4     <type>Spillbuffer</type>
5     <action>remove</action>
6     <source>1</source>
7   </hardware>
8     <type>MUX</type>
9     <action>remove</action>
10    <source>560</source>
11  </hardware>
12 </hardware>
13 <hardware>
14   <type>Spillbuffer</type>
15   <action>remove</action>
16   <source>2</source>
17 </hardware>
18 <hardware>
19   <type>Spillbuffer</type>
20   <action>remove</action>
21   <source>3</source>
22 </hardware>
23 </structure>
```

```
1 <?xml version="1.0" encoding="UTF-8"?>
2 <card id="REGISTERS">
3   <block id="GB">
4     <register id="IDReg" address="0x0" permission="r">
5       <register_part id="FPGAVER" mask="0xffff" description="FPGA firmware version"/>
6       <register_part id="DeID" mask="0xffff0000" description="Device ID"/>
7     </register>
8     <register id="SourceID" address="0x1" permission="rw">
9       <register_part id="SID" mask="0x3fff" description="Source ID"/>
10    </register>
11    <register id="CurEvNum" address="0x2" permission="r">
12      <register_part id="EN" mask="0xffff" description="Event number"/>
13      <register_part id="CSP" mask="0x7ff00000" description="Current spill number"/>
14      <register_part id="bx0" mask="0x80000000" description="bx0"/>
15    </register>
16    <register id="CurEvTI" address="0x3" permission="r">
17      <register_part id="ETDCE" mask="0x1f" description="Event type of current event"/>
18      <register_part id="TDCE" mask="0xfffffe0" description="Time of current event"/>
19    </register>
20    <register id="LSpEvNum" address="0x4" permission="r">
21      <register_part id="LDN" mask="0xffff" description="LEvent number"/>
22      <register_part id="LSN" mask="0x7ff00000" description="Last spill number"/>
23      <register_part id="Lbx0" mask="0x80000000" description="Lbx0"/>
24    </register>
25    <register id="LSpEvTI" address="0x5" permission="r">
26      <register_part id="LETOCE" mask="0x1f" description="LEvent type of current event"/>
27      <register_part id="LTDCE" mask="0xfffffe0" description="LTime of current event"/>
28    </register>
29    <register id="TCSSStat" address="0x6" permission="rw">
30      <register_part id="IPBUSI" mask="0x1" description="IPBUS TCS reciever enable"/>
31      <register_part id="SIAZE" mask="0x6" description="Slink 1 and 2 enable"/>
32      <register_part id="bx000R" mask="0x38" description="bx000 reserved"/>
33      <register_part id="TCSRE" mask="0x40" description="TCS receiver enabled"/>
34      <register_part id="ECCH" mask="0x80" description="ECC mode"/>
35      <register_part id="TCSRID" mask="0xff00" description="TCS receiver ID"/>
36      <register_part id="TCSSE" mask="0xffff0000" description="TCS errors"/>
37      <register_part id="TCSDM" mask="0xff000000" description="TCS DAQ mask"/>
38    </register>
39    <register id="FIR01FL" address="0x7" permission="r">
40      <register_part id="FM1" mask="0xffffffff" description="Filled memory 1"/>
41    </register>
42    <register id="FIR02FL" address="0x8" permission="r">
43      <register_part id="FM2" mask="0xffffffff" description="Filled memory 2"/>
44    </register>
45  </block></card>
```

Present status - sub-DAQ tests

Setting up new DAQ



Advantages of new DAQ

- ▶ More compact
- ▶ Flexible configuration
- ▶ Data verification on every step
- ▶ Less power demanding
- ▶ Easier to control (more time for reaction)

Conclusion

- ▶ communication system tested
- ▶ sub-DAQ tested without detectors
- ▶ expected peak performance 1.5 GB/s and sustainable 1.2 GB/s but real performance still to be measured
- ▶ on the route to commissioning by end of July

References



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References



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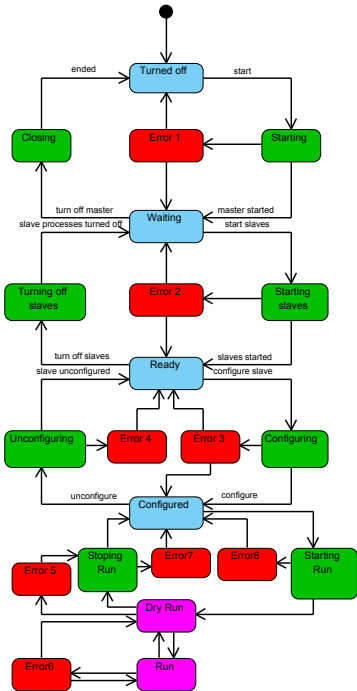
T. M. Shaw, et al.: *Architecture and development of the CDF hardware event builder* IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 36, NO. 1, AUGUST 1989



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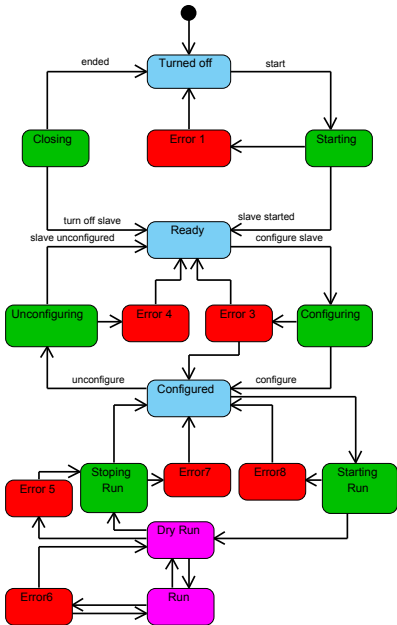


M. Wittgen, et al.: *The NA48' Event-Building PC Farm* IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 47, NO. 2, APRIL 2000



- stable state, states that do nothing just wait for next command
- transference states(not stable), do not accept comm:
- error state
- working states, stable until command come or end condition is reached

number	name
0	Turned off
1	Waiting
2	Ready
3	Configured
11	Dry Run
12	Run
21	Starting
22	Closing
23	Starting slaves
24	Turning off slaves
25	Configuring
26	Unconfiguring
27	Starting run
28	Stopping Run
41-48	Error 1-8

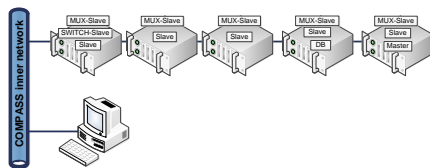


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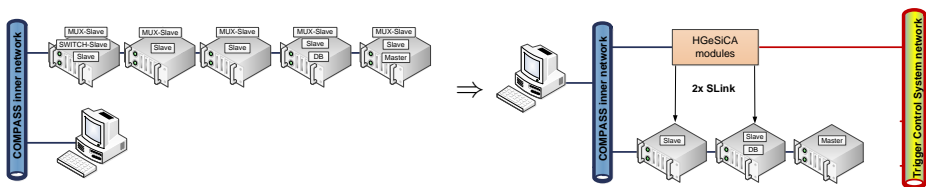
Route to final setup

- ▶ System tests phase 1 - communication tests [2]
- ▶ System tests phase 2 - readout tests [2]
- ▶ System tests phase 3 - multiplexer tests
- ▶ System tests phase 4 - sub-DAQ tests



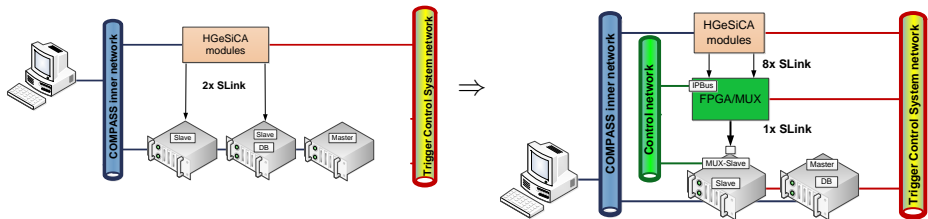
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