Development of new data acquisition system for COMPASS experiment

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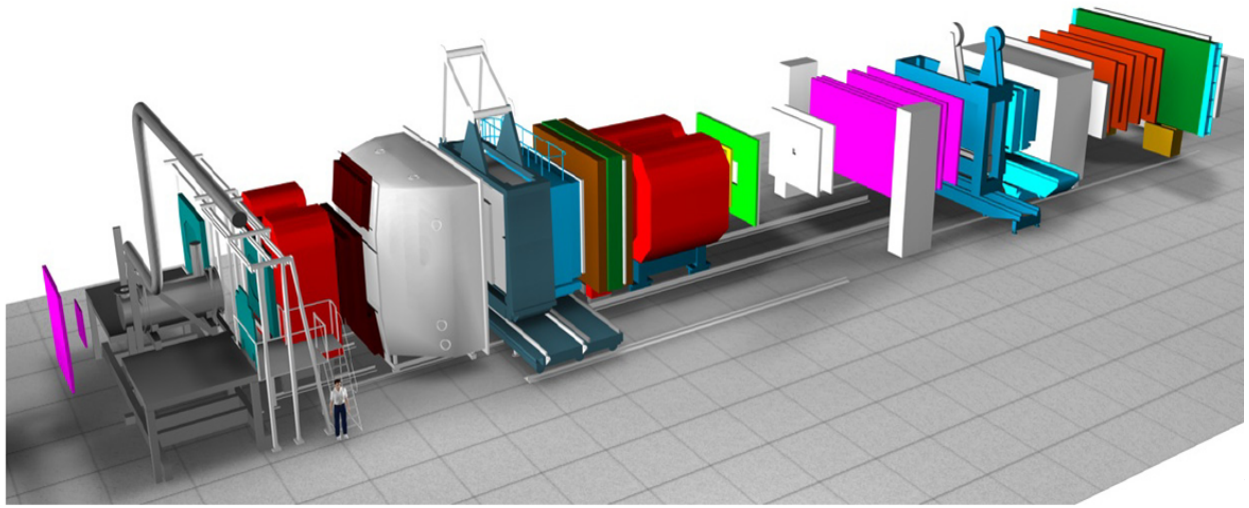
COMPASS experiment

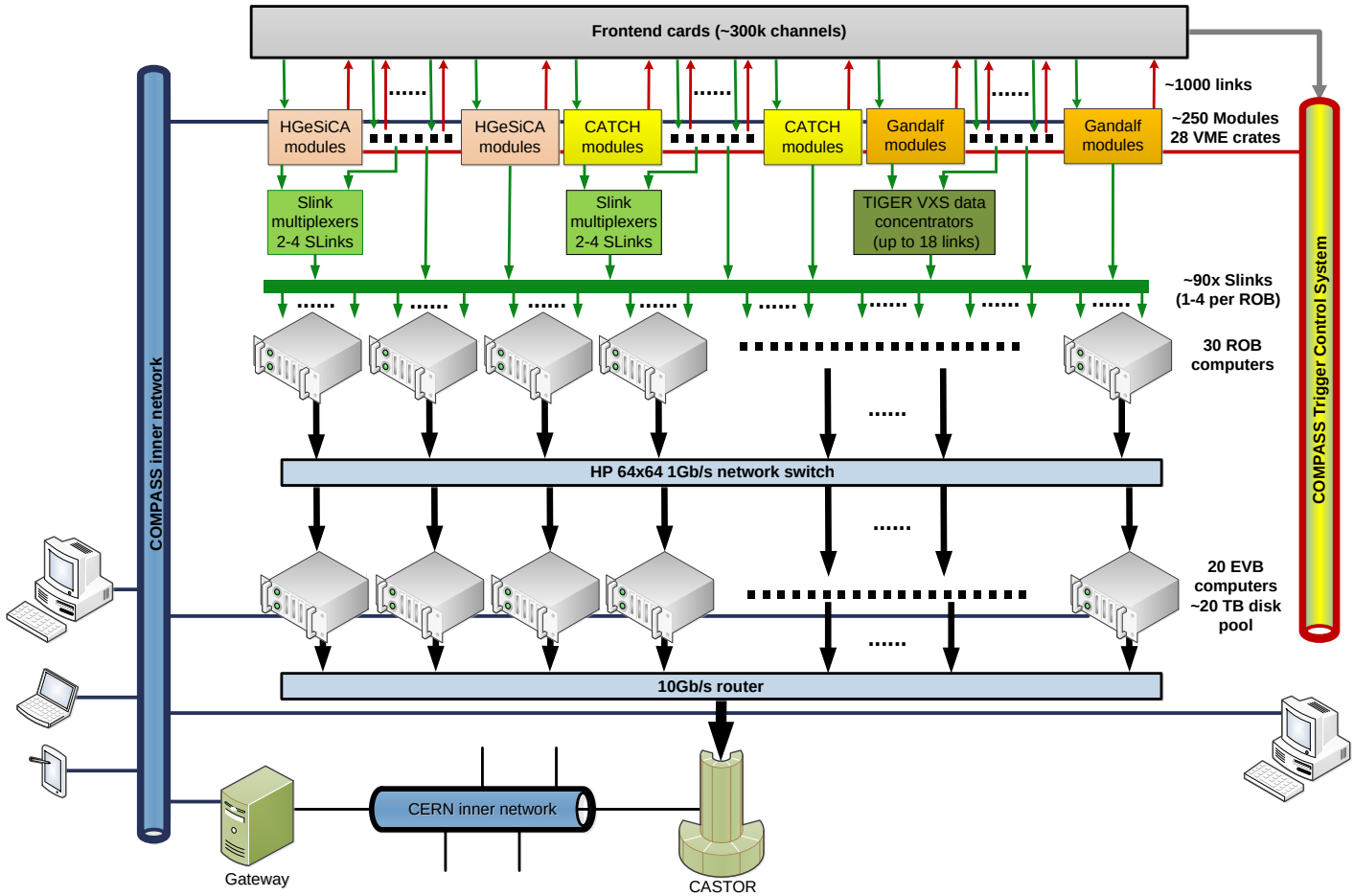
- fixed target experiment at SPS accelerator at CERN
- study of hadron structure and hadron spectroscopy with high intensity muon and hadron beams
- data-taking started in 2002
- trigger rate up to 30 kHz, average event size up to 50 kB
- in spill data rate 1.5 GB/s and sustained data rate 500 MB/s



Hardware/Software structure of the old DAQ

Network based E.B.

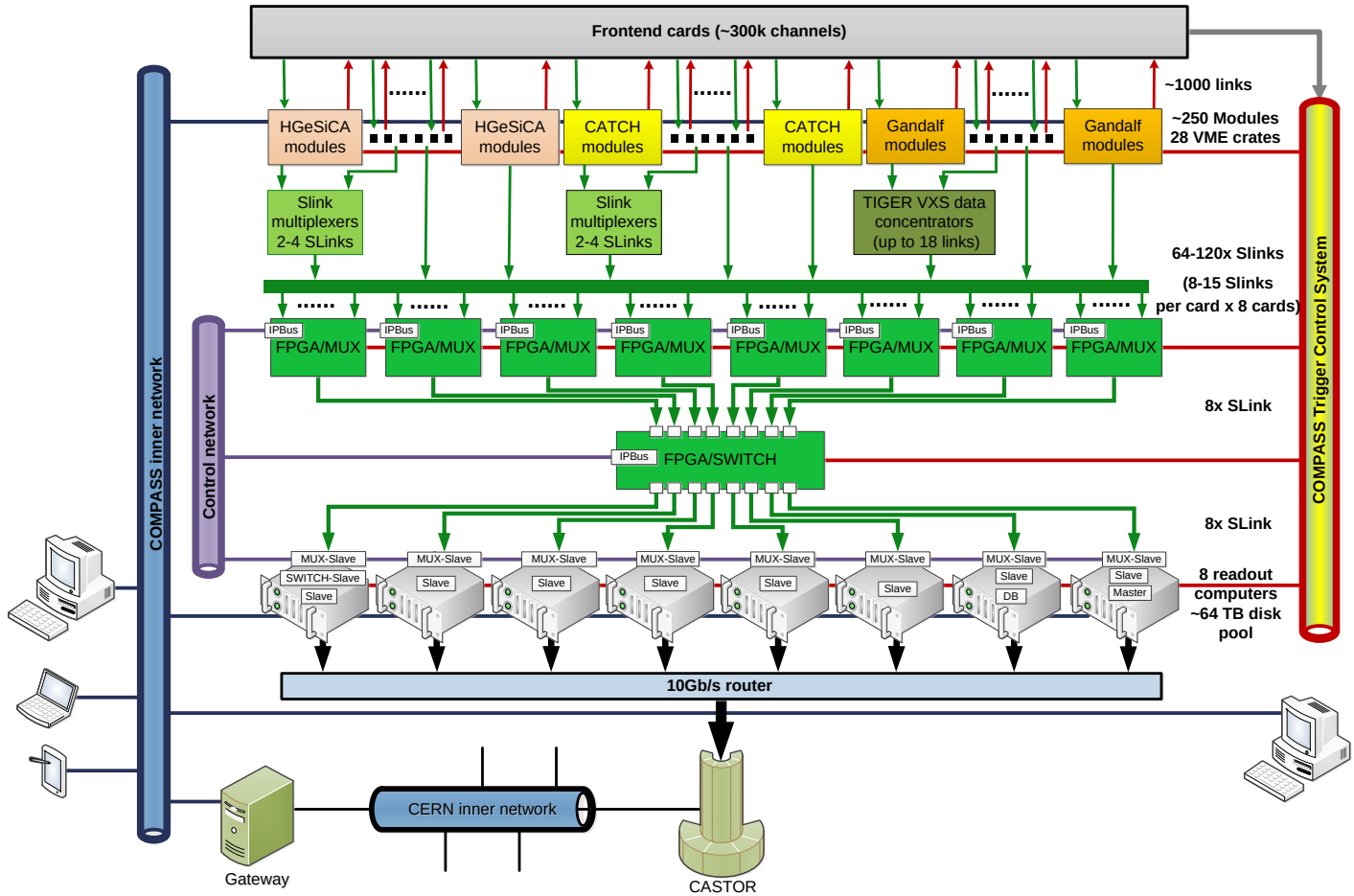
- ∽ 300k channels
- ∽ 1000 links to ∽ 250 modules
- ∽ 90 S-links to 30 ROBs
- **50 online computers** = 30 ROB+ 20 EB
- DAQ built in 2000
- sustained rate only of 500 MB/s
- Software event building



Hardware/Software structure of the new DAQ

Hardware based E.B.

- 8 new DAQ modules as multiplexer
- 1 new DAQ modules as switch
- 8 readout computers
- 64 TB disk pool using RAID 10
- less components
- full events received by servers
- consistency check at many layer



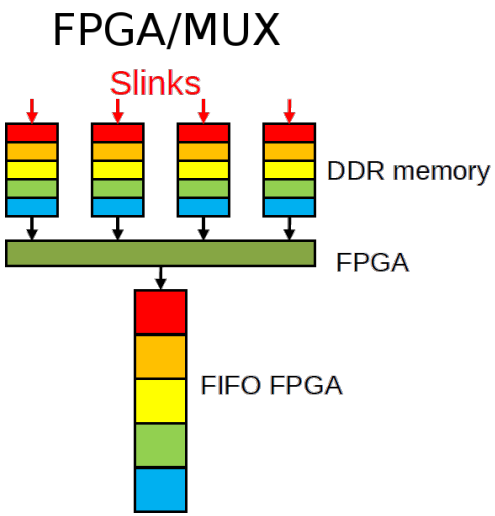
Hardware based event building

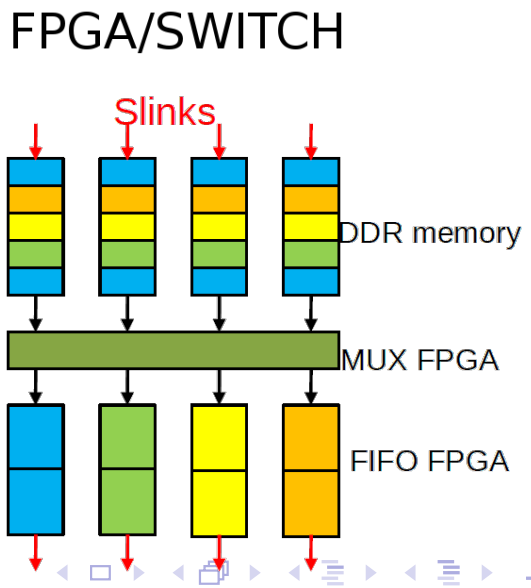
HW event building in history

- CDF - Fermilab [11]
- NA48 - CERN [12],[13]

HW event building now with new FPGAs

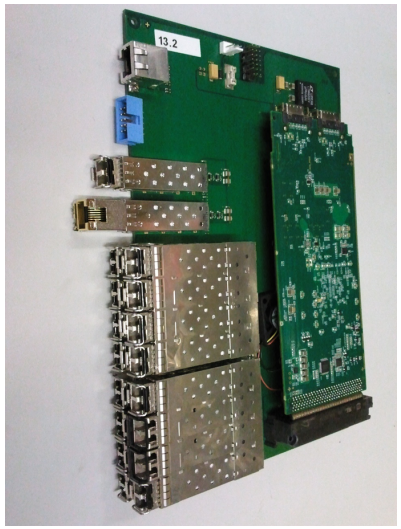
- faster - high speed serial links
- more flexible
- cheaper and more reliable

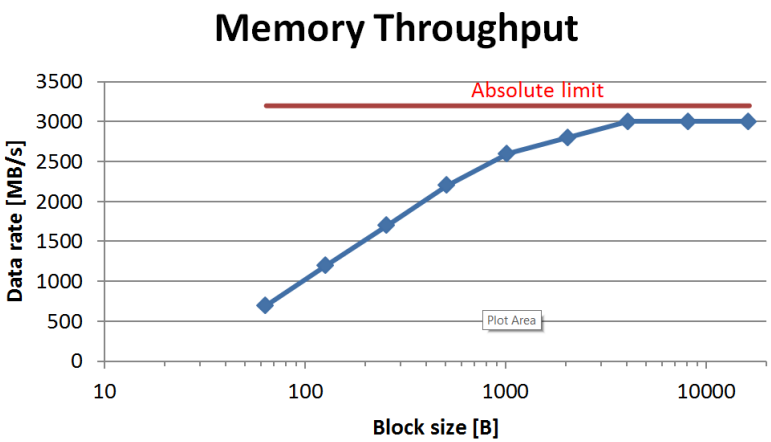




DAQ unit

- TCS (Trigger Control System) receiver - synchronization information
- 1 Gb Ethernet - control system link (IPbus)
- 16xSerial links - data links
  - Slink (2 Gbps)
  - Aurora (6.25 Gbps)
- 6 U VME form factor module → New DAQ fits in one 6 U VME crate

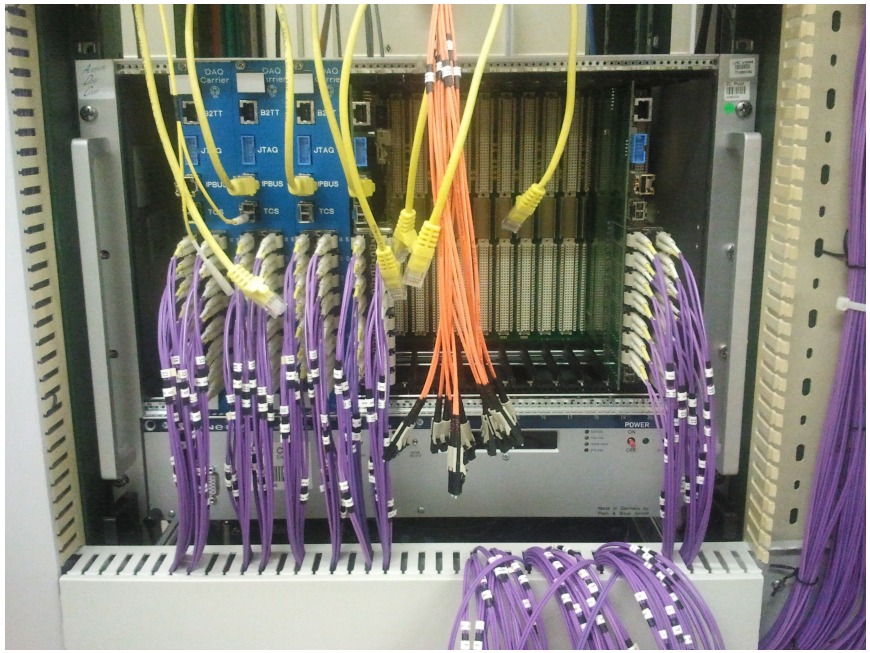


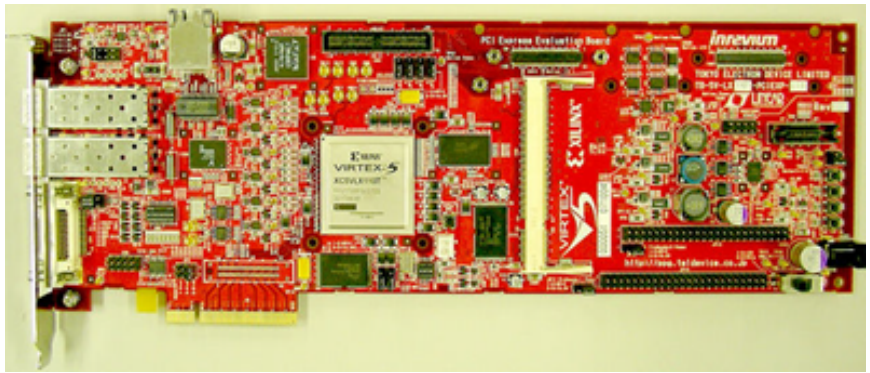


- AMC module, ATCA standard
- VIRTEX6 XC6VLX130T FPGA - middle sized FPGA and relatively cheap (500 Euro/chip)
- 4 GB DDR3
- Module programmed as MX 15:1 or SW 8x8 (can be recompiled to any NxM configuration)

New hardware parts

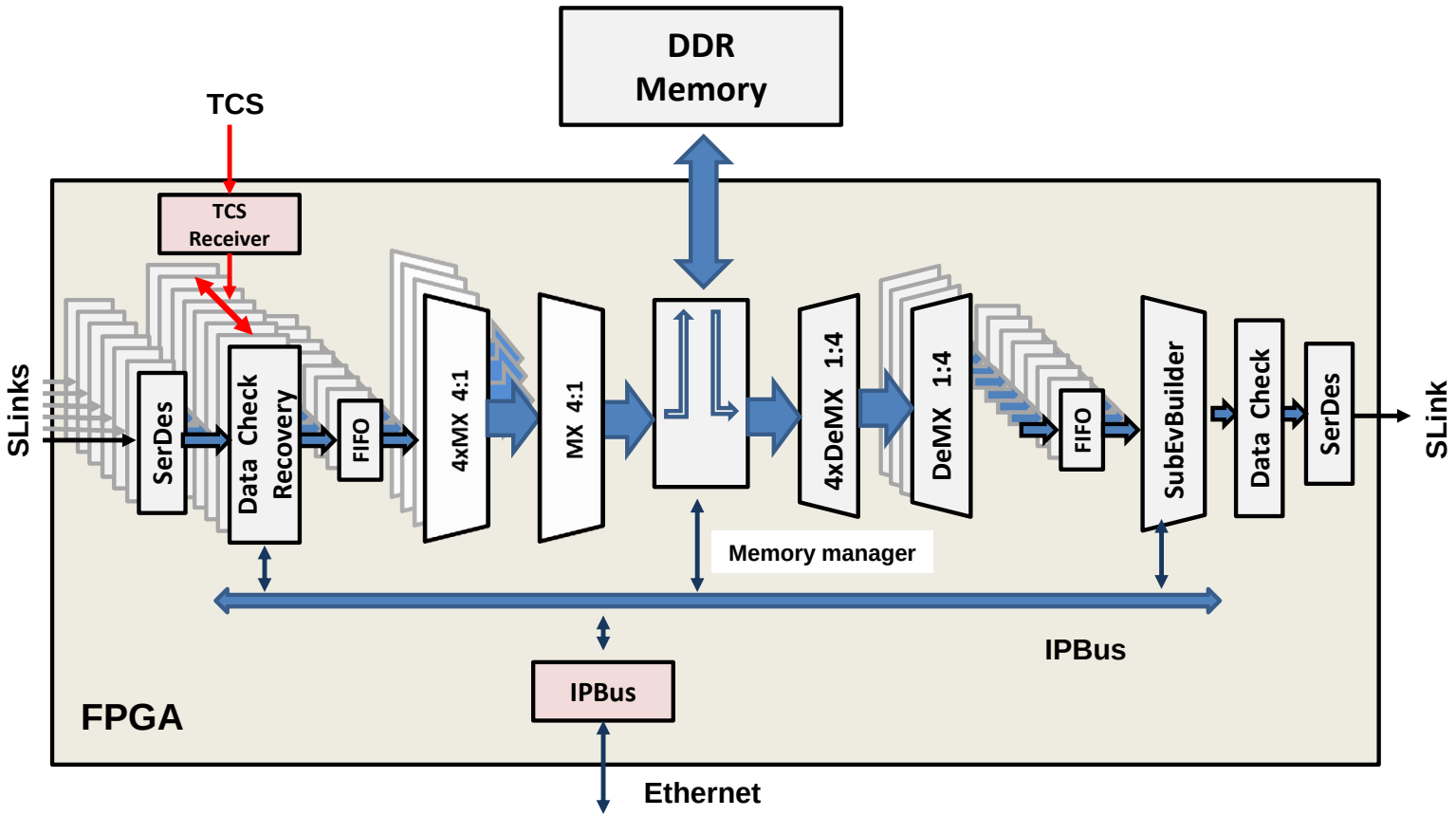
- 10 AMC cards + adapter cards
- 12 PCIe cards + 14 TCS receivers
- 6 TCS encoders/controllers
  - Substitute obsolete and not available TTC encoders
  - Wave length adapter from 1300 nm to 830 nm
  - IPbus for control and monitoring, VME is only for power and cooling





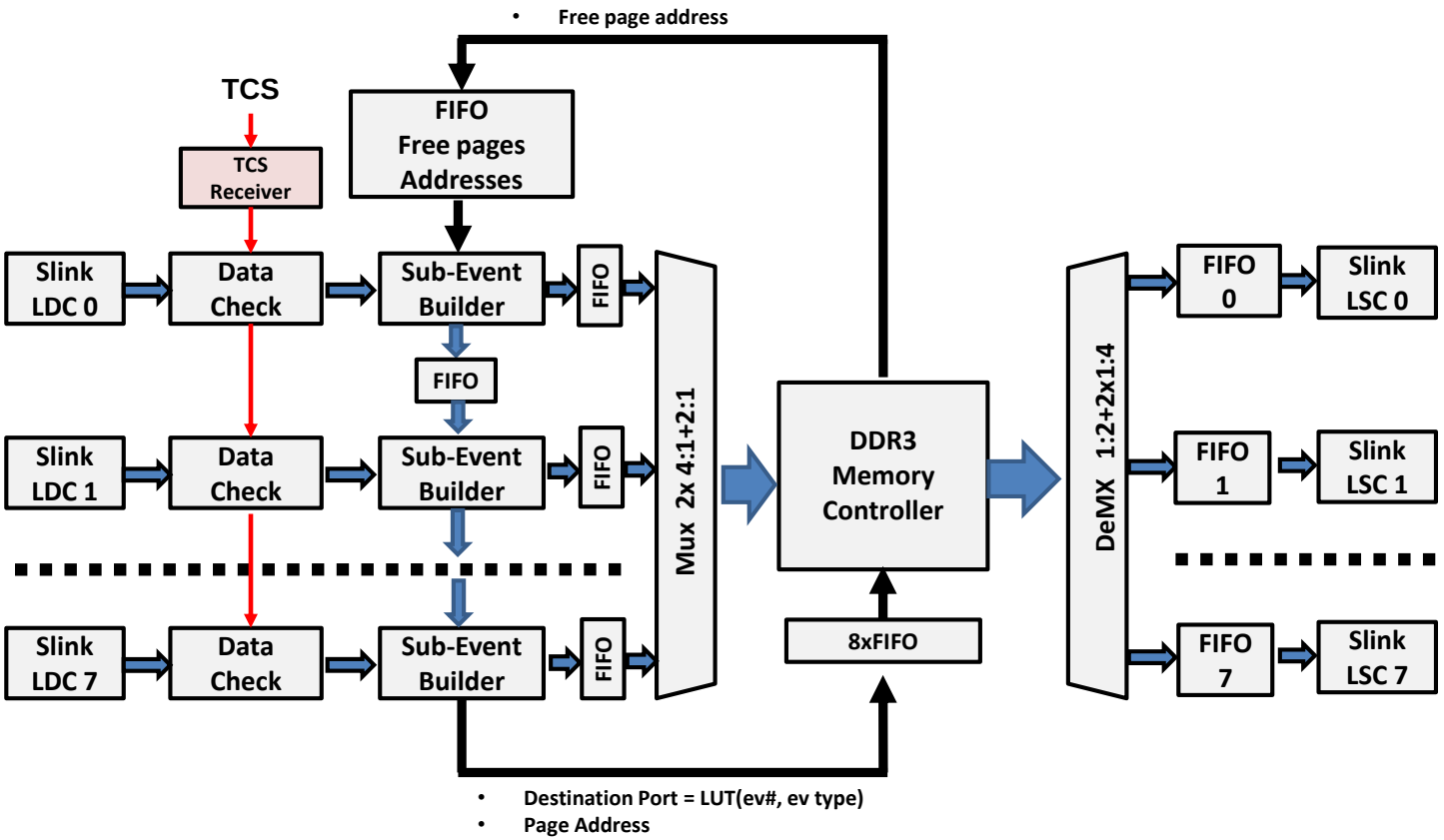
MX firmware

- buffering - enough memory to store one spill
- sub-event building



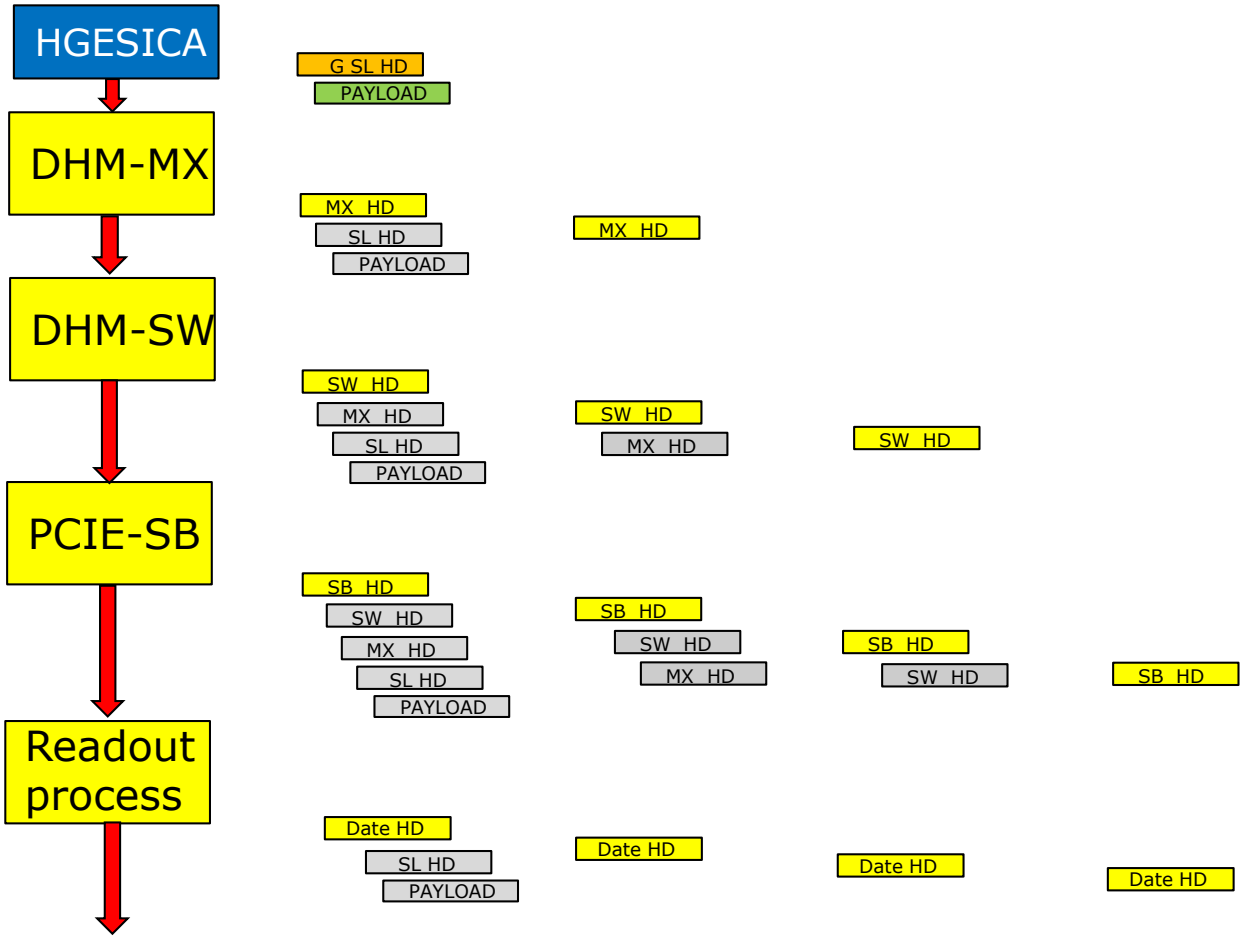
SW firmware

- DDR memory divided to 8k pages of 500kB each (bigger than maximum event size)
- Memory address is attached to data block header



Example of Data Flow and Data encapsulation

- Each step controls data and adds new header
- Data with errors thrown away and header generated

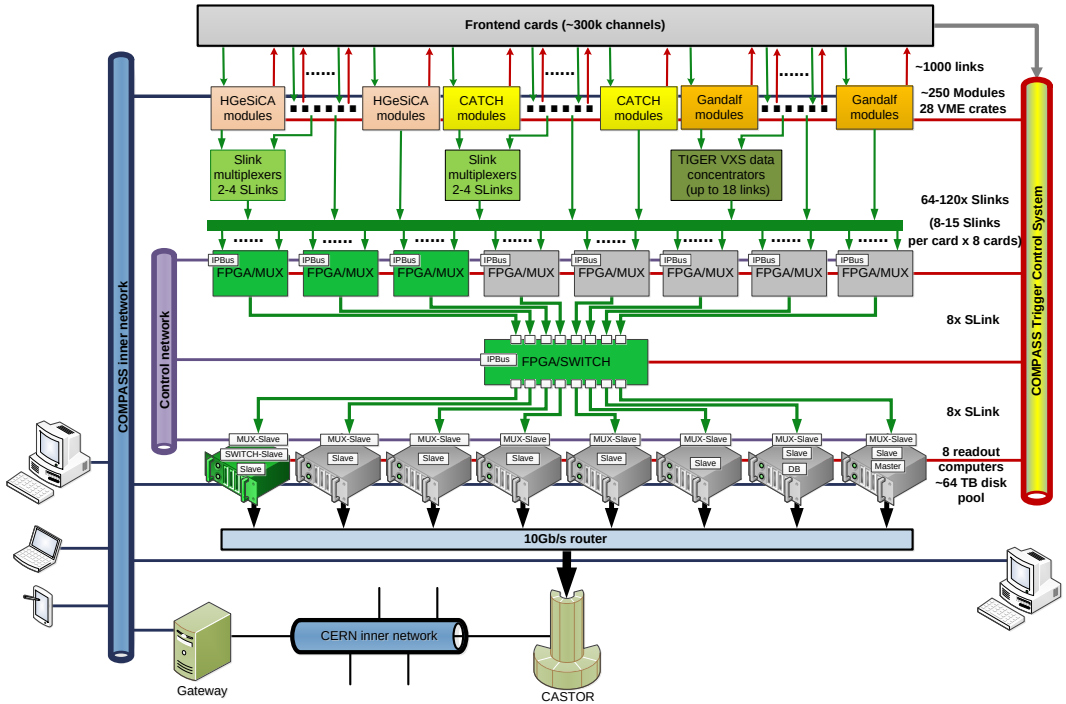


Used software technologies

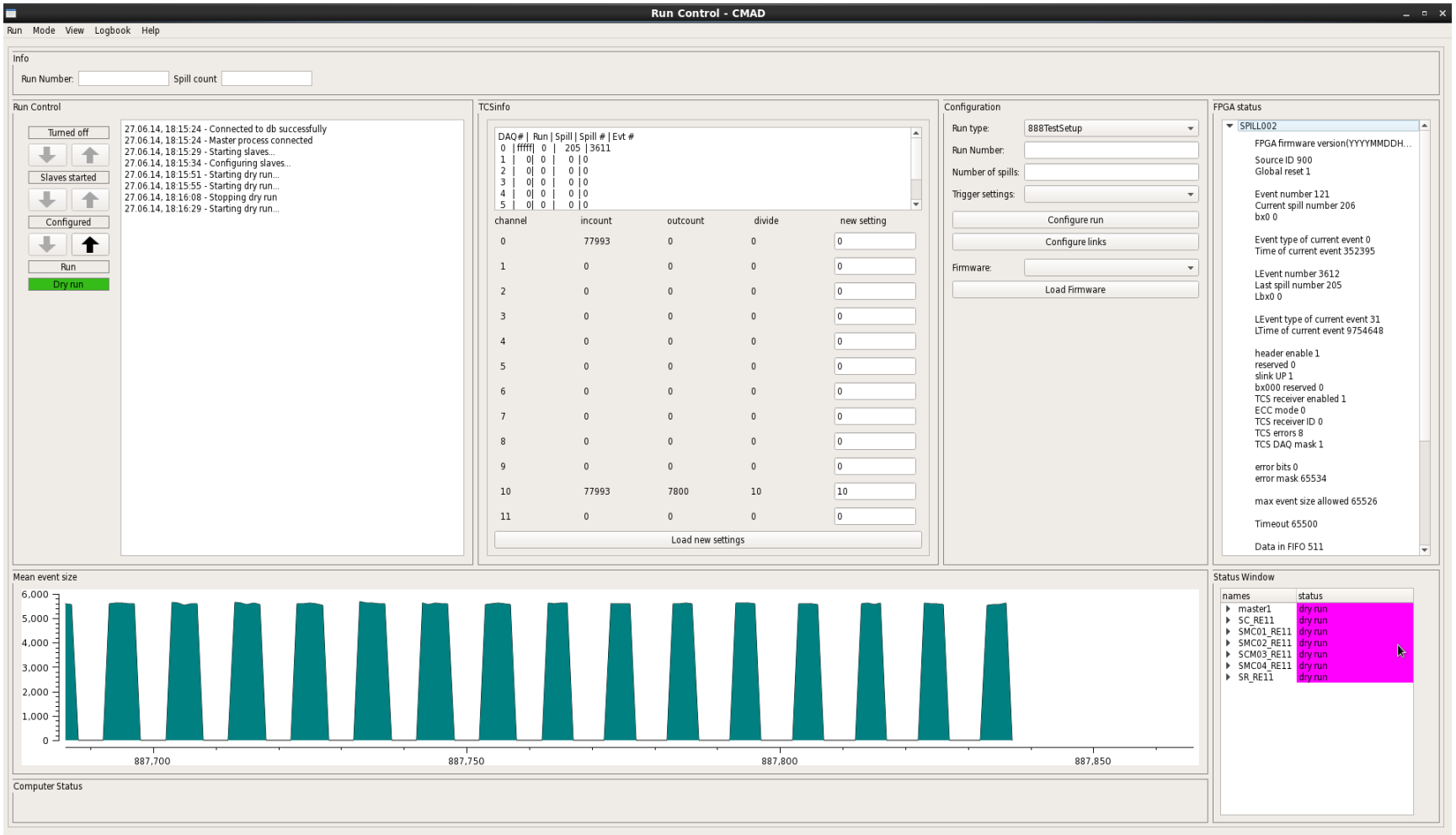
- C++, Python
- Qt framework
- DIM (Distributed Information Management System)
- IPbus suite for communication with FPGAs
- MySQL
- PHP, javascript
- Zabbix package used for computer resources monitoring

Present status

- preparation for commissioning
- fraction of detectors connected
- testing of links, data transmission and data handling

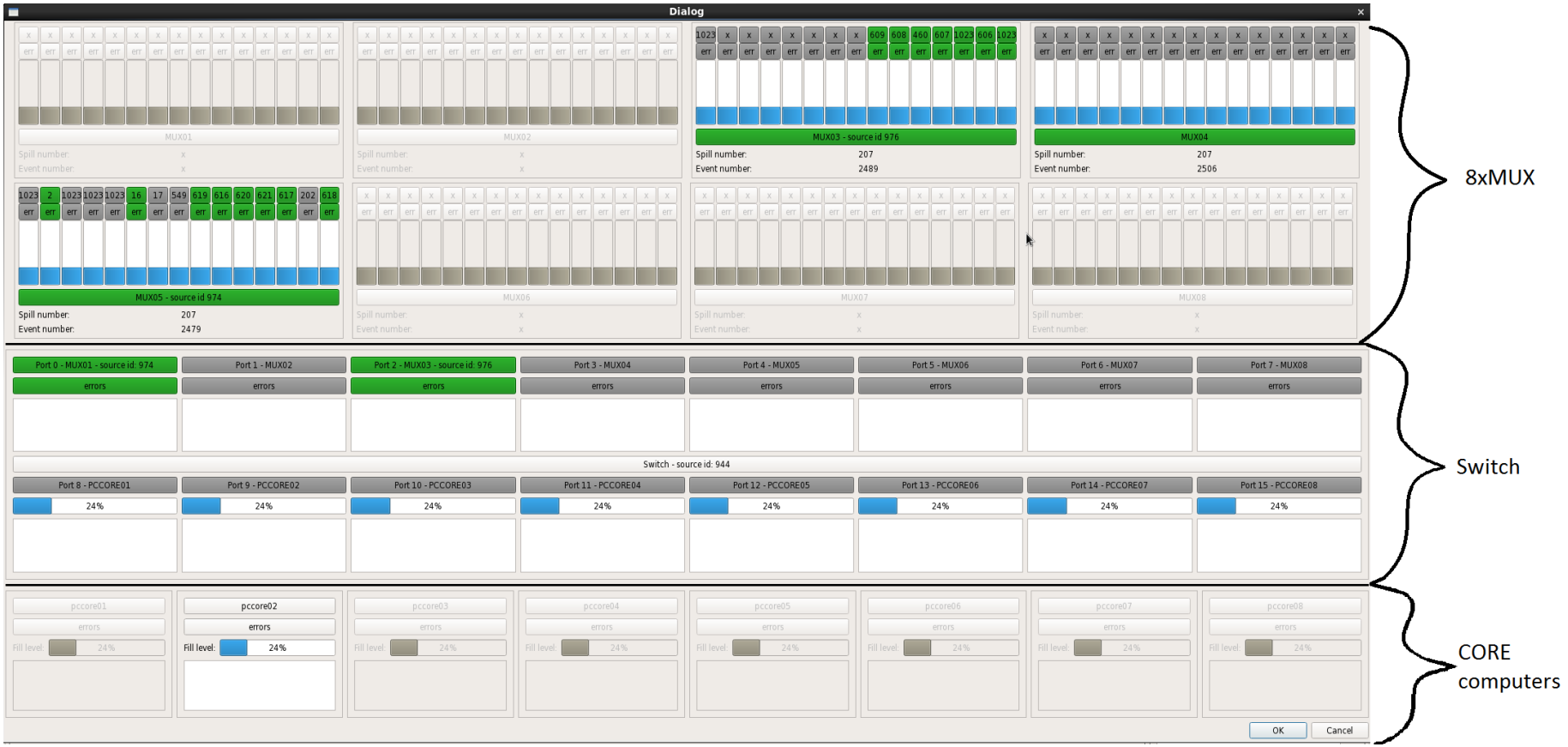


Run control GUI



DAQ system main window

- component status overview and configuration

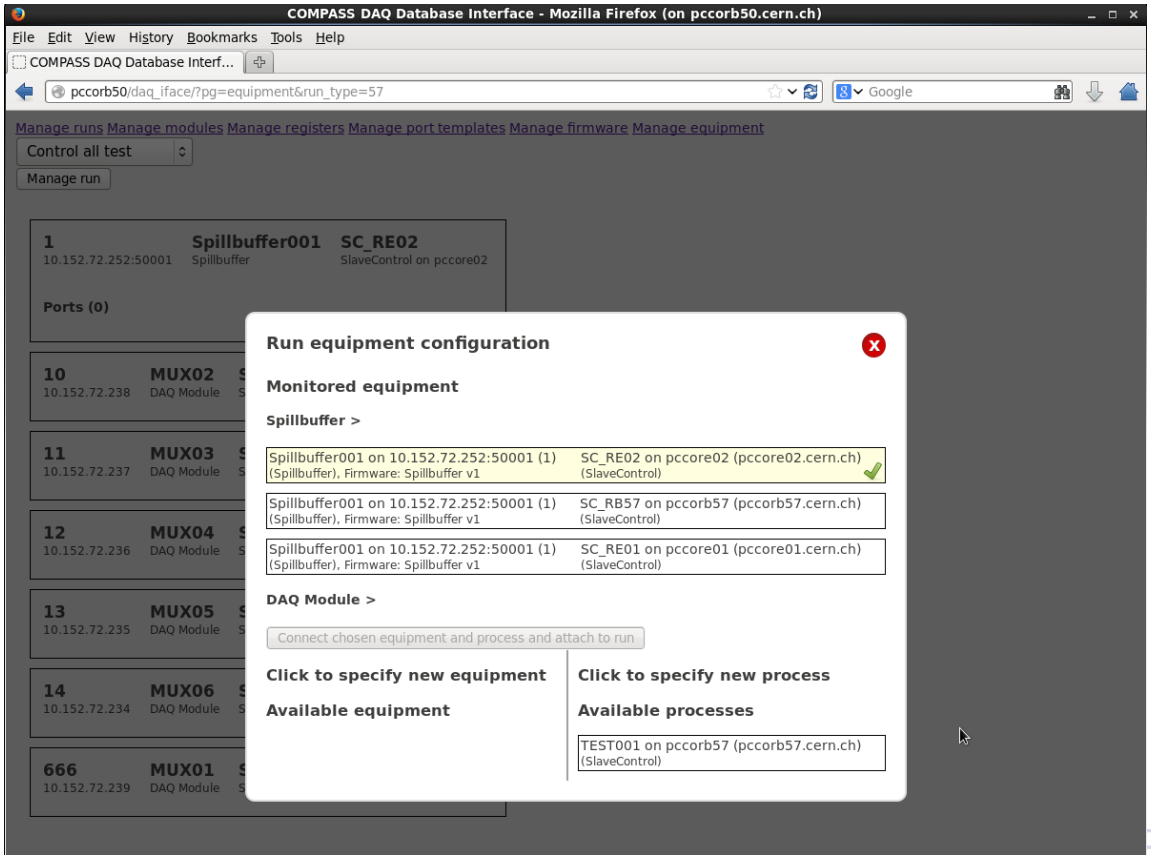


MessageBrowser

id	tm	dt	sender	severity	runNum	spillNum	eventNum	text
1	12:00 AM	11/11/11	6	FATAL ERROR	1000	1	5	Random text 3 6
2	1:00 AM	11/11/11	9	ERROR	1004	7	9	Random text 2 9
3	1:01 AM	11/11/11	8	ERROR	1004	13	3	Random text 2 8
4	1:01 AM	11/11/11	9	INFO	1004	13	12	Random text 0 9
5	1:01 AM	11/11/11	8	WARNING	1004	13	17	Random text 1 8
6	1:02 AM	11/11/11	7	INFO	1004	14	6	Random text 0 7
7	1:03 AM	11/11/11	8	WARNING	1004	22	9	Random text 1 8
8	2:03 AM	11/11/11	6	WARNING	1005	5	5	Random text 1 6
9	2:04 AM	11/11/11	2	FATAL ERROR	1005	14	4	Random text 3 2
10	2:04 AM	11/11/11	7	INFO	1005	14	7	Random text 0 7
11	2:04 AM	11/11/11	1	INFO	1005	14	14	Random text 0 1
12	2:04 AM	11/11/11	10	FATAL ERROR	1005	14	18	Random text 3 10
13	2:04 AM	11/11/11	8	WARNING	1005	14	22	Random text 1 8
14	2:05 AM	11/11/11	10	FATAL ERROR	1005	24	7	Random text 3 10
15	2:06 AM	11/11/11	4	FATAL ERROR	1005	31	3	Random text 3 4
16	2:06 AM	11/11/11	3	WARNING	1005	31	7	Random text 1 3
17	2:06 AM	11/11/11	7	WARNING	1005	31	10	Random text 1 7
18	3:06 AM	11/11/11	6	ERROR	1014	7	1	Random text 2 6
19	3:07 AM	11/11/11	10	WARNING	1014	12	9	Random text 1 10
20	3:08 AM	11/11/11	1	INFO	1014	19	10	Random text 0 1
21	3:09 AM	11/11/11	9	WARNING	1014	25	3	Random text 1 9
22	3:09 AM	11/11/11	9	ERROR	1014	25	10	Random text 2 9
23	3:09 AM	11/11/11	7	ERROR	1014	25	14	Random text 2 7
24	3:10 AM	11/11/11	4	INFO	1014	31	2	Random text 0 4
25	3:11 AM	11/11/11	9	ERROR	1014	37	4	Random text 2 9
26	4:11 AM	11/11/11	8	FATAL ERROR	1016	10	1	Random text 3 8
27	4:12 AM	11/11/11	7	ERROR	1016	12	10	Random text 2 7
28	4:12 AM	11/11/11	9	ERROR	1016	12	13	Random text 2 9
29	4:13 AM	11/11/11	10	WARNING	1016	17	9	Random text 1 10
30	4:14 AM	11/11/11	4	ERROR	1016	18	3	Random text 2 4
31	4:14 AM	11/11/11	2	WARNING	1016	18	4	Random text 1 2
32	4:15 AM	11/11/11	2	WARNING	1016	21	5	Random text 1 2
33	4:15 AM	11/11/11	9	FATAL ERROR	1016	21	10	Random text 3 9
34	4:15 AM	11/11/11	6	ERROR	1016	21	18	Random text 2 6
35	5:15 AM	11/11/11	5	INFO	1023	10	6	Random text 0 5
36	6:15 AM	11/11/11	9	INFO	1027	8	6	Random text 0 9
37	6:16 AM	11/11/11	9	ERROR	1027	15	4	Random text 2 9
38	6:16 AM	11/11/11	4	FATAL ERROR	1027	15	11	Random text 3 4
39	7:16 AM	11/11/11	3	INFO	1036	7	7	Random text 0 3
40	7:16 AM	11/11/11	3	ERROR	1036	7	11	Random text 2 3
41	8:16 AM	11/11/11	1	ERROR	1041	10	7	Random text 2 1
42	8:17 AM	11/11/11	5	FATAL ERROR	1041	17	8	Random text 3 5
43	8:18 AM	11/11/11	1	INFO	1041	19	5	Random text 0 1
44	8:18 AM	11/11/11	9	INFO	1041	19	14	Random text 0 9
45	9:18 AM	11/11/11	9	WARNING	1043	3	6	Random text 1 9

Configuration interface

- new configuration interface -> system fully configurable through web interface



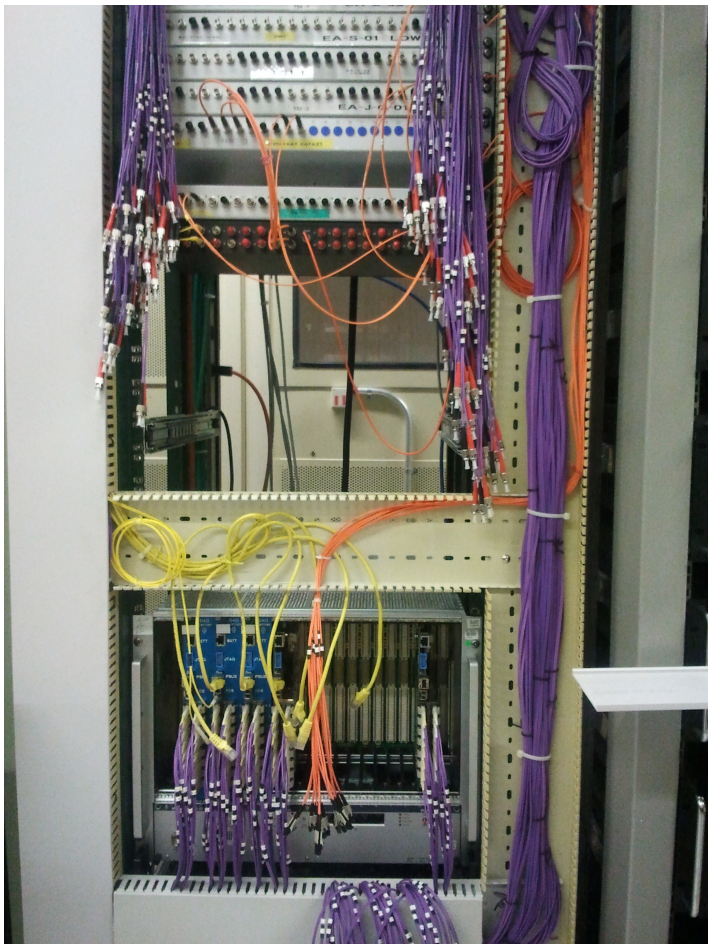
Present status - sub-DAQ tests

- XML description of DAQ structure and FPGA registers automatically generated from DB
- used for IPbus communication, event consistency checks, parsing of information from registers

```xml
<?xml version="1.0" encoding="UTF-8"?>
<structure>
    <hardware>
        <type>Spillbuffer</type>
        <action>remove</action>
        <source>1</source>
        <hardware>
                <type>MUX</type>
                <action>remove</action>
                <source>560</source>
        </hardware>
    </hardware>
    <hardware>
        <type>Spillbuffer</type>
        <action>remove</action>
        <source>2</source>
    </hardware>
    <hardware>
        <type>Spillbuffer</type>
        <action>remove</action>
        <source>3</source>
    </hardware>
</structure>
```

```xml
<?xml version="1.0" encoding="UTF-8"?>
<card id="REGISTERS">
        <block id="GB">
                <register id="IDReg" address="0x0" permission="r">
                        <register_part id="FPGAFV" mask="0xffff" description="FPGA firmware version"/>
                        <register_part id="DeID" mask="0xffff0000" description="Device ID"/>
                </register>
                <register id="SourceID" address="0x1" permission="rw">
                        <register_part id="SID" mask="0x3ff" description="Source ID"/>
                </register>
                <register id="CurEvNum" address="0x2" permission="r">
                        <register_part id="EN" mask="0xfffff" description="Event number"/>
                        <register_part id="CSP" mask="0x7ff00000" description="Current spill number"/>
                        <register_part id="bx0" mask="0x80000000" description="bx0"/>
                </register>
                <register id="CurEvTT" address="0x3" permission="r">
                        <register_part id="ETOCE" mask="0x1f" description="Event type of current event"/>
                        <register_part id="TOCE" mask="0xfffffe0" description="Time of current event"/>
                </register>
                <register id="LSpEvNum" address="0x4" permission="r">
                        <register_part id="LEN" mask="0xfffff" description="LEvent number"/>
                        <register_part id="LSN" mask="0x7ff00000" description="Last spill number"/>
                        <register_part id="Lbx0" mask="0x80000000" description="Lbx0"/>
                </register>
                <register id="LSpEvTT" address="0x5" permission="r">
                        <register_part id="LETOCE" mask="0x1f" description="LEvent type of current event"/>
                        <register_part id="LTOCE" mask="0xfffffe0" description="LTime of current event"/>
                </register>
                <register id="TCSStat" address="0x6" permission="rw">
                        <register_part id="IPBUST" mask="0x1" description="IPBUS TCS reciever enable"/>
                        <register_part id="S1A2E" mask="0x6" description="Slink 1 and 2 enable"/>
                        <register_part id="bx000R" mask="0x38" description="bx000 reserved"/>
                        <register_part id="TCSRE" mask="0x40" description="TCS receiver enabled"/>
                        <register_part id="ECCM" mask="0x80" description="ECC mode"/>
                        <register_part id="TCSRID" mask="0xff00" description="TCS receiver ID"/>
                        <register_part id="TCSE" mask="0xff0000" description="TCS errors"/>
                        <register_part id="TCSDM" mask="0xff000000" description="TCS DAQ mask"/>
                </register>
                <register id="FIFO1FL" address="0x7" permission="r">
                        <register_part id="FM1" mask="0xeffffff" description="Filled memory 1"/>
                </register>
                <register id="FIFO2FL" address="0x8" permission="r">
                        <register_part id="FM2" mask="0xeffffff" description="Filled memory 2"/>
                </register>
        </block></card>
```

Setting up new DAQ



Advantages of new DAQ

- More compact
- Flexible configuration
- Data verification on every step
- Less power demanding
- Easier to control (more time for reaction)

Conclusion

- communication system tested
- sub-DAQ tested without detectors
- expected peak performance 1.5 GB/s and sustainable 1.2 GB/s but real performance still to be measured
- on the route to commissioning by end of July

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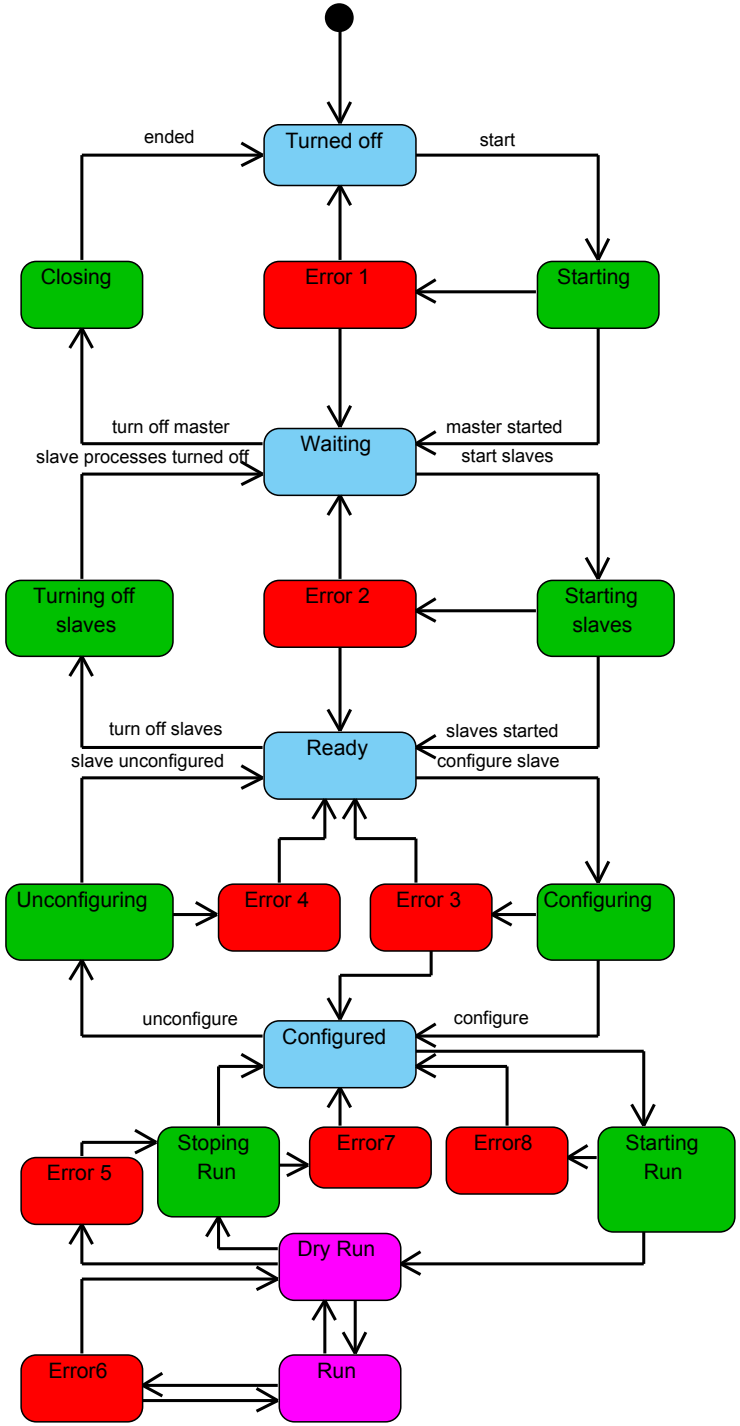


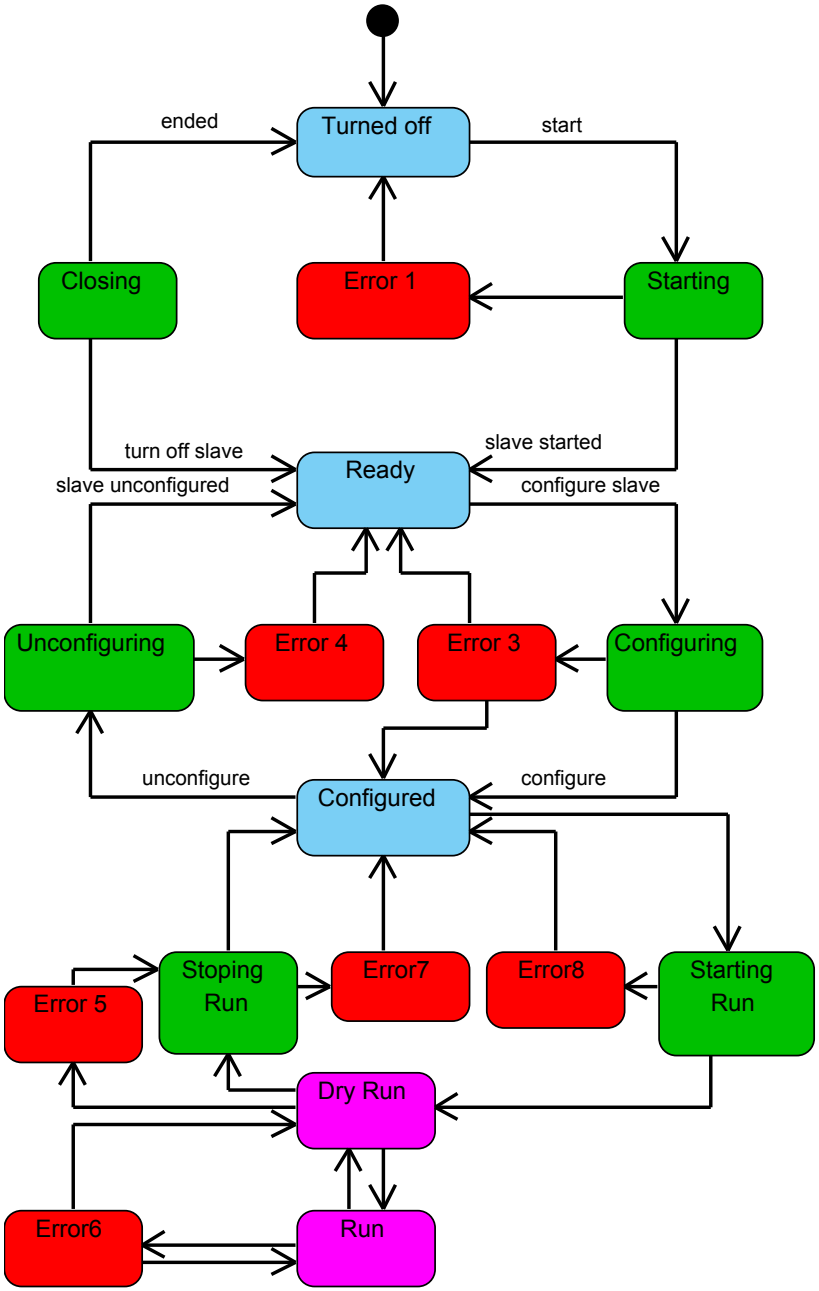
stable state,states that do nothing just wait for next command

transfere states(not stable), do not accept comm

error state

working states, stable untile command come or end condition is reached

number	name
0	Turned off
1	Waiting
2	Ready
3	Configured
11	Dry Run
12	Run
21	Starting
22	Closing
23	Starting slaves
24	Turning off slaves
25	Configuring
26	Unconfiguring
27	Starting run
28	Stoping Run
41-48	Error 1-8



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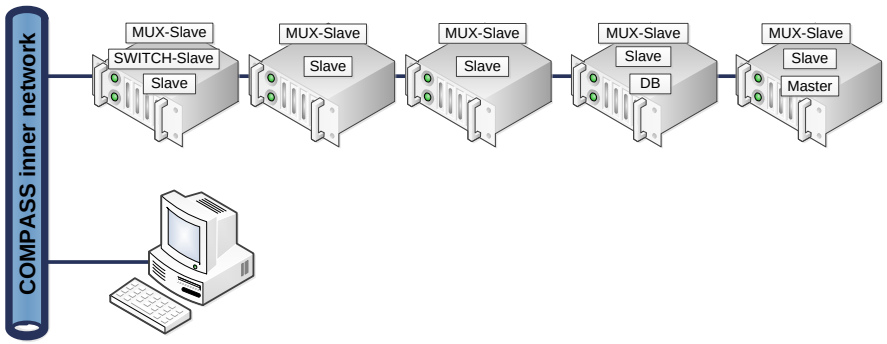
number	name
0	Turned off
2	Ready
3	Configured
11	Dry Run
12	Run
21	Starting
22	Closing
25	Configuring
26	Unconfiguring
27	Starting run
28	Stoping Run
41-48	Error 1-8

Route to final setup

- System tests phase 1 - communication tests [2]
- System tests phase 2 - readout tests [2]
- System tests phase 3 - multiplexer tests
- System tests phase 4 - sub-DAQ tests



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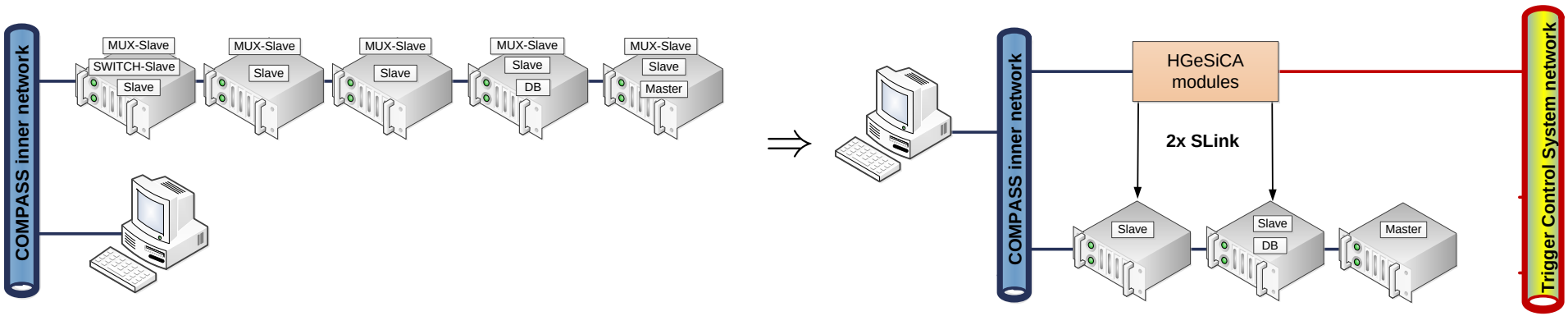

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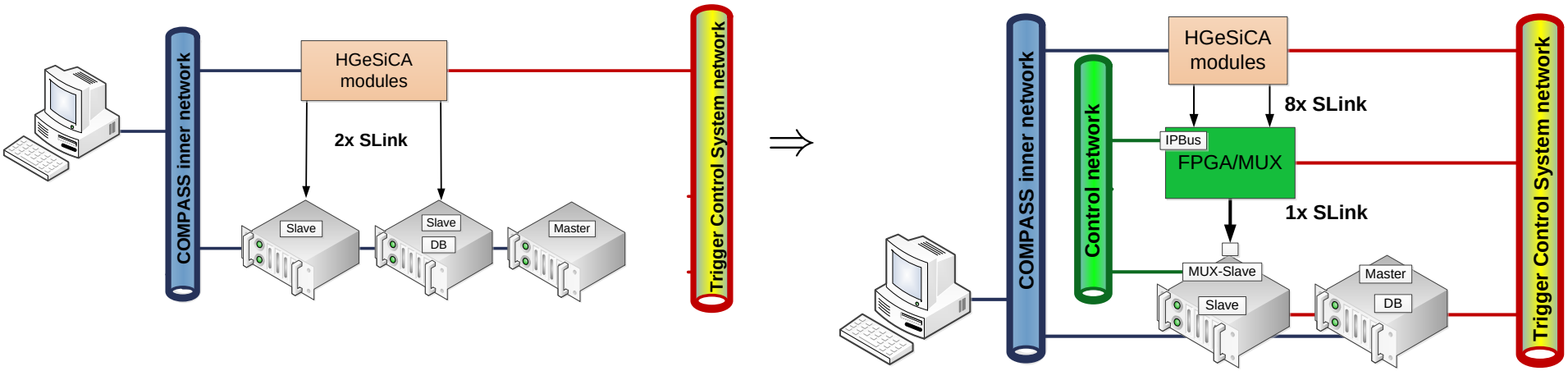

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