Development and Verification of a High Performance Electronic Readout Framework for High Energy Physics

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Dissertation
zur
Erlangung des Doktorgrades
der
Fakultät für Mathematik und Physik
der
Albert-Ludwigs-Universität
Freiburg im Breisgau

vorgelegt von
Florian Herrmann
aus
Offenburg

Freiburg, August 2011

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Korreferent:	Prof. Dr. Ulrich Landgraf
Tag der Verkündigung des Prüfungsergebnisses:	28.09.2011

Teile dieser Arbeit wurden in folgenden Fachzeitschriften veröffentlicht:

- S. Bartknecht et al., Nucl. Instrum. Methods Phys. Res., A **623** (2010) 507 - 509, doi:10.1016/j.nima.2010.03.052
- S. Bartknecht et al., Real Time Conference (RT), 2010 17th IEEE-NPSS, doi:10.1109/RTC.2010.5750360
- M. Alexeev et al., Nucl. Instrum. Methods Phys. Res., A **617** (2010) 396 - 397, doi:10.1016/j.nima.2009.08.087

*"A wizard is never late, nor is he early.
He arrives precisely when he means to."*

– Gandalf the White –

Contents

List of Figures

List of Tables

1. Introduction

Known matter in our universe is built up of two classes of particles: leptons and hadrons. While leptons, like the electron, seem to be elementary particles without any substructure, hadrons, among others represented by protons and neutrons, are compositions of other elementary particles. The first effect which led to the formulation of this concept was the discovery of the anomalous magnetic moment of the nucleon [1, 2].

The parton model was the first theory describing the constitution of baryons and mesons using quarks of different flavors. Since the 50s of the last century, high energy physics experiments have been set up to discover and prove this concept [3]. Today we know from these experiments that the nucleon consists of three valence-quarks surrounded by sea-quarks and gluons. The interaction, which provides the cohesion of these partons, is described by a comprehensive mathematical theory, Quantum Chromo Dynamics.
Knowing this, one obvious question to proof this theoretical description of hadronic matter is:

As nucleons have a substructure, how do the characteristics of the constituents contribute to the appearance of the nucleon?

During the last decades studies in high energy physics have been focused on answering this question. The research based on the quark parton model determines how the momenta of separate partons can be constituted to the total momentum of the nucleon. This has led to parton distribution functions which describe this composition of momentum.

Another characteristic which is yet to be understood is the spin of the nucleon. In order to address this question, studies were performed to determine which contributions of the spin, carried by the partons, sum up to the total spin of the nucleon. In the 80s of the last century it turned out that the answer to this question cannot be described in a simple naive model. Initial measurements from the European Muon Collaboration, followed by further experiments at CERN[1], DESY[2] and SLAC[3] National Accelerator Laboratory showed that the contribution from quark and anti-quark spins alone cannot compose the total spin of the nucleon [4].

A ground breaking research performed at the COMPASS[4] experiment at CERN was the measurement of the gluon helicity which turned out to be much smaller than expected by theorists. The result did not confirm the prevailing concepts of a nucleon spin

[1] **C**onseil **E**uropéen de la **R**echerche **N**ucléaire, Geneva
[2] **D**eutsches **E**lektronen **Sy**nchroton, Hamburg
[3] **S**tanford **L**inear **A**ccelerator **C**enter, Stanford
[4] **Co**mmon **M**uon and **P**roton **A**pparatus for **S**tructure and **S**pectroscopy

composed of quark and gluon spins only, because the measured gluon contributions are marginal.
A new approach to describe the structure of the nucleon is provided by the concept of Generalized Parton Distributions (GPD). This theoretical framework allows for accessing the total angular momentum of partons separated in contributions from quarks and gluons. With the measurement of the total angular momenta, the maybe last part of the *spin puzzle* of the nucleon can be solved.

To access information about the GPD exclusive measurements of Deeply Virtual Compton Scattering (DVCS) processes are planned coming along with an upgrade of the COMPASS spectrometer. This measurement requires an exclusive detection of the particles in the final state of the process. This exclusivity can be accomplished by extending the existing COMPASS spectrometer with detectors for hermeticity. Recoiled protons scattered off the fixed target need to be detected exclusively as well as the scattered muon and the photon, produced during the DVCS process. While the muon and the photon can be detected by the COMPASS-II spectrometer, a new detector, the CAMERA[5], will be installed surrounding the fixed target to detect the recoiled proton from background.

The characteristics of the electronic output signal from the CAMERA detector like rate, pile-up and pulse shape requires the development of a special readout system. The GANDALF[6] framework was developed to cover the electronic readout challenges for this detector. The development and verification of this readout system for the CAMERA detector is the main purpose of the work performed within the completion of this thesis.

The expected detector pulse shapes have a rise time in the nanosecond-range and a high repetition rate which makes it impossible to perform the readout task with conventional electronic readout systems without introducing unnecessarily single channel dead times. The occurrence of the pulses has to be determined with a precision in the picosecond-range to enable time-of-flight measurements of the recoiled protons. In addition, an online trigger signal on the characteristics of a recoiled proton in the detector should be implemented to allow for optimum efficiency for the measurement of the rare DVCS events. Therefore, the readout system must also have the capability to process the combined information of all detector channels.

In the following chapter a short introduction for the importance of GPD and their interpretations will be presented. It will be explained how the measurement of the DVCS process allows for a promising access to the GPD.
The third chapter will provide an overview of the COMPASS-II experiment upgrade [5], focusing on the major extension of the experiment e.g. the CAMERA detector which is needed for the exclusive measurement of DVCS events. The proposal for the experiment has already been approved by the SPSC[7].
The GANDALF framework consists of different programmable electronic components. There are different mezzanine cards, which can be combined with the GANDALF module. This modularity of the system allows a variety of application fields. An overview of the

[5] **C**ompass **A**pparatus for **M**easuring **E**xclusive **R**e**A**ctions
[6] **G**eneric **A**dvanced **N**umerical **D**evice for **A**nalytic and **L**ogic **F**unctions
[7] **S**uper **P**roton **S**ynchrotron **C**ommittee

hardware and software parts developed within this framework will be given in chapter four.
The chapter *Pulse Shape Analysis* will focus on the theory of different algorithms applied on detector pulse shapes to extract characteristics like time and amplitude information. The performance of the GANDALF framework operated as a *transient analyzer* will also be demonstrated. Further on, the experimental results obtained while using GANDALF modules to analyze detector pulses during various experimental and laboratory test measurements will be given.
Chapter six concludes with a summary on the work and results obtained within this thesis. This last chapter will be followed by an appendix filled with concise technical information about the printed circuit board, firmware registers, connectivity tables and specifications created within the development, production and operation of the GANDALF framework.

2. Theoretical Motivation

2.1 The Spin Structure of the Nucleon

The spin of the nucleon is known to be 1/2 of $\hbar$, the Planck constant. As the nucleon is composed of quarks and gluons, the spin of the nucleon can be written as the sum of the contributions from its constituents [6]:

$$\frac{J}{\hbar} = \frac{1}{2} = J_q + J_g, \tag{2.1}$$

where J_q and J_g are the total angular momenta of the quarks and gluons inside the nucleon. While from preceding experiments the contributions of quarks, anti-quarks and gluon helicity are known to be $\Delta\Sigma \approx 0.3$ and $|\Delta G| \approx 0.2 - 0.3$ [7], yet there is no knowledge of the angular momenta of quarks L_q and of gluons L_g, which sum up to the total spin S:

$$\frac{S}{\hbar} = \frac{1}{2} = \frac{1}{2}\Delta\Sigma + \Delta G + L_q + L_g. \tag{2.2}$$

With the future knowledge of the Generalized Parton Distributions (GPD) H^f and E^f, the total angular momentum of the quarks and gluons can be constraint by using the Ji relation [8]:

$$J_f = \frac{1}{2}\lim_{t\to 0}\int_{-1}^{1} dx\; x\left[H^f + E^f\right], \tag{2.3}$$

where J_f denotes the total angular momenta for quarks or gluons ($f = q,\, g$).
The following section will give an overview of the definition of the GPD, their interpretation as well as how they can be accessed by measuring the Deeply Virtual Compton Scattering (DVCS) cross sections.

2.2 Deep Inelastic Scattering

The structure of the nucleon can be investigated in deep inelastic scattering (DIS) processes. Here an incoming leptonic probe is scattered off a quark inside the nucleon by exchanging a virtual photon γ^*. The scattered quark leaves the core of the nucleon and fragments into one or more hadrons:

$$l + N \to l' + X, \tag{2.4}$$

where l and l' denote the incoming and outgoing lepton scattered off the nucleon N and X describes the final state hadrons. This measurement is called inclusive if it scopes on the lepton only. In semi-inclusive measurements at least one generated hadron is detected in addition. If all particles in the final state are detected, the measurement will be called exclusive.
The DIS processes are described in the infinite momentum frame, where the nucleon carries an infinite momentum and the transverse momenta of the constituents can be neglected compared to the longitudinal momentum. In Fig. 2.1 a simplified schematic of a semi-inclusive deep inelastic scattering is given. Important variables used to describe DIS processes are listed in Tab 2.1.

Table 2.1: Kinematic variables in DIS

$p = (E, \vec{p}) \overset{\text{lab}}{=} (E, 0, 0, \lvert\vec{p}\rvert)$	- four momentum of the incoming lepton
$p' = (E', \vec{p'})$	- four momentum of the outgoing lepton
$P = (E_P, \vec{P}) \overset{\text{lab}}{=} (M_P, 0, 0, 0)$	- four momentum of the proton
$q = p - p'$	- four momentum of the virtual photon
$Q^2 = -q^2 \overset{\text{lab}}{\approx} 4EE' \cdot sin^2\vartheta/2$	- negative square of the four momentum of the virtual photon
$\nu = \frac{P \cdot q}{M}$	- Energy loss of the scattered lepton
$y = \frac{P \cdot q}{P \cdot p} \overset{\text{lab}}{=} \frac{\nu}{E}$	- Fractional energy of the virtual photon
$x_{Bj} = \frac{Q^2}{2P \cdot q} \overset{\text{lab}}{=} \frac{Q^2}{2M \cdot \nu}$	- Bjorken variable

2.3 Parton Distribution Functions

An interpretation of the structure of the nucleon is given by the quark parton model [10]. Here the nucleon is constituted by point-like particles: the partons. These are identified with quarks carrying spin $\frac{1}{2}$ and gluons with spin 1.
In the Bjorken limit, where

$$Q^2, \nu \to \infty, \text{ with } x_{Bj} = const. \tag{2.5}$$

the DIS process can be separated into a hard leptonic and a soft hadronic part. This separation is expressed in the cross section for this process [11, 12]:

$$\frac{d^2\sigma}{\mathrm{d}x_{Bj}\mathrm{d}y} = \frac{2\pi y\alpha^2}{Q^4} L_{\mu\nu} W^{\mu\nu}, \tag{2.6}$$

where $L_{\mu\nu}$ is the leptonic tensor describing the scattering of the virtual photon off a quark and the hadronic tensor $W^{\mu\nu}$ describes the internal structure of the nucleon.

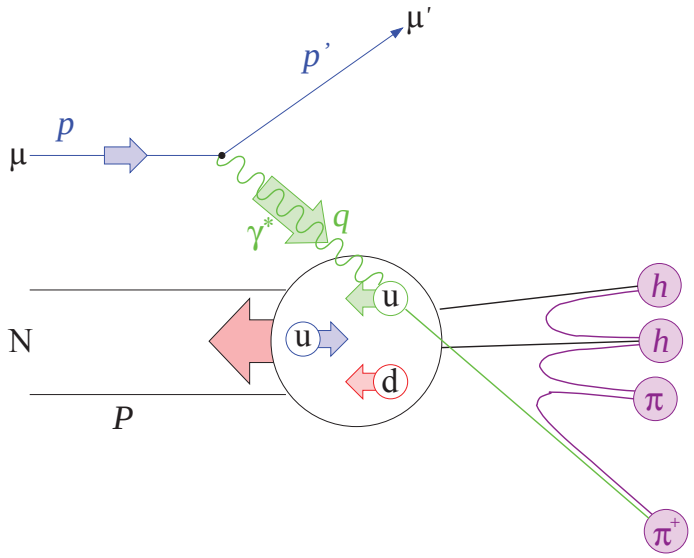


Figure 2.1: Simplified schematic diagram of semi-inclusive deep inelastic scattering [9].

While the former tensor can be calculated in QED the second expression for the "soft" hadronic part can be parametrized with parton distribution functions (PDFs). The cross section in (2.6) can be expressed by using the structure functions F_1 and F_2 for DIS on unpolarized nucleons [13]:

$$\frac{\mathrm{d}^2\sigma}{\mathrm{d}x_{Bj}\mathrm{d}y} = \frac{4\pi\alpha^2}{x_{Bj}yQ^2}\left[y^2 x_{Bj}F_1(x_{Bj}) + \left(1 - y - \frac{x_{Bj}^2 y^2 M^2}{Q^2}\right)F_2(x_{Bj})\right]. \tag{2.7}$$

With the structure functions g_1 and g_2 the cross section for a longitudinally polarized nucleon is given by:

$$\frac{\mathrm{d}^2\Delta\sigma}{\mathrm{d}x_{Bj}\mathrm{d}y} = \frac{8\pi\alpha^2}{x_{Bj}yQ^2}\left[\lambda_l y\left(2 - y - 2x_{Bj}^2 y^2\frac{M^2}{Q^2}\right)x_{Bj}g_1(x_{Bj}) - \lambda_l 4x_{Bj}^3 y^2\frac{M^2}{Q^2}g_2(x_{Bj})\right] \tag{2.8}$$

where λ_l represents the helicity (± 1) of the incoming lepton.

2.3.1 Unpolarized PDFs

In the quark parton model the unpolarized parton distribution functions are related to two structure functions F_1 and F_2 occurring in (2.7):

$$F_1(x_{Bj}) = \frac{1}{2}\sum_f e_f^2 q_f(x_{Bj}), \tag{2.9}$$

$$F_2(x_{Bj}) = x_{Bj}\sum_f e_f^2 q_f(x_{Bj}), \tag{2.10}$$

where F_1 can be derived from magnetic interaction and is $F_1 = 0$ for particles without spin. The function $q_f(x_{Bj})\mathrm{d}x_{Bj}$ defines the probability to find a quark with flavor f which carries a fraction of the nucleons momentum in the range of x_{Bj} to $x_{Bj} + \mathrm{d}x_{Bj}$. This interpretation is valid in the infinite momentum frame, where the Bjorken variable x_{Bj} describes the fraction of the momentum which is carried by the parton. The structure function F_2 expresses the sum over the flavours of the momentum distributions of quarks and anti-quarks weighted with the squared charge e_f. The expressions (2.9) and (2.10) lead to the Callan-Gross relation which includes the evidence that quarks carry the spin of $\frac{1}{2}$ [14]:

$$F_2(x_{Bj}) = 2x_{Bj}F_1(x_{Bj}). \tag{2.11}$$

Measurement results prove the dependency of the structure function F_2 on Q^2 (see Fig. 2.2). This behavior can be explained with the fact that valence quarks inside the nucleon are surrounded by sea quarks carrying small momentum fractions. Together with Q^2 the resolution increases and detects more sea quarks at higher Q^2. Therefore, more partons at small x_{Bj} can be found with increasing Q^2.

2.3.2 Polarized PDFs

The helicity distribution of the quarks is described by the polarized distribution function $\Delta q_f(x_{Bj})$. For longitudinally polarized nucleons, this distribution is defined as:

$$\Delta q_f(x_{Bj}) = q_f^{\rightrightarrows}(x_{Bj}) - q_f^{\rightleftarrows}(x_{Bj}). \tag{2.12}$$

It expresses the difference of the probability that a struck quark carries the momentum fraction x and its helicity is parallel $q_f^{\rightrightarrows}(x_{Bj})$ or anti-parallel $q_f^{\rightleftarrows}(x_{Bj})$ to the spin of the nucleon. Due to helicity conservation in the scattering process, the virtual photon can only be absorbed by a quark with a helicity direction opposite to the photon helicity. In this context the comparable expression for the unpolarized distribution function is:

$$q_f(x_{Bj}) = q_f^{\rightrightarrows}(x_{Bj}) + q_f^{\rightleftarrows}(x_{Bj}). \tag{2.13}$$

The spin dependent structure function $g_1(x_{Bj})$ can be related to the polarized distribution functions, where

$$g_1(x_{Bj}) = \frac{1}{2}\sum_f e_f^2 \Delta q_f(x_{Bj}). \tag{2.14}$$

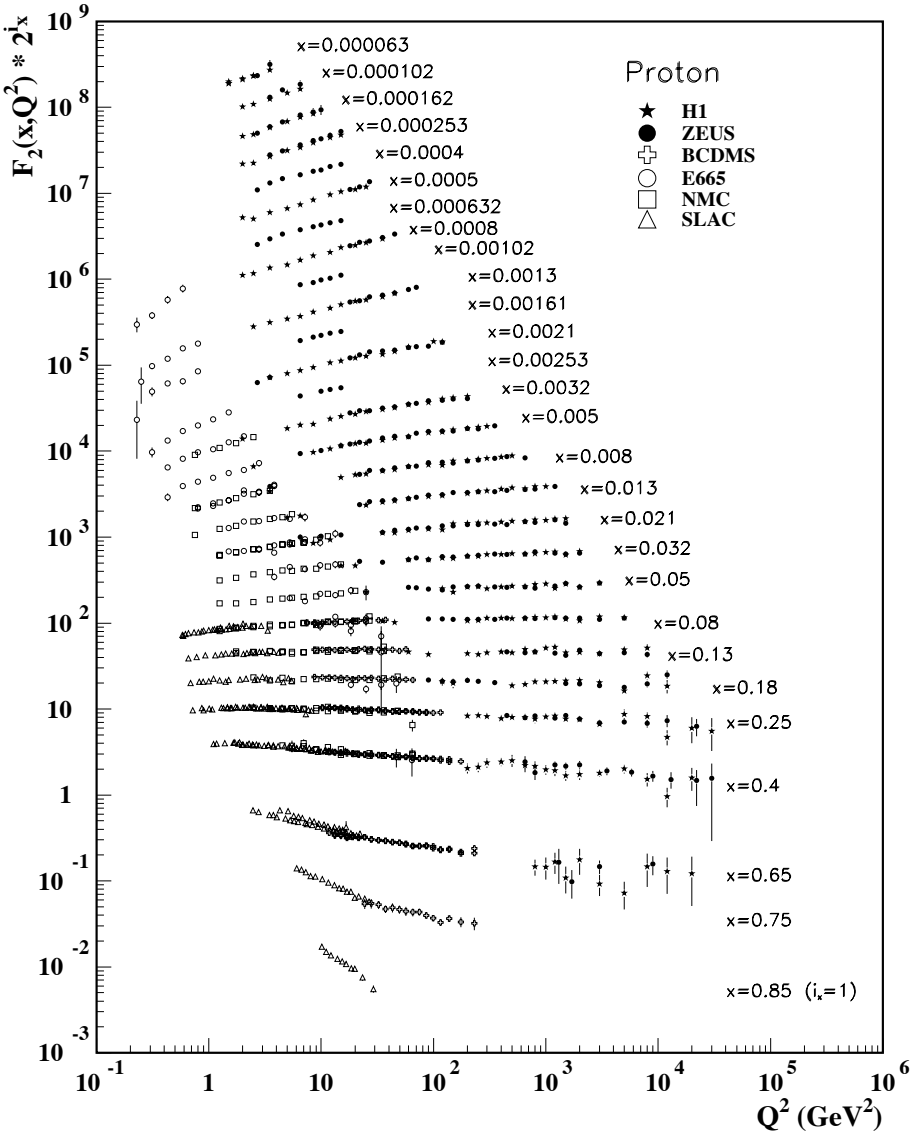


Figure 2.2: Proton structure function F_2 in dependency on Q^2 for different values of x_{Bj} (in this plot x_{Bj} is replaced by x) [13]. For the purpose of plotting, F_2 has been multiplied by 2^{i_x} where i_x is the number of the x_{Bj} bin ranging from $i_x = 1$ ($x_{Bj} = 0.85$) to $i_x = 28$ ($x_{Bj} = 0.000063$).

This structure function is used to describe the cross section for polarized nucleons (see Eq. (2.8)). In Fig. 2.3 measurements of xg_1 for proton, deuteron and neutron is given. In the quark parton model there is no expression using PDFs for the spin dependent structure function g_2.

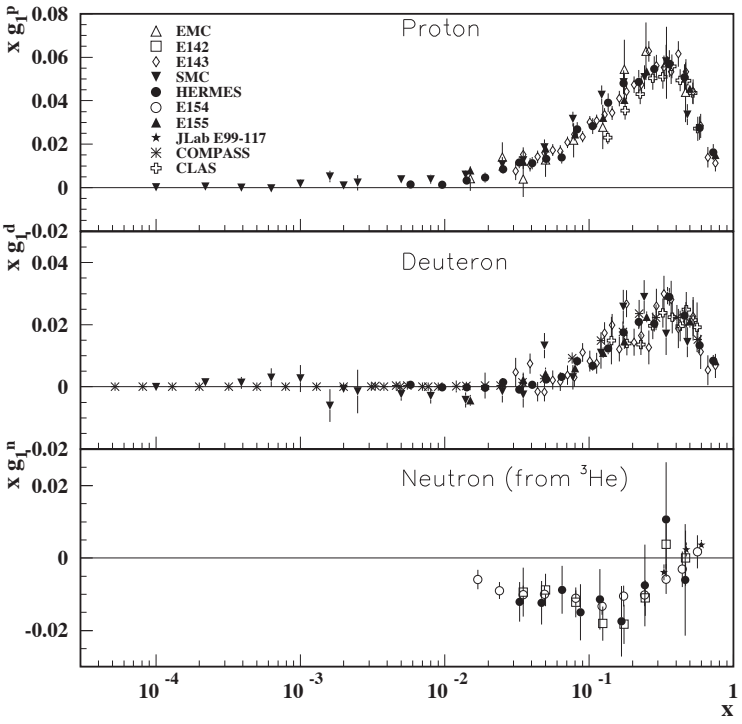


Figure 2.3: Spin dependent structure function xg_1 for proton, deuteron and neutron measured with polarized deep inelastic scattering at different fixed target experiments [13].

The distribution $\Delta q_f(x_{Bj})$ can be used to describe the contribution of the helicity of the quarks and anti-quarks $\Delta\Sigma$ to the total spin of the nucleon:

$$\Delta\Sigma = \sum_f \Delta q_f(x_{Bj}), \tag{2.15}$$

where $\Delta q_f(x_{Bj})$ can be calculated by the integration of the polarized parton distributions:

$$\Delta q_f = \int_0^1 dx_{Bj} \Delta q_f(x_{Bj}). \tag{2.16}$$

2.4 Generalized Parton Distributions

Generalized Parton Distributions (GPD) are a versatile description of the structure of the nucleon. GPD combine information about the electric form factors of the nucleon together with the parton distribution functions measured in DIS.
A "nucleon tomography", concerning transverse spatial information and longitudinal momentum information, can be derived from GPD. They also allow for a view on the total angular momenta of quarks and gluons inside the nucleon. The following sections will introduce to the definition and interpretation of the GPD.

The factorization theorem used in deep inelastic scattering, describing the process with a separation in a soft and a hard part can be applied in the context of GPD for large virtualities. The interaction between the virtual photon and a quark from the nucleon can be separated from remaining nucleon structure in the "soft part" of the process using the GPD as a universal description [15]. In Fig. 2.4 a handbag diagram for the Deeply Virtual Compton Scattering (DVCS) process in the Bjorken limit ($Q^2 \to \infty$, fixed x_{Bj} and small $|t|/Q^2$) is given.

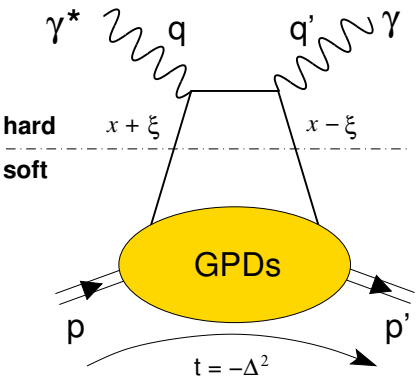


Figure 2.4: Handbag diagram for the DVCS process [5]. The soft part is described by Generalized Parton Distribution functions. The kinematic variables are explained in section 2.4.1.

2.4.1 Kinematic Variables

In the following an additional set of kinematic variables describing the GPD will be introduced. They depend on the photon virtuality $Q^2 = -q^2$ (see Tab 2.1) and the transferred total four-momentum

$$t = (p - p')^2 = (q - q')^2 = -\Delta^2 \tag{2.17}$$

between the initial and final state of the nucleon. Additional variables are x and ξ which give the average as well as half the difference between the initial and the final longitudinal momentum fractions of the nucleon which is carried by the parton in the "hard part" of the process. In the DVCS process the x variable is integrated over a

function which is the convolution with a GPD and the function describing the "hard part" of the process.
Here, the Bjorken variable $x_{Bj} = \frac{Q^2}{2 \cdot p \cdot q}$ is related to the "skewness" ξ of the process in the Bjorken limit:

$$\xi = \frac{x_{Bj}}{2 - x_{Bj}}. \tag{2.18}$$

This value corresponds to the direction of the momentum transfer in relation to the direction of the momentum in the infinite momentum frame. In case that $\xi = 0$, both momenta will be orthogonally orientated, if $\xi \neq 0$ the momentum transfer will possess parts with the same direction as the virtual photon.
The nucleon helicity conservation in the scattering process is described by the GPD H^f and $\tilde{H}^f$ with $f = u,\ d,\ s,\ g$. The GPD E^f and $\tilde{E}^f$ describe the case of a nucleon-helicity flip in the scattering process.

Table 2.2: Four Spin-$\frac{1}{2}$ GPD: There are two GPD $(H, \tilde{H})$ describing nucleon-helicity conservation and two GPD $(E, \tilde{E})$ describing nucleon-helicity flip. The functions are unpolarized and polarized (marked with ˜).

		nucleon helicity	
		conservation	flip
quark helicity	independent	$H^{q,g}$	$E^{q,g}$
	dependent	$\tilde{H}^{q,g}$	$\tilde{E}^{q,g}$

2.4.2 GPD and known Parton Distributions

In general, the momentum and the helicity of the nucleon can differ between the initial and the final state. In the infinite momentum frame where

$$t = 0 \quad \text{and} \quad \xi = 0, \tag{2.19}$$

the four-momentum and helicity remain identical and can be connected to the PDFs $q(x)$ and $\Delta q(x)$, as follows [16]:

$$\text{for } x > 0: \quad H^q(x,0,0) = q(x), \qquad \tilde{H}^q(x,0,0) = \Delta q(x) \tag{2.20}$$

$$H^g(x,0,0) = xg(x), \qquad \tilde{H}^g(x,0,0) = x\Delta g(x) \tag{2.21}$$

$$\text{for } x < 0: \quad H^q(x,0,0) = -\bar{q}(-x), \qquad \tilde{H}^q(x,0,0) = \Delta\bar{q}(-x). \tag{2.22}$$

In this case the GPD H^f and $\tilde{H}^f$ represent the unpolarized and the polarized distribution functions for quarks $(x > 0)$ and anti-quarks $(x < 0)$. In Fig. 2.5 the dependency

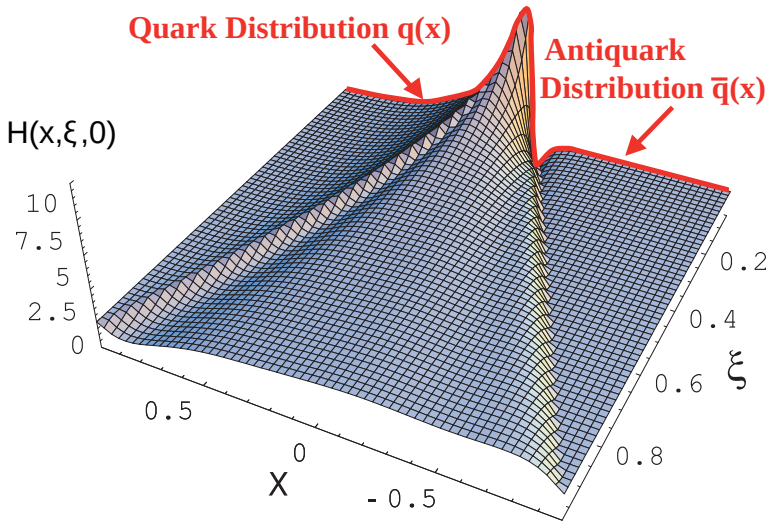


Figure 2.5: The x and ξ dependence of the GPD $H(x,\xi,t=0)$ for the u-quark distribution. The red line at $\xi = 0$ is corresponding to usual PDFs. The region $|x| > \xi$ can be accessed with the DVCS process [17].

on $H^u(x,\xi,t=0)$ on x and ξ is given. The red line is corresponding to the PDFs $q(x)$ for quark and anti-quark.

There is no comparable interpretation for the GPD E^f and $\tilde{E}^f$ describing the nucleon helicity flip. This can be explained with the fact, that due to the helicity flip, a finite momentum has to be transferred. Due to this the GPD E^f and $\tilde{E}^f$ cannot be interpreted with PDFs.

Another interpretation of the GPD can be found by calculating their first moments. They are directly connected to the elastic form factors of the nucleon [8]:

$$\int_{-1}^{1} dx H^q(x,\xi,t) = F_1^q(t) \tag{2.23}$$

$$\int_{-1}^{1} dx E^q(x,\xi,t) = F_2^q(t) \tag{2.24}$$

$$\int_{-1}^{1} dt \tilde{H}^q(x,\xi,t) = g_A^q(t) \tag{2.25}$$

$$\int_{-1}^{1} dt \tilde{E}^q(x,\xi,t) = h_A^q(t), \tag{2.26}$$

where $F_1^q(t)$, $F_2^q(t)$, $g_A^q(t)$ and $h_A^q(t)$ are the elastic Dirac, Pauli, axial and pseudoscalar form factors.
As with the usual PDFs, there are leading order corrections in α_s for the GPD which are depending on Q^2. For the elastic Dirac form factors, the Q^2 dependency disappears after calculating the first moments.

2.4.3 Phenomenological Interpretations of the GPD

The GPD give access to interesting phenomenological interpretations of the structure of the nucleon. A visualization of the proton in a tomographic way and a kind of "3 dimensional" visualization of the nucleon can be extracted from the GPD.
As tomography is in general defined as imaging of an object in different sections, this term is used to describe different images of the proton generated in dependency on the kinematic variable x. The images, themselves, can be built from impact parameter information described below.
In the limiting case $\xi = 0$, the parton carries identical longitudinal momentum fraction x in the initial and final states. Therefore, the momentum transfer $t = -\Delta^2 = -\Delta_L^2 - \Delta_\perp^2 = -\Delta_\perp^2$ is purely transverse.
A Fourier transformation of the GPD $H^f(x, 0, -\Delta_\perp^2)$ depending on $-\Delta_\perp^2$ gives a spatial distribution of different partons carrying the longitudinal momentum fraction x as a function of the transverse impact-parameter $\vec{b}_\perp$ [18]:

$$q^f(x, \vec{b}_\perp) = \int \frac{d^2\Delta_\perp^2}{(2\pi)^2} e^{-i\Delta_\perp \vec{b}_\perp} H^f(x, 0, -\Delta_\perp^2). \tag{2.27}$$

In Fig. 2.6 a sketch of the impact-parameter representation for different values of $x < 0.1$, $x \approx 0.3$ and $x \approx 0.8$ is given. This visualization of the impact parameter dependent parton distribution $q^f(x, \vec{b}_\perp)$ can be interpreted as a set of "tomographic images" for different values of x.

The impact parameter $b_\perp$ is defined as the distance to the center of momentum of the nucleon which can be described by the sum over the transverse positions $\vec{r}_{\perp,i}$ of all partons weighted with the corresponding momentum fractions [20]:

$$\vec{R}_\perp = \sum_{i=q,g} x_i \vec{r}_{\perp,i}. \tag{2.28}$$

With $x \to 1$ the active quark is mainly defining the center of momentum and the distribution $q(x, \vec{b_\perp}) = \Sigma q^f(x, \vec{b}_\perp)$ tends to zero (see Fig. 2.7).
The Fourier transform of GPD for $x = \xi$ gives access to the distance $r_\perp$ [21]. Averaging over distances between the struck quark and the spectator system $< r_\perp^2(x) >$ can be set in relation to the t-slope parameter $B(x_{Bj})$ at small x_{Bj}. In this region the overall transverse size of the nucleon can be written as:

$$< r_\perp^2(x) > \approx 2 \cdot B(x_{Bj}). \tag{2.29}$$

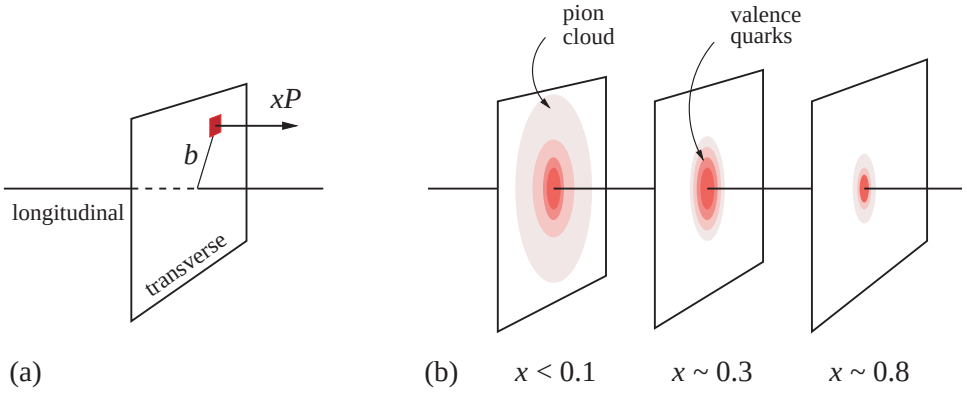


Figure 2.6: Nucleon Tomography: (a) The distribution of the transverse distance b from the center of momentum of the nucleon of partons which are carrying the fraction x of the longitudinal momentum of the nucleon. (b) Tomographic views of the nucleon at three values of x. $x < 0.1$: In the low x range the distribution is dominated by sea quarks and gluons. $x \approx 0.3$: In this x region a core built from the valence quarks is prominent. $x \approx 0.8$: For large values of x the size of the nucleon is mainly described from the active parton which is the center of momentum of the nucleon [19].

Measurements of the t-slope parameter can, therefore, help to understand the dependency on the transverse size of the nucleon on the momentum fraction carried by the scattered parton. The characteristic t-slope can be determined with the ansatz

$$\frac{d\sigma}{dt} \propto (exp(-B(x_{Bj}) \cdot |t|), \tag{2.30}$$

where the parameter $B(x_{Bj})$ is written as

$$B(x_{Bj}) = B_0 + 2\alpha' log(\frac{x_0}{x_{Bj}}) \tag{2.31}$$

and α' is the parameter for the increase of the nucleon size with decreasing x_{Bj}. To obtain $B(x_{Bj})$, a ϕ-integrated beam charge and spin sum (see (2.39)) of DVCS cross section has to be measured after subtracting the BH events. As experimental data for $B(x_{Bj})$ only exists for small x_{Bj}, the COMPASS-II experiment will measure the t-slope parameter in regions with $x_{Bj} > 10^{-2}$. The expected statistical errors for these measurements are given in Fig. 2.8.

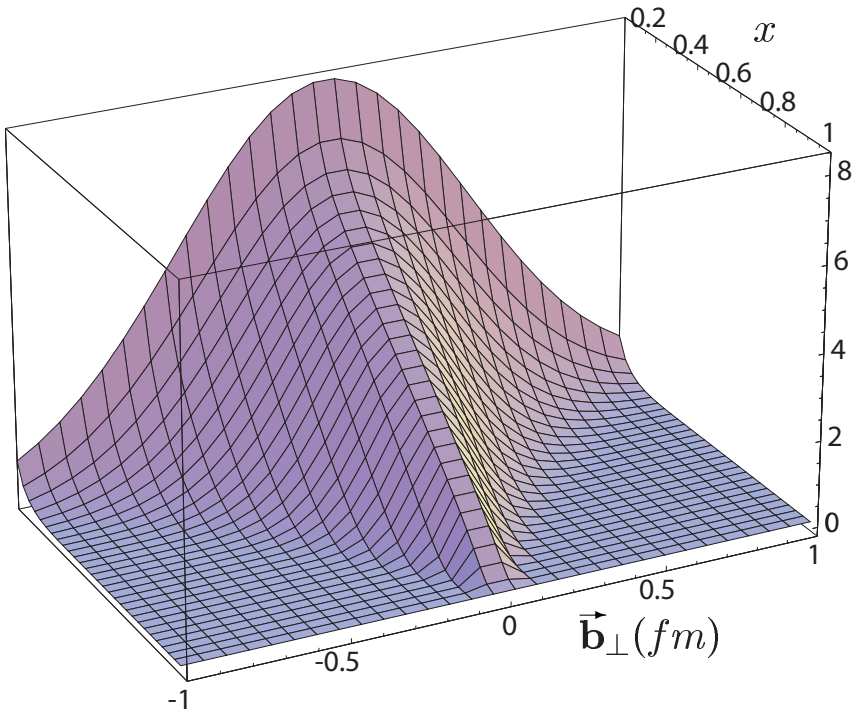


Figure 2.7: Qualitative distribution of $q(x, \vec{b_\perp})$ [17].

2.5 Deeply Virtual Compton Scattering

The gateway to GPD is the Deeply Virtual Compton Scattering (DVCS):

$$l + N \rightarrow l' + N' + \gamma. \tag{2.32}$$

Here the lepton probe scatters off a nucleon with the exchange of a virtual photon and a real photon is emitted. The nucleon remains intact. This process is well understood from the theoretical point of view.
However, there is a competing process with the same final state as the DVCS process, namely the Bethe-Heidler (BH) process. This process is well known and can be described and calculated in QED. To clarify the difference the Feynman diagrams of the DVCS and the two variants of the BH processes are plotted in Fig. 2.9. The diagram (a) represents the DVCS process with a lepton is scattering off a nucleon. Thereby one quark from the nucleon (gray bulb) with a longitudinal momentum fraction $x + \xi$ is absorbing a virtual photon with Q^2. A real photon is emitted and the longitudinal momentum fraction of the quark is therewith reduced to $x - \xi$. The diagrams (b) and (c) in Fig. 2.9 show two possible BH processes, where an incoming or outgoing lepton is emitting a real photon due to bremsstrahlung.

The DVCS and BH processes interfere at amplitude level. The cross section of the processes detecting a real photon and an exclusive muon scattered at an unpolarized proton target can, therefore, be written as [26]:

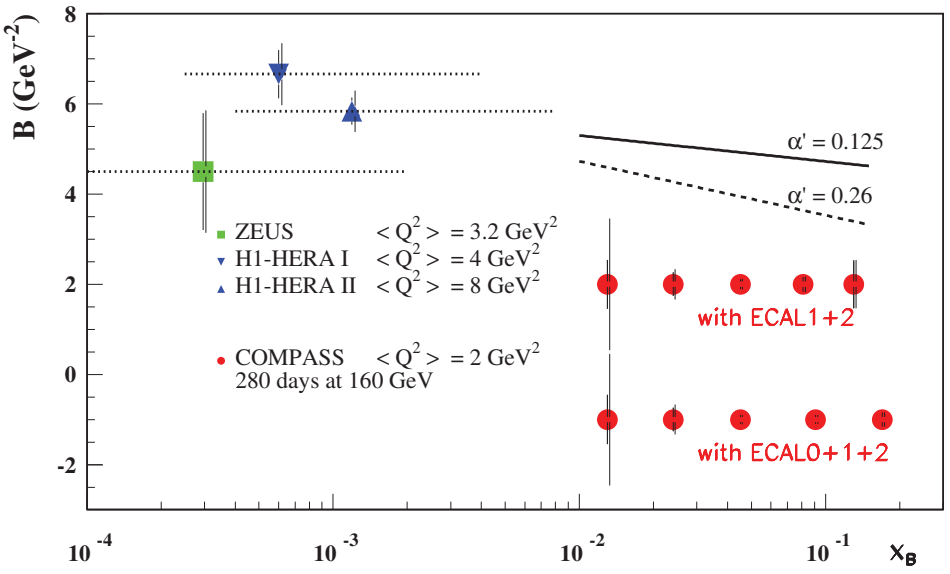


Figure 2.8: Projections for the x_{Bj} dependence of the t-slope parameter $B(x_{Bj})$. The calculations are done for the region $1 < Q^2 < 8\,\mathrm{GeV}^2$ [22, 23, 24]. The dashed lines represent the corresponding x_{Bj} range of the experiment. For the predictions two different values of $\alpha' = 0.125\,\mathrm{GeV}^{-2}$ and $\alpha' = 0.260\,\mathrm{GeV}^{-2}$ were chosen. The expected values for B are given for simulations with and without ECAL0. For each of the red data point, the left vertical bar represents the statistical error only and the right one also includes the added quadratic systematic uncertainty.

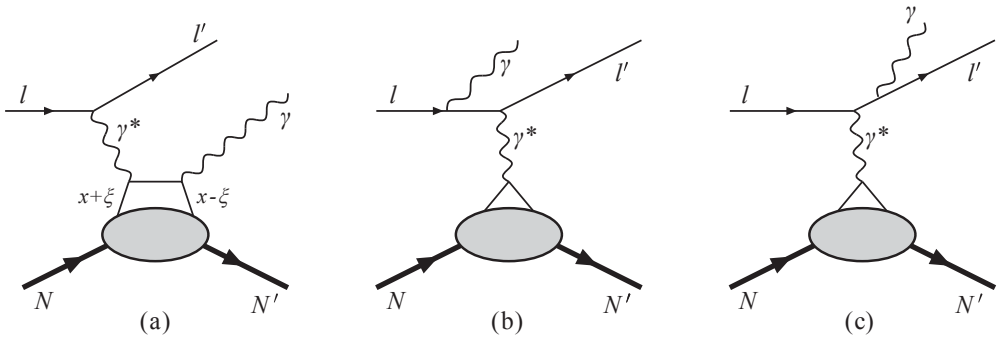


Figure 2.9: Leading order processes for lepto production of real photons. (a) DVCS, (b) and (c) Bethe-Heidler process [25].

$$\frac{d\sigma(lN \to lN\gamma)}{dx\ dQ^2\ d|t|\ d\phi} \propto |\tau_{\mathrm{BH}}|^2 + |\tau_{\mathrm{DVCS}}|^2 + \underbrace{\tau_{\mathrm{DVCS}}\tau^*_{\mathrm{BH}} + \tau_{\mathrm{BH}}\tau^*_{\mathrm{DVCS}}}_{I}, \tag{2.33}$$

where ϕ is the azimuthal angle between lepton scattering plane and the $p\gamma$-plane and τ denotes the amplitude of the corresponding process. The analysis of this angular distribution provides information about the $\tau_{\mathrm{DVCS}}/\tau_{\mathrm{BH}}$ dependency on the DVCS cross section.
There are different conditions where the BH or the DVCS process is dominating depending on the x_{Bj} and the Q^2 region. For small x_{Bj}, the DVCS process is suppressed, but for increasing x_{Bj} the amplitudes of both processes are expected to be of the same order of magnitude. When reaching $x_{Bj} > 0.03$ the DVCS process is expected to dominate (see Fig. 2.10). In this case the cross section for the exclusive final state will be mainly contributed by the DVCS amplitude in leading order [27]:

$$\tau_{\mathrm{DVCS}} \sim \int_{-1}^{1} \frac{H(x,\xi,t)}{x - \xi + i\epsilon}\, dx. \tag{2.34}$$

In Fig. 2.10 a Monte Carlo prediction for DVCS and BH event yield as function of ϕ at different values of x_{Bj} is shown. The remarkable difference in the cross sections of both processes can be seen in for $x_{Bj} > 0.03$.

2.5.1 Beam Charge Asymmetries

Beside the separation of the DVCS events from the BH processes by pointing on the different x_{Bj} regions, the second way to access DVCS processes is the measurement of the beam charge asymmetry (BCA). In both processes hard exclusive muon production occurs and for the cross section it can be found [5]:

$$\frac{d\sigma(\mu N \to \mu N\gamma)}{dx_{Bj}\ dQ^2\ d|t|\ d\phi} = d\sigma_{BH} + (d\sigma_{DVCS,unpol} + P_\mu\ d\sigma_{DVCS,pol}) + e_\mu\,(\Re I + P_\mu\ \Im I)\,, \tag{2.35}$$

where e_μ is the charge in units of the elementary charge of the polarised muon beam and P_μ its polarization. Due to the interference of the DVCS and BH amplitude the interference term I contributes to this cross section. With the fact that the BH contribution to the cross section is purely real, the difference of the cross sections for leptonic probes of different charges can be written as[1]:

$$\sigma(l^+) - \sigma(l^-) \propto \tau_{\mathrm{BH}} \cdot Re(\tau_{\mathrm{DVCS}}). \tag{2.36}$$

Whereas the sign of the DVCS amplitude is changing in dependency on the beam charge, the BH contribution is not affected. With the knowledge of the BH amplitude, which depends on nucleon form factors, a relation between the real part of the DVCS

[1] in the following σ replaces $\frac{d\sigma(\mu p \to \mu p\gamma)}{dx_{Bj}\ dQ^2\ d|t|\ d\phi}$

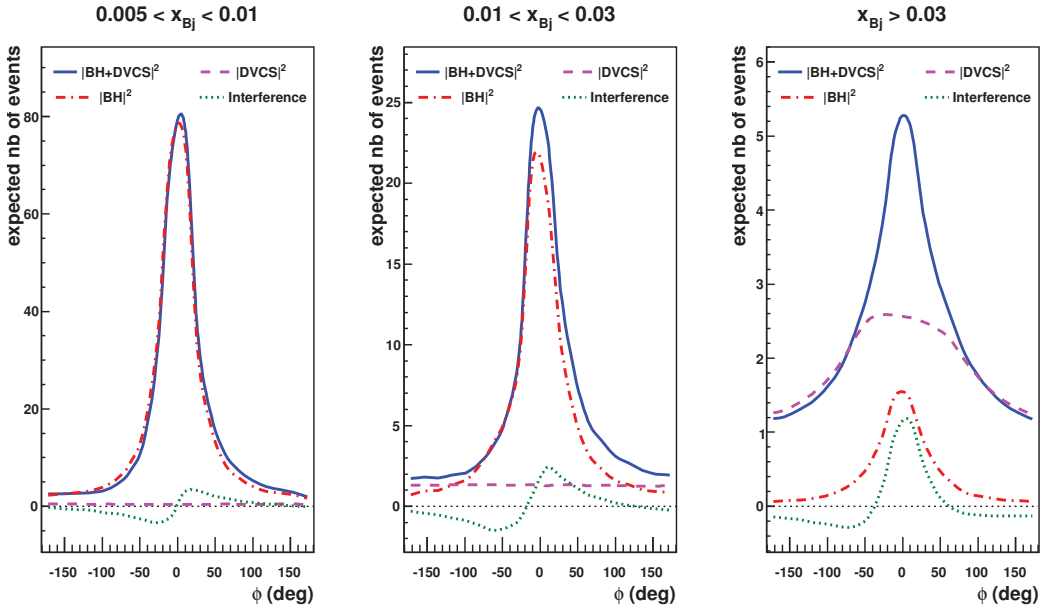


Figure 2.10: Monte Carlo simulation for $\mu p \to \mu p \gamma$ in dependency on the angle between lepton scattering plane and the $p\gamma$-plane. A comparison between BH (dot-dashed), DVCS (dashed) and total cross section is given for different values of x_{Bj} [5].

amplitude and the difference of the cross sections can be measured. For an unpolarized target the DVCS amplitude can be written as:

$$\tau_{\mathrm{DVCS}} \propto \left[F_1\mathcal{H} + \xi(F_1+F_2)\tilde{\mathcal{H}} - \frac{t}{4m^2}F_2\mathcal{E} \right], \tag{2.37}$$

where F_1 and F_2 are the elastic Dirac- and Pauli form factors, m is the nucleon mass and $\mathcal{H}$, $\tilde{\mathcal{H}}$, $\mathcal{E}$ are the Compton form factors (CFF). A CFF is a sum over quark flavors f of convolutions of respective GPD with functions describing the hard Compton scattering $\gamma^* q$.

The COMPASS-II experiment provides muon beams of different charges. Therewith, the naturally polarization of the beam is generated due to the parity violating pion decay. Hence, a change of charge is also affecting the polarization of the beam. In this case the sum $\mathcal{S}$ and the difference $\mathcal{D}$ of the polarized cross sections off an unpolarized target can be written as:

$$\mathcal{S} = \sigma^{l^+\leftarrow} + \sigma^{l^-\rightarrow} \propto Im(F_1\mathcal{H})\sin(\phi) \tag{2.38}$$

$$\mathcal{D} = \sigma^{l^+\leftarrow} - \sigma^{l^-\rightarrow} \propto Re(F_1\mathcal{H})\cos(\phi), \tag{2.39}$$

The sum $\mathcal{S}$ is connected to the imaginary part of $\mathcal{H}$ and provides a direct access to the GPD H. As mentioned in section 2.4.3 the knowledge of this GPD leads to information about the impact parameter dependent parton distribution. The analysis of the difference $\mathcal{D}$ provides access to the real part of the CCF $\mathcal{H}$ which can be used to describe the transverse distribution of the nucleon for the complete x range.
With the expressions for the sum $\mathcal{S}$ and the difference $\mathcal{D}$ of the polarized cross sections the Beam Charge and Spin Asymmetry can be defined:

$$\mathcal{A} = \frac{\sigma^{l^+\leftarrow} - \sigma^{l^-\rightarrow}}{\sigma^{l^+\leftarrow} + \sigma^{l^-\rightarrow}} = \frac{\mathcal{D}}{\mathcal{S}} \tag{2.40}$$

As mentioned above, the study of the BCA in dependency on the azimuthal angular distribution of ϕ can be used to determine different quark GPD. The accuracy of the possible measured Beam Charge and Spin Difference $\mathcal{D}$ at COMPASS-II is predicted in Fig. 2.12. Here, the expected azimuthal distribution of $\mathcal{D}$ and its statistical and systematic accuracy for $1 \leq Q^2 \leq 4\,\mathrm{GeV/c^2}$ and $0.03 \leq x_{Bj} \leq 0.007$ are given. Fig. 2.11 provides the expected statistical accuracies for the measurement of the Beam Charge and Spin Asymmetries $\mathcal{A}$. The measurement of the asymmetries is predicted to be easier compared to the difference as certain systematic change and it is more insensitive to theoretical corrections [5]. The projected statistical accuracy for the measurement of $\mathcal{A}$ is given in Fig. 2.13 for six different x_{Bj} bins.

Test measurements were performed in 2008 and 2009 at the COMPASS facility to proof the capability of the spectrometer to identify exclusive single photon events. For these tests the experimental setup was similar to the one used for the hadron spectroscopy

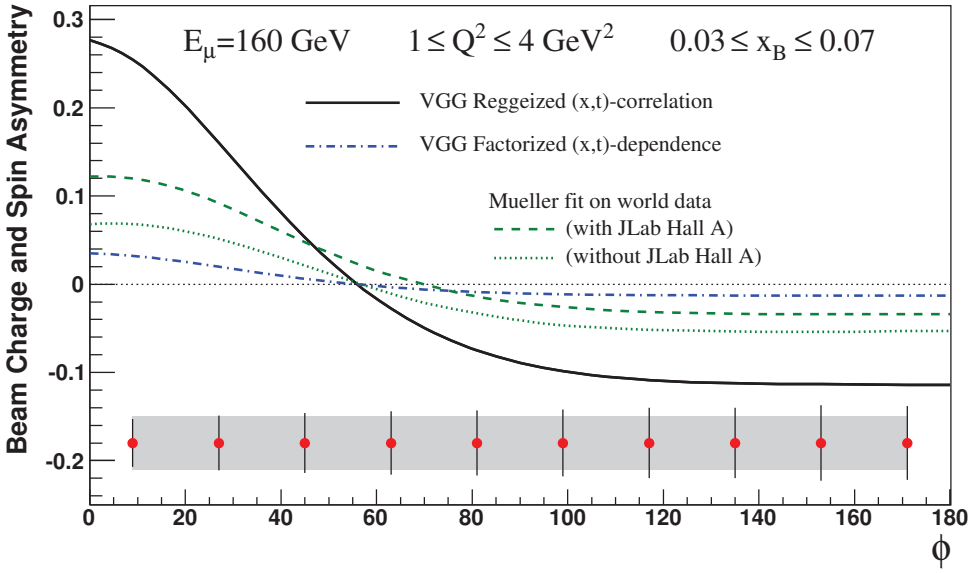


Figure 2.11: Azimuthal distribution of the Beam Charge and Spin Asymmetry at beam energy of $E_\mu = 160\,\text{GeV}$. There are two distributions plotted using the VGG modes (black solid and dashed lines) and a fit on world data (green dashed line: JLab Hall A data included, green dotted line: JLab Hall A data excluded) [28, 29, 30].

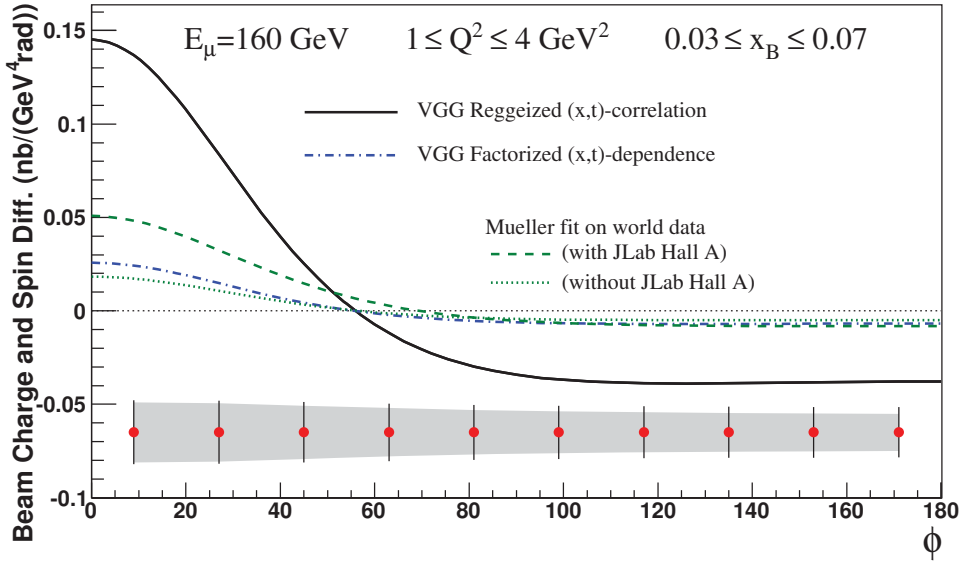


Figure 2.12: Azimuthal distribution of the Beam Charge and Spin Difference at beam energy of $E_\mu = 160\,\text{GeV}$ (detailed description in caption of Fig. 2.11).

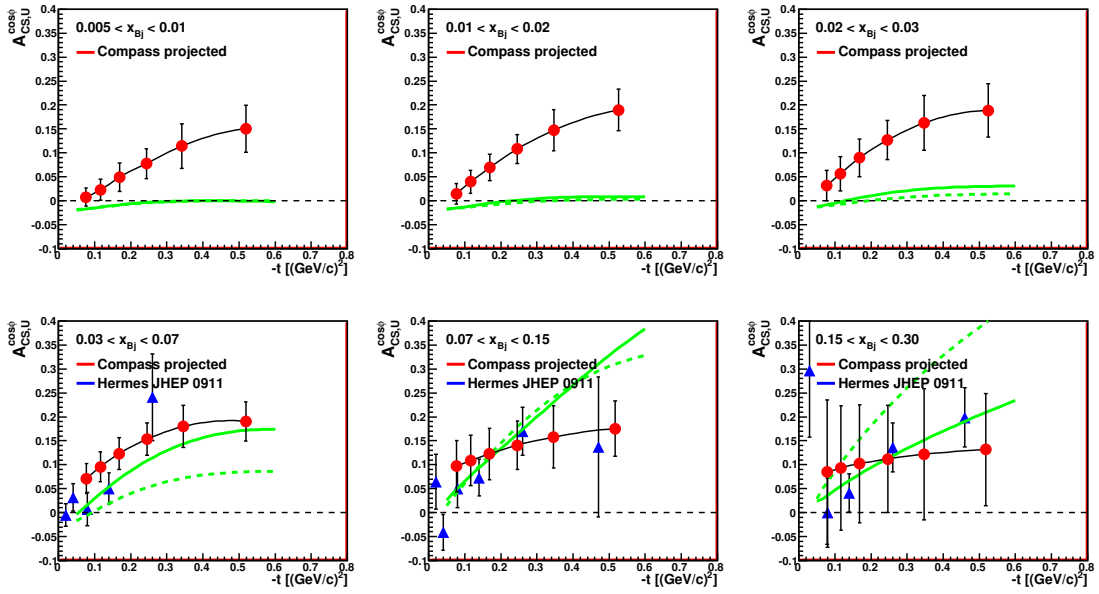


Figure 2.13: Projections for Beam Charge and Spin Asymmetry for six different x_{Bj} bins. The red dots denote the amplitude predictions for the COMPASS experiment. For a comparison the recent HERMES results (blue triangles) and first fits on world data (green solid line; green dashed line: excluding JLab Hall A) [29, 31].

experiments at COMPASS. This includes a short recoil proton detector (RPD) of 2.0 m length surrounding a 40.0 cm long liquid hydrogen target. For the measurements μ^+ and μ^- beams of 160.0 GeV energy were used.

First results from the test run in 2008 with a μ^+ beam are given in Fig. 2.14. The data is plotted in three different x_{Bj} bins. Dominated by the BH processes is the low x_{Bj} region (left plot), where 278 events with an exclusive single photon and proton in the final state have been found in the analysis. In the high x_{Bj} region (right plot) where DVCS dominates 54 events could be selected (continuous and dashed line in Fig. 2.14) are plotted. These results are comparable with the simulations as given in Fig. 2.10.

For the planned measurements at the COMPASS-II experiment, an extended liquid hydrogen target will be used with a new recoil proton detector surrounding this target (see section 3.3.2). The simulations performed in advance predict that a high precision measurement with the COMPASS-II spectrometer is needed to obtain the expected statistics of DVCS events in a beam period of 280 days (70 days with μ^+ and 210 days with μ^- beam). Depending on the binning of x_{Bj}, some hundreds of DVCS events are expected over the same number of BH events in the high x_{Bj} region.

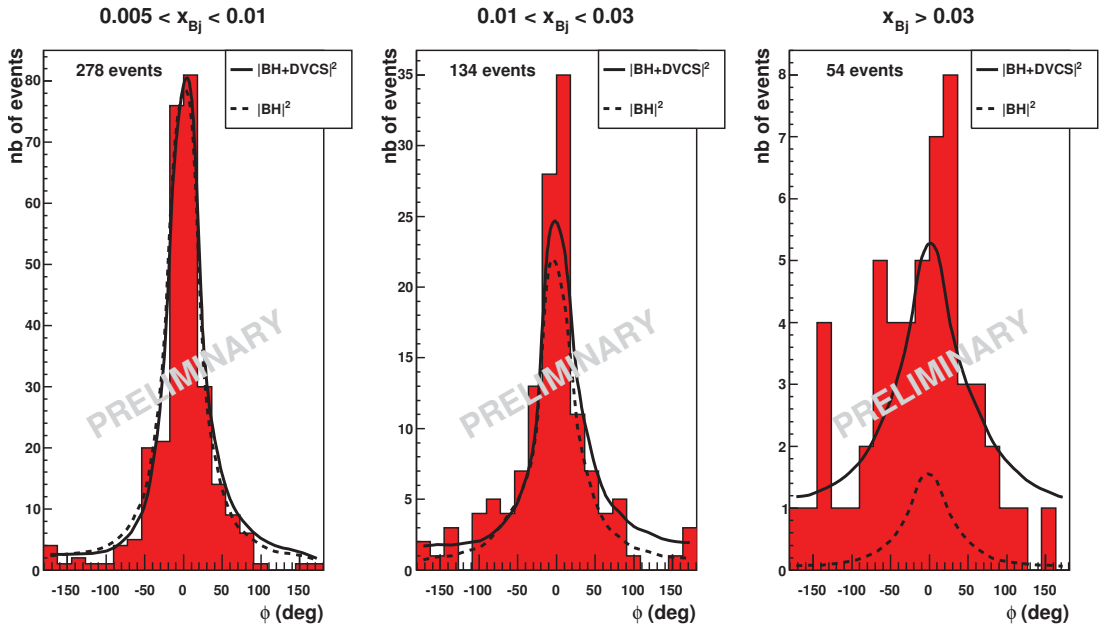


Figure 2.14: Measured azimuthal distribution for angle ϕ in exclusive single-photon events. The black line is representing Monte Carlo simulation of BH and DVCS events, the dashed line is describing the simulation results for BH events only [5].

3. The COMPASS-II Experiment

The COMPASS experiment located in the North Area of the CERN accelerator facility (see Fig. 3.1) consists of a highly flexible spectrometer which can easily be adapted to different requirements for a variety of hadron structure and spectroscopy studies (see Fig. 3.3, [32]). In the past years successful measurements on exotic spin quantum states of matter and on the helicity and transverse spin structure of protons and neutrons were performed. Today strong efforts on spectrometer and target upgrades are in progress as outlined in the COMPASS-II proposal for future studies, like the measurements of the Generalized Parton Distribution Functions, introduced in the preceding chapter [5]. In the following sections an overview of important parts of the existing spectrometer will be given and essential upgrades for GPD measurements will be outlined.

3.1 The Beam

The COMPASS facility has the capability to make use of different beam configurations for fixed target physics programs. The beam is provided by the SPS[1], accelerating protons to energies up to 450 GeV. To select between different beam types like muon or hadron beam, an exchangeable primary target (T6) and mechanical filters can be moved into beam line M2 (see Fig. 3.1).

For measurements of the DVCS amplitude with an unpolarized liquid hydrogen target highly polarized μ^+ and μ^- beams are needed. The muons originate from weak decays of kaons and pions. They are produced by reactions of the accelerated protons from the SPS with the nucleons inside the 60 cm primary beryllium target. After the pion production at T6, the decay process takes place in a 600 m long decay tunnel leading to the entrance of the experiment hall. The polarization of the muons is generated naturally due to the parity violating processes: $K^+ \rightarrow \mu^+ + \nu_\mu$ and $\pi^+ \rightarrow \mu^+ + \nu_\mu$ or charge conjugated respectively. The beam is injected into the COMPASS facility with a spill structure. Depending on the number of other experiments served by the SPS a spill, composed of an on-spill and off-spill phase, can least up to 50 s. During the 10 s long on-spill phase $2 \cdot 10^8$ muons are injected into the experiment.

Due to the production of muons from particle decay in flight, the beam has a momentum distribution of about 5%. As the precise knowledge of the momenta is important for the determination of the μ polarization, a measurement of the momentum of any beam particle is mandatory. At the end of the beam line the beam momentum station (BMS) can determine the momentum by calculating the radius of the beam tracks where the beam is deflected to enter the COMPASS facility using the bending magnet B6 (see Fig. 3.2).

[1] Super Proton Synchroton

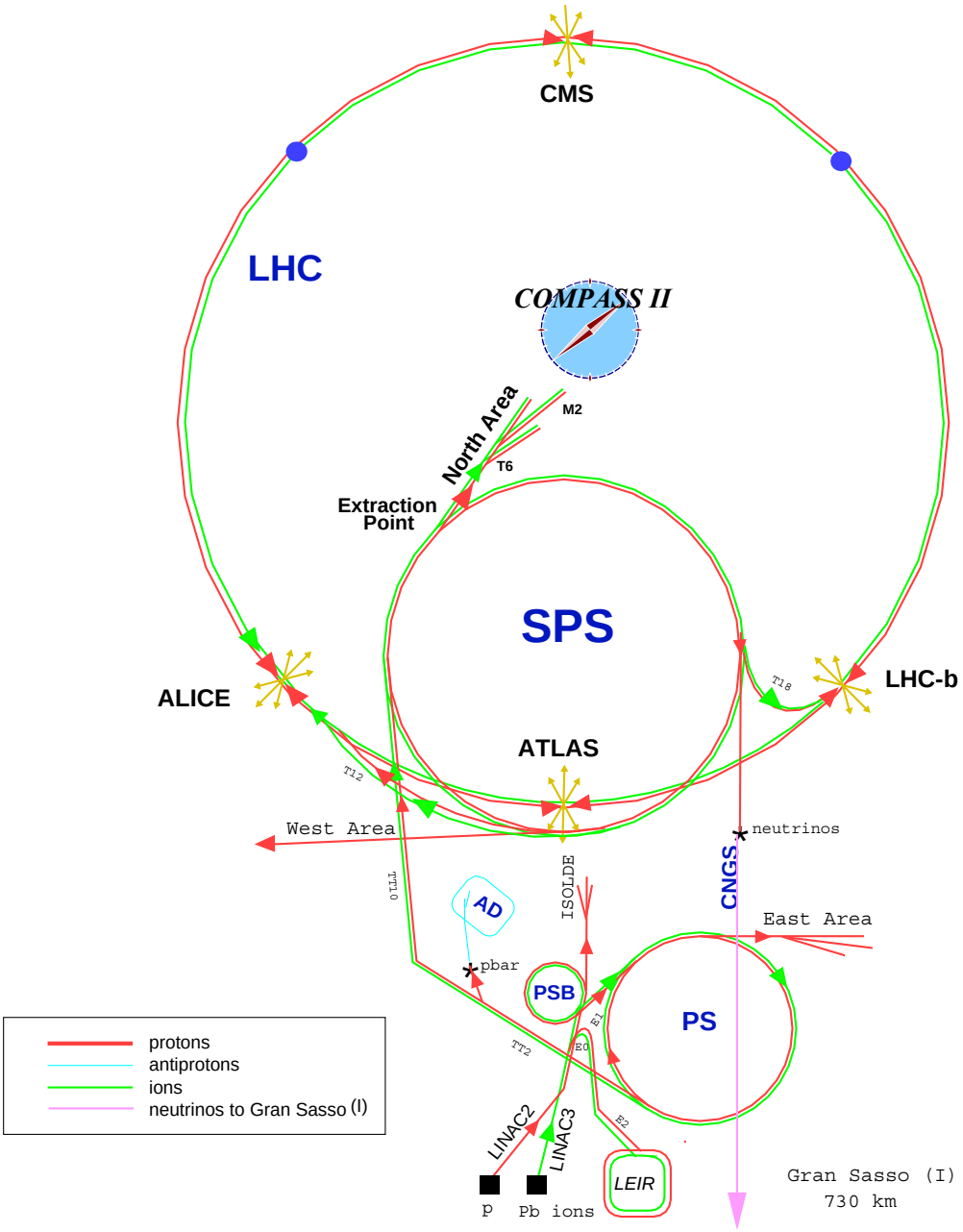


Figure 3.1: Schematic overview of the CERN accelerators. The COMPASS-II experiment is located in the North Area of the CERN facilities and is there connected to the M2 beamline.

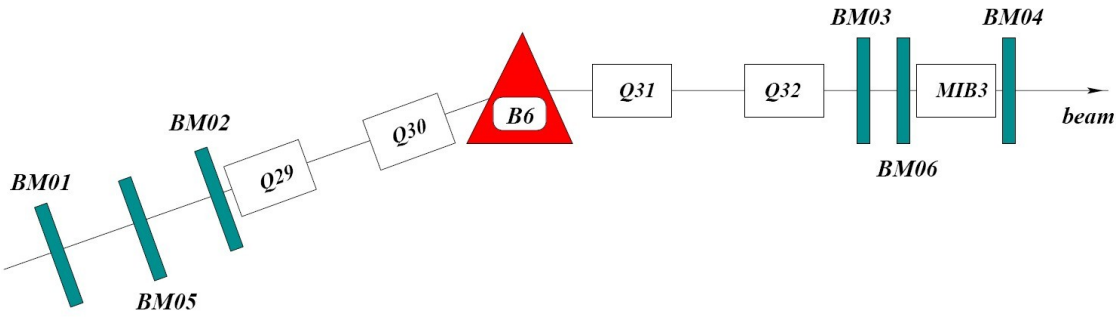


Figure 3.2: Schematic overview of the final beam section including Beam Momentum Station and bending magnet B6.

In order to study the asymmetry of the DVCS amplitude, measurements with μ^- beam at one third of the beam intensity of the μ^+ beam will be performed. This relation can be derived from the production of the muons by protons. A very precise measurement of the μ^+ and μ^- beam flux on percent level must be guaranteed. This is accomplished by using scintillating fiber detectors in front of the liquid hydrogen target. In the following sections the detectors which are necessary for the measurement of GPD, will be highlighted.

3.2 The Liquid Hydrogen Target

For the GPD physics program, a long liquid hydrogen target surrounded by a recoil proton detector (RPD) is needed in order to study the exclusive reactions $\mu p \to \mu p \gamma$ (see Fig. 3.3). As the luminosity depends on the length of the liquid hydrogen target as well as the beam intensity, a 2.5 m target is foreseen to provide a focused luminosity of $10^{32}\,\mathrm{cm}^{-2}\mathrm{s}^{-1}$ for the μ^+ beam. An accurate knowledge of the target density and precise measurements of the beam flux with 1% accuracy is important for a good quantification of the luminosity.

Due to the transverse size of the μ^+ and μ^- beam the diameter of the liquid hydrogen target must be at least 40 mm. The development of such a target with a minimum gas-phase volume and a homogeneous hydrogen density over the length of 2.5 m will be a challenge. The thickness of the Mylar surrounding the target and the aluminum material of the cryostat tube must be minimized (125 μm for the Mylar and 1.8 mm for the aluminium shield) to reach a lowest possible momentum of 260 MeV/c for recoiled protons under an angle of 90°.

In a subsequent phase of the DVCS program the measurements of the transverse target spin asymmetries for protons are planned. Therefore an upgrade to a polarized target surrounded by a recoil proton detector is foreseen.

3.3 The Spectrometer

3.3.1 Tracking Detectors

The COMPASS-II spectrometer consists of a large variety of tracking detectors and detectors for particle identification. With the use of dipole magnets, the momentum of

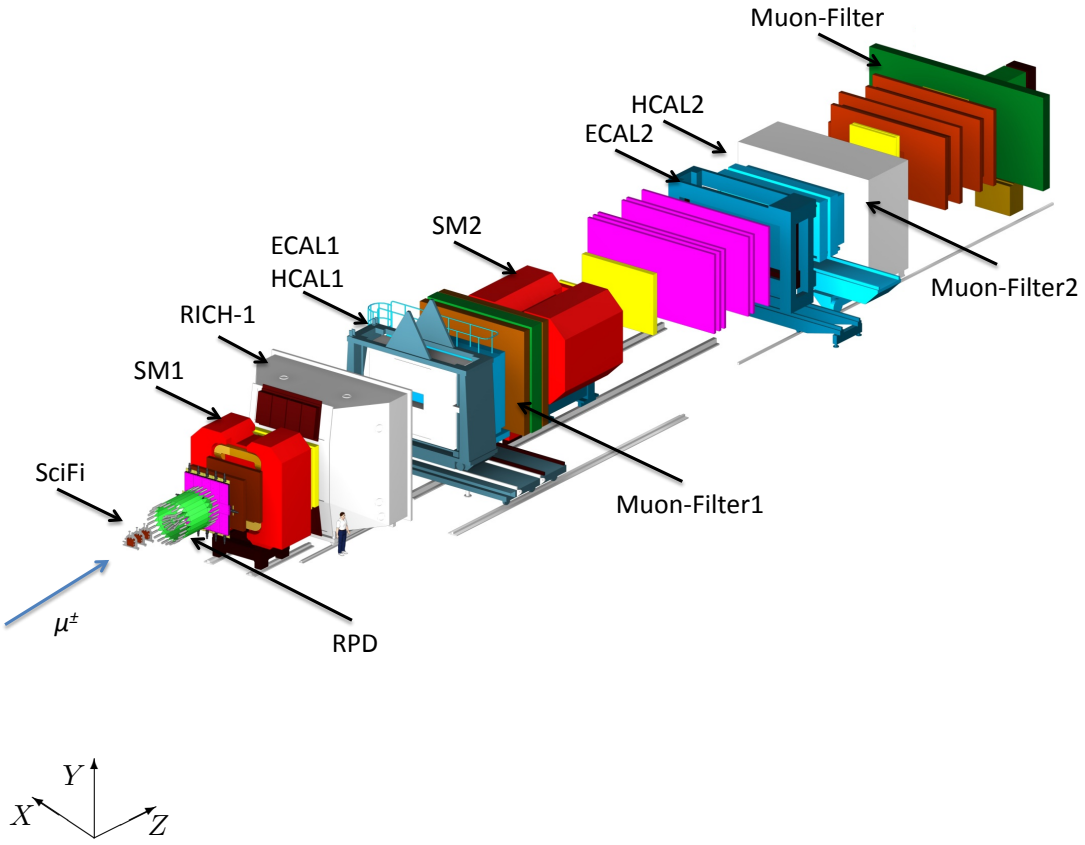


Figure 3.3: Artistic view of the 60 m long COMPASS two-stage spectrometer [33]. This sketch shows the setup used in 2009 with a RPD for DVCS test measurements. In future the small recoil proton detector (RPD) used in 2009 will be replaced by the CAMERA detector described in section 3.3.2. The different tracking detectors installed along the 50 m long two stage spectrometer are also identified.

the particles can be identified with the tracking detectors. The detectors spatial and time resolution and its capable rate are optimized depending on the distance from the target for excellent momentum resolution in the range from 1 GeV/c up to 200 GeV/c. The spectrometer is separated into two stages with two dipole magnets covering detectors with dedicated characteristics: the *large angle spectrometer* (LAS) and the *small angle spectrometer* (SAS). The tracking stations are composed of detectors like MicroMegas[2], drift chambers, GEM[3], MWPC[4], DC[5] and straw detectors (see Fig. 3.3).

[2]Micro MEsh Gaseous Structure
[3]Gas Electron Multiplier
[4]Multi Wire Proportional Chambers
[5]Drift Chambers

The LAS is able to detect particles with a small momentum or a deflection under large angles. This part includes the SM1 dipole magnet and has an angular acceptance of θ_x, $\theta_y = \pm 180\,\text{mrad}$, where θ_x and θ_y are horizontal and vertical polar angle components. The SAS covers the second dipole magnet SM2 and can detect high momentum particles with an angular distribution of θ_x, $\theta_y = 30\,\text{mrad}$. A detailed description of all different detector types can be found in [32].

3.3.2 Particle Identification Detectors

The RICH-1 Detector

For SIDIS[6] as well as DVMP[7] measurements, particle identification with the spectrometer is mandatory. With DVMP the GPD H can be studied in measuring cross sections for different mesons e.g. the ϕ meson [34].

The particle identification of hadrons in the LAS is performed with a Ring Imaging Cherenkov detector. When particles pass through a dielectric medium with a velocity greater than the phase velocity of light in that medium, Cherenkov light is emitted under a certain angle ϕ_c relative to the propagation direction of the particle. Therefore the velocity of such particles can be determined by measuring the angle ϕ_c.

$$\cos\phi_c = \frac{1}{n\beta} = \frac{1}{n}\frac{1}{\sqrt{1+m^2/p^2}}. \tag{3.1}$$

Together with the measurement of the particle momenta, the calculation of the mass of the particles and, therefore, particle identification is possible with (3.1). The radiator used with the RICH-1 is C_4F_{10} gas with a refractive index of $n = 1.0015$ ($T = 25\,^\circ\text{C}$, $P = 10\,\text{Pa}$). Momenta thresholds p_{th} for the different hadrons can be estimated from (3.1) for $\cos\phi_c = 1$:

$$p_{th} = \frac{m}{\sqrt{n^2-1}} \tag{3.2}$$

Therefore, the RICH-1 detector can separate pions, kaons and protons with momenta from $2.4\,\text{GeV/c}$ to $50\,\text{GeV/c}$ [35]. The emitted Cherenkov photons are reflected by spheric mirrors and then detected in the outer region of the detector by Multi Wire Proportional Chambers (MWPC) equipped with solid state CsI coated photo-cathodes. In the inner region, where charged track occupancy is high, the photo-conversion is performed by fast multi-anode photomultiplier Tubes. The angular resolution for Cherenkov ring measurement for the inner region is 0.3 mrad and 1.6 mrad for the outer region [36].

In conjunction with the upgrades for the GPD physics program at the COMPASS-II experiment the outer region of the RICH-1 photo-conversion detectors will be upgraded. Due to fatigue and aging of the CsI photo-cathodes resulting in a reduction of the quantum efficiency and long recovering time of the MWPC after a detector discharge, a

[6] Semi Inclusive Deep Inelastic Scattering
[7] Deeply Virtual Meson Production

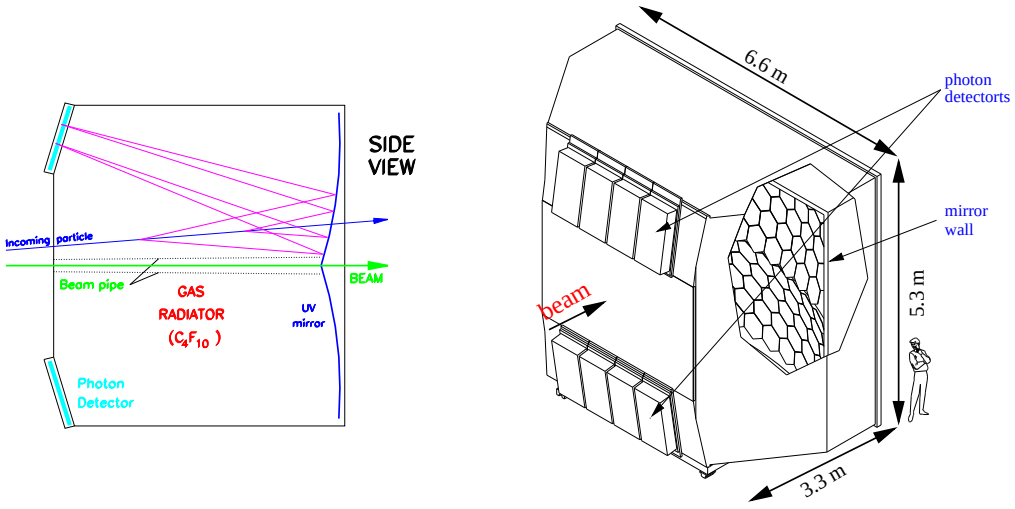


Figure 3.4: Schematic overview of the RICH-1 detector [37]. The left figure shows the geometric principle of the Cherenkov photon detection. The right sketch gives an overview of the RICH-1 detector dimensions.

replacement by THGEM[8] based photon detectors together with solid state *CsI* photocathodes is in progress [38].

Muon Filters

For exclusive DVCS measurements the detection of the scattered muon passing the spectrometer is mandatory. To separate muons from other particles, large massive muon filters are installed at the end of the LAS and the SAS built from iron or concrete (*Muon Filter 1*, *Muon Filter 2* in Fig. 3.3). These filters absorb all particles except the weak interacting muons e.g. high energetic pions. A hole is placed in *Muon Filter 1* to allow particles entering the SAS. In front of and behind the filters, large hodoscopes consisting of plastic scintillation slats are installed to identify passing muons.

Electromagnetic and Hadronic Calorimeters

For exclusive DVCS process measurements, photons will be detected in the planned COMPASS-II spectrometer with three electromagnetic calorimeters. There are already ECAL1 and ECAL2 as parts of the LAS and SAS of the COMPASS spectrometer (see Fig. 3.3). An additional ECAL0 located between the target and the SM1 dipole magnet will cover a larger photon detection angle and optimize the hermeticity needed for the exclusive measurement of DVCS events. The existing electromagnetic calorimeters detect photons with energies larger than 100 MeV. The detector units consist of homogeneous lead glass where photons are producing secondary electromagnetic showers due to pair production. The induced Cherenkov light of these showers defines the energy deposition of the initial photons. The lead glass blocks have a depth of 16 radiation lengths, being able to detect 99% of the particle energy.

[8] THick GEM

The hadronic calorimeters HCAL1 and HCAL2 are sampling calorimeters built from detector units in a *sandwich* design. These calorimeter units are composed of alternating layers of iron and plastic scintillator material. Hadrons, passing the iron parts of the calorimeter, generate hadronic showers which can be identified in the subsequent scintillating material. In the spectrometer setup, the electromagnetic calorimeters are located in front of the hadronic calorimeters due to the better resolution $\sigma_{HCAL}/\sqrt{E} >> \sigma_{ECAL}/\sqrt{E}$ of the hadronic calorimeters.

Recoil Proton Detector

Recoiled protons from the liquid hydrogen target need to be positively identified for exclusive DVCS process detection. Therefore, a two barrel recoil proton detector (RPD) is planned within the COMPASS-II upgrade to surround the target. It has to cover the target in full length and its dimension has to take into account the expected angular distribution of the recoiled protons. The thickness of the scintillating material has to be chosen carefully to permit energy deposition and time-of-flight measurements of the recoiled particles at the same time. Hence, the inner one of the two barrels consists of scintillating material with a small thickness compared to the outer barrel.

The design of the CAMERA detector consists of two concentric barrels built from 24 scintillating slats each (see Fig. 3.5). The inner barrel is called *Ring A* and is composed of BC408 scintillator slats with a dimension of $275 \,\mathrm{x}\, 6.3 \,\mathrm{x}\, 0.4\,\mathrm{cm}^3$ each. The outer barrel (*Ring B*) consists of BC408 scintillator slats which measure $360 \,\mathrm{x}\, 30 \,\mathrm{x}\, 5\,\mathrm{cm}^3$. The distance from the slats in *Ring A* to the center of the target is 24 cm, while the slats from *Ring B* have a distance of 110 cm.
As each slat from *Ring A* or *B* is covering an azimuthal angle of 15°, the barrels are rotated by an angle of 7.5° to each other allowing for an appropriate azimuthal angular resolution of the detector.

The slats will be equipped from both sides with photo multiplier tubes. This summarizes a total number of 96 detector channels. The smaller slats in *Ring A* will be read by *ET9813* photomultipliers with 2 inches diameter end-windows [39]. For the *Ring B* slats *ET9823* photomultiplier tubes with 5 inch diameter end-windows will be used [40]. Simulations were performed to determine the range of the expected time-of-flight for different momenta of the recoiled protons. The time distance of hits in *Ring A* and *Ring B* are in an expected range of 3.0 to 60.0 ns for the dimensions of this detector. The simulations have also shown that a time resolution of the detector of $\sigma_t \approx 200$ ps is mandatory for the separation of protons from pions and background. Combined with additional COMPASS-II spectrometer data and the physical information obtained from this detector, a trigger signal on interesting events can be generated (see section 3.4.2).

3.4 COMPASS-II Trigger System

3.4.1 The Muon Trigger

A trigger on the muon passing the COMPASS-II spectrometer is mandatory for the exclusive measurement of DVCS events. This trigger must be able to discriminate scattered muons which are covering a large range in Q^2 and x_B and are scattered under

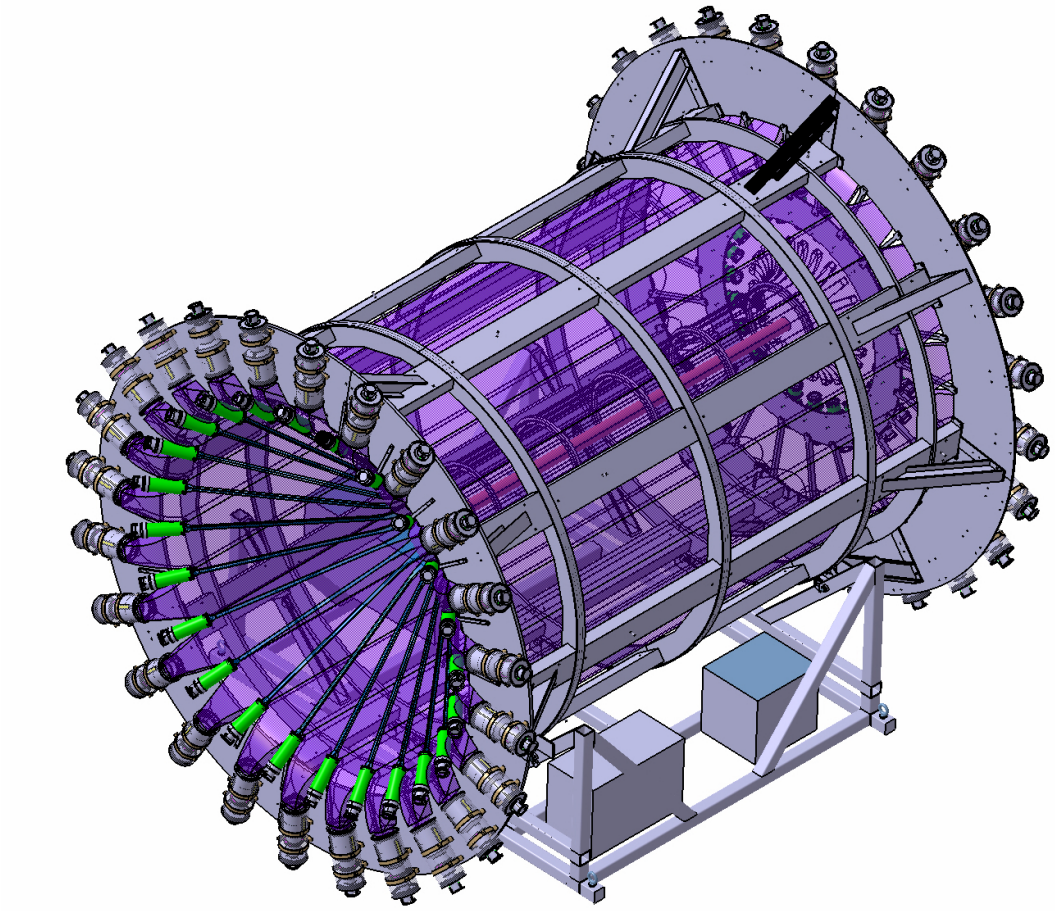


Figure 3.5: Schematic drawing of the CAMERA detector. The dimensions of the outer barrel are 4.0 m in length and 2.2 m in diameter. For time calibrations of the detector and PMT functionality tests, a laser system connected to the scintillating slats is integrated into the design of the CAMERA detector. In the gray boxes placed below the detector barrel, the space for the electronic readout and the high voltage is foreseen. The entire detector is self contained and can be lifted into the COMPASS-II target area after commissioning at test facilities.

small and large angles from beam halo tracks.
Two methods exist to separate the muons with different angles and momentum transfers: the *vertical and horizontal target pointing*. Horizontally orientated hodoscopes are able to separate particles concerning geometric conditions with a "target pointing" scheme. This method can be applied for scattering under large angles only. Whereas the vertically arranged hodoscopes are suppressing particles depending on the degree of deflection in the dipole magnets (see Fig. 3.7).

For the COMPASS-II spectrometer four types of trigger systems are foreseen which can be used to identify muons from DVCS events: The *Ladder trigger* will identify muons scattered under small angles with high energy loss and small Q^2. To perform *horizontal target pointing*, the system uses the hodoscopes H4L and H5L. The *Middle Trigger* covers the relative energy transfer y from 0.1 to 0.7 at small scattering angles by using *vertical and horizontal target pointing* with the hodoscopes H4M and H5M. The *Outer Trigger* covers the full range in y and large Q^2 up to $10\,(\mathrm{GeV/c})^2$ (see Fig. 3.6, [5, 41]).
Since 2010 the *LAS trigger* has been used with the hodoscope planes H1 and H2. This system is used to generate a trigger on geometric information. Therefore, an electronic readout system has been set up to determine the meantime of the signals generated in the two photomultipliers, which are used to readout a hodoscope scintillator slat. These meantimes have to be combined with geometric information interpreted by a trigger matrix to generate the LAS trigger.

Two GANDALF modules equipped with Digital Mezzanine Cards[9] have already been used during the 2010 run to implement this trigger design at the COMPASS experiment [42]. The new trigger extends the experiment trigger to the region above $Q^2 > 20\,\mathrm{GeV^2/c}$. This electronic readout functionality is one of the various additional applications which can be performed within the GANDALF framework.
In the upstream direction of the target region, veto elements are set-up to suppress the halo of the beam. Particles in the halo region of the beam which are not passing the target could generate a false trigger signal. These events will be rejected, if a veto counter detects corresponding particles. The veto system covers an area of $250 \times 320\,\mathrm{cm}$ in the x-y plane of the spectrometer.

3.4.2 The CAMERA Trigger

The planned CAMERA detector is integrated into the COMPASS-II upgrade for the time-of-flight measurement of recoiled protons from the liquid hydrogen target. The two barrel design will allow for measuring the times of occurring particles in *Ring A* and *B* and the respective energy deposition. The detector will also be used to separate the proton signal from the background, like delta electrons, pions and particles from the beam halo. Therewith, a trigger signal will be generated from the detector information which can be included in the first level trigger of the experiment.
In the COMPASS setup used for DVCS test in 2009, a small RPD was included and different first level trigger conditions could be tested. These trigger capabilities will be significantly extended with the future CAMERA detector by the GANDALF electronic readout framework. For the trigger schemes explained below, it is absolutely necessary

[9] A detailed description about the mezzanine cards follows in section 4.1.3

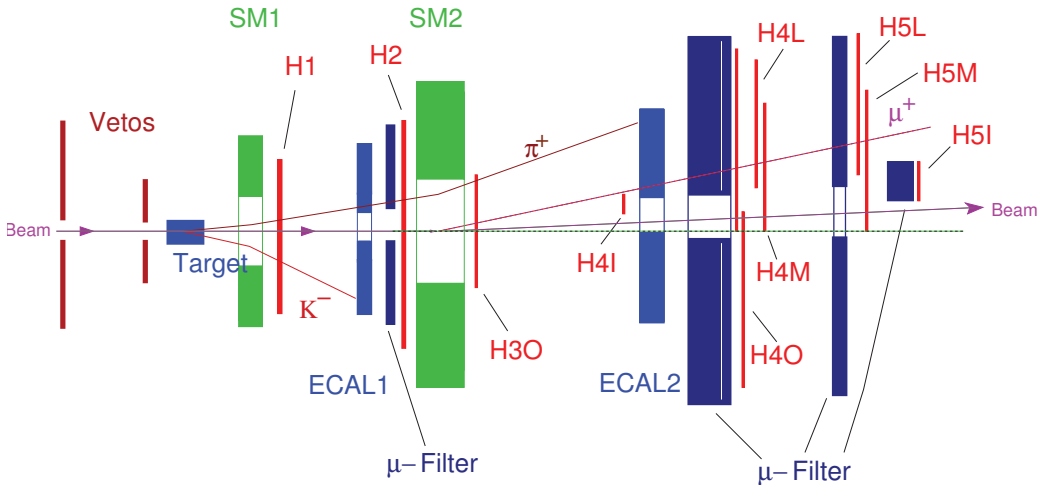


Figure 3.6: Location of trigger relevant components used in the COMPASS-II spectrometer [5]. The inner trigger hodoscopes H4I and H5I will not be used for DVCS measurements.

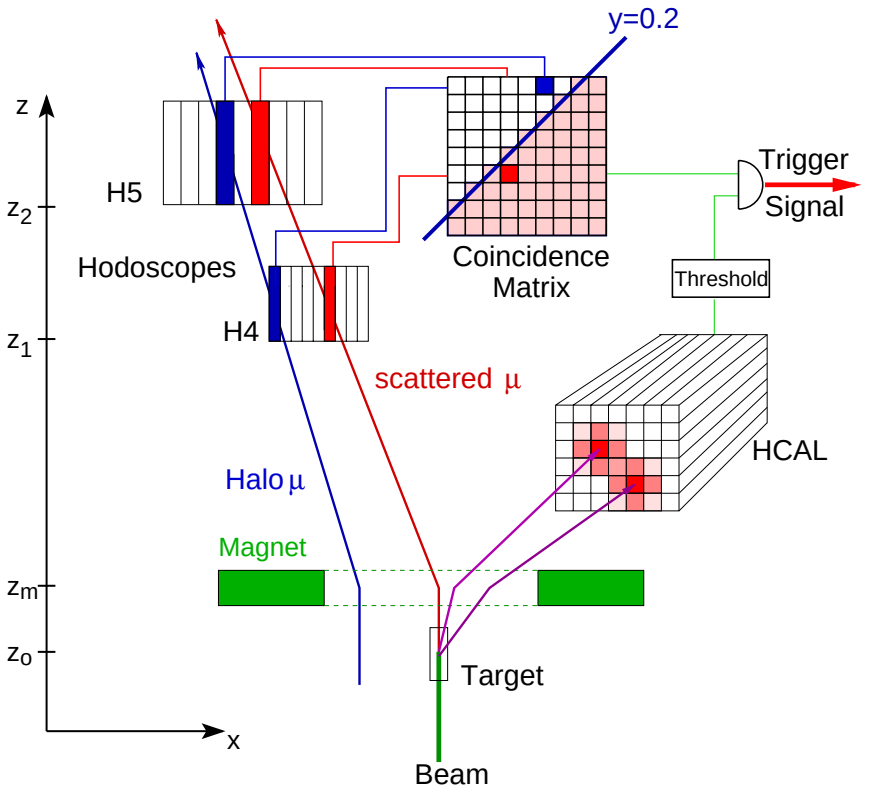


Figure 3.7: Schematic overview of the energy loss trigger. The scattered muon (red arrow) passing the target produces signals in two hodoscope elements of H4 and H5. If a coincidence occurs in the activated area of the coincidence matrix (sallow red) a trigger is generated. The muon from the halo (blue arrow) does not activate the trigger. A minimum energy deposition in the HCALs may be used as additional constraint [41].

that a central readout module has all detector information available. In the next chapter *The GANDALF Framework* the technical implementation for such a central readout scheme is described.
Here, an overview of different possible trigger conditions on a recoil proton is given:

- **Geometric correlation**

  If a recoiled proton passes *Ring A* and *B* of the CAMERA detector, an angular coincidence between signals in two opposed scintillator slats can occur. To optimize the resolution of the detector, the slats of *Ring A* will not cover the same absolute angle of $\alpha = 15°$ as the ones from *Ring B*. Instead *Ring A* is rotated azimuthally to *Ring B* by $\beta = 7.5°$. Enabling the generation of trigger decisions from geometric coincidences, ring segments of three slats have to be combined. This summarizes to the information of six readout channels for one tracking segment of the CAMERA detector (one slat from *Ring A* and two corresponding slats from *Ring B* read by two PMTs each). Due to the exclusivity of the measured events, an exclusion condition of all remaining slats can be considered. Fig. 3.8 demonstrates the logic composition of an event detected on a geometric signature.

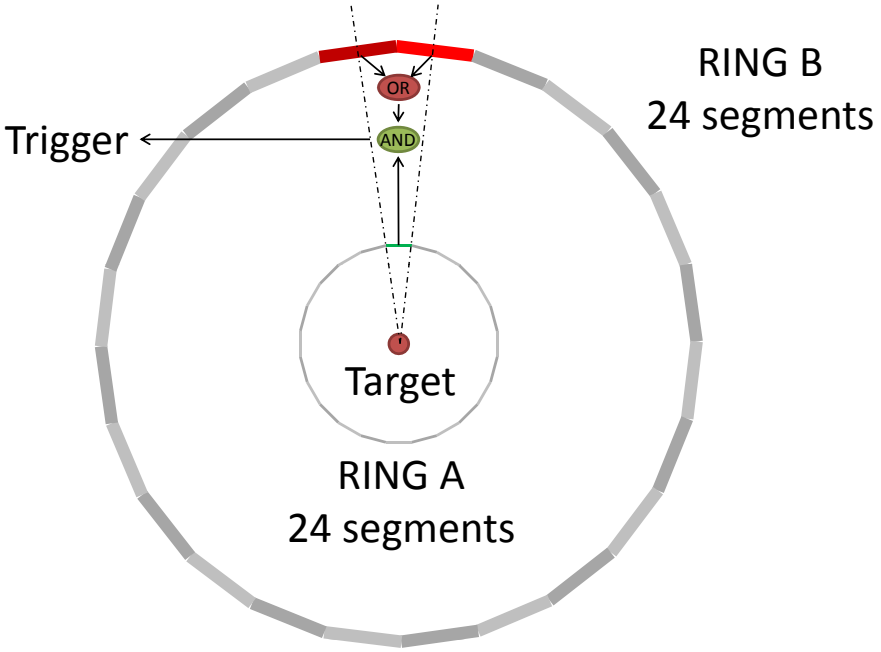


Figure 3.8: Geometric correlation of a particle passing scintillator slats in *Ring A* and *Ring B* can be used to generate a proton trigger in the CAMERA detector.

- **Energy deposition**

  Following the Bethe-Bloch formula, describing the energy loss of charged particles in matter, a significant correlation for the energy deposition in the *Ring A* and *B* can be found. Simulation results for the RPD are given in Fig. 3.9. The signatures

of protons (filled circles) and pions (unfilled circles) can be separated from the background by defining thresholds (S^{High}, S^{Low}) for the energy deposition in *Ring A* and *B*. With the following composition, a basic separation from the detector background is possible [43]:

$$(E_A > S_A^{Low}) \wedge (E_B > S_B^{High}) \text{ or } (E_B > S_B^{Low}) \wedge (E_A > S_A^{High}) \tag{3.3}$$

This composition has been implemented electronically in the 2008 and 2009 DVCS test runs at COMPASS as described below. In the future setup a more powerful electronic readout with a good signal-amplitude resolution will have the capability to provide much more detailed signatures on the proton signal.

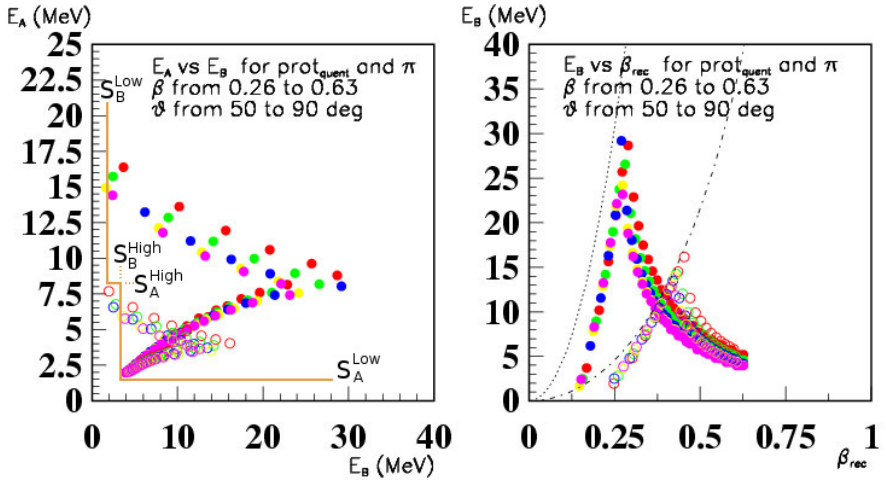


Figure 3.9: Energy deposition for protons and pions in the recoil proton detector [44]. The left figure shows the energy deposition of a particle in *Ring A* in dependency on the deposition in *Ring B*. The right figure gives the energy deposition in *Ring B* in dependency on β (filled circles: protons, unfilled circles: pions).

- **Time correlation**

  A third concept for the recoiled proton trigger is a coincidence in time between the incoming muon particle and the recoiled proton. The scintillating fiber detectors (*FI01* to *FI02*) located upstream to the target provide time information about the beam particles passing the target (see Fig. 3.10). If a recoiled particle is detected in the CAMERA, a time coincidence between the recoiled particle and the beam particle can be generated. Therefore the readout electronic must be able to perform fast calculations on the time information of the complete CAMERA detector (t_{Aup}, t_{Adn}, t_{Bup}, t_{Bdn}) and must be able to accept the time information of the incoming muon measured by the scintillating fiber detectors (t_{FI}).

The implementation of the energy deposition and geometric correlation of the proton trigger was performed during DVCS tests in 2008 and 2009 inside a Virtex-4 FPGA

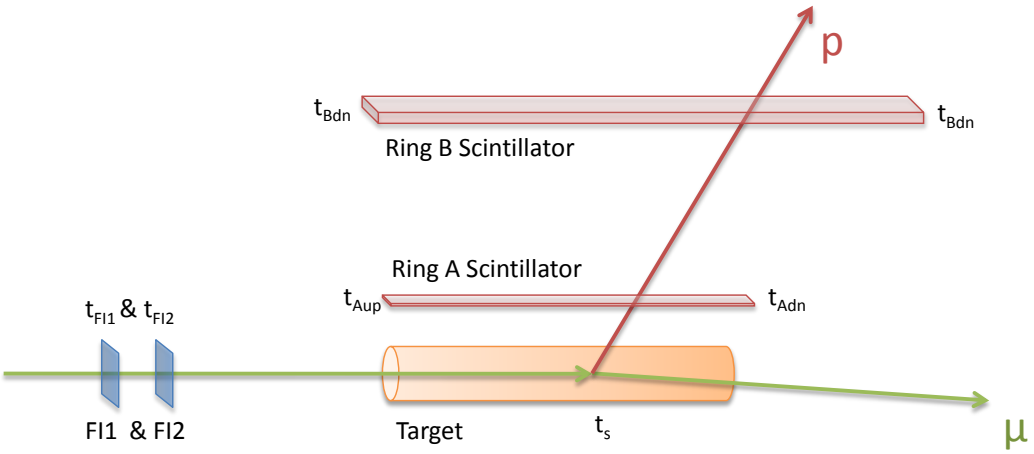


Figure 3.10: Time correlation of the incoming particle and the recoiled proton can be used to generate a proton trigger in the CAMERA detector.

[45]. Eight copies of the analog signals from the RPD with different amplifications were generated. Two connected to ADCs[10] for amplitude measurements, three with amplification factors of 0.1, 0.2 and 0.7 were connected to TDC units for time and time over threshold measurements. The remaining copies were connected to constant fraction modules to use the information in coincidences as explained in Fig. 3.11. For the energy deposition measurement the analog sum of upstream and downstream scintillators is composed.

3.5 Data Acquisition System

The DAQ[11] at COMPASS-II has to accomplish great challenges for the electronic readout of the spectrometer. It has to be able to cover the read-out of 250.000 channels spread over a large spectrometer dimension of $4\,\mathrm{x}\,5\,\mathrm{x}\,50\mathrm{m}^3$ at trigger rates of up to 100 kHz. The high beam intensity of 4×10^8 muons per spill results in high hit occupancies per channel of up to several MHz. This produces in total several Gigabytes of data per second, the data rate the readout system has to deal with.

A schematic overview of the data stream from the detector readout to the storage of the recorded data is given in Fig. 3.12. The detector signal is digitized by TDC[12] or ADC units as close as possible to the detector front ends. These are mainly located on front-end cards or readout modules like GANDALF and CATCH[13] modules. In case of front-end cards the digitized data is then pushed to GANDALF, CATCH or GeSiCA[14]

[10] Analog-to-Digital Conversion
[11] Data Acquisition System
[12] Time-to-Digital Conversion
[13] COMPASS Accumulate, Transfer and Control Hardware
[14] GEM and Silicon Control and Acquisition

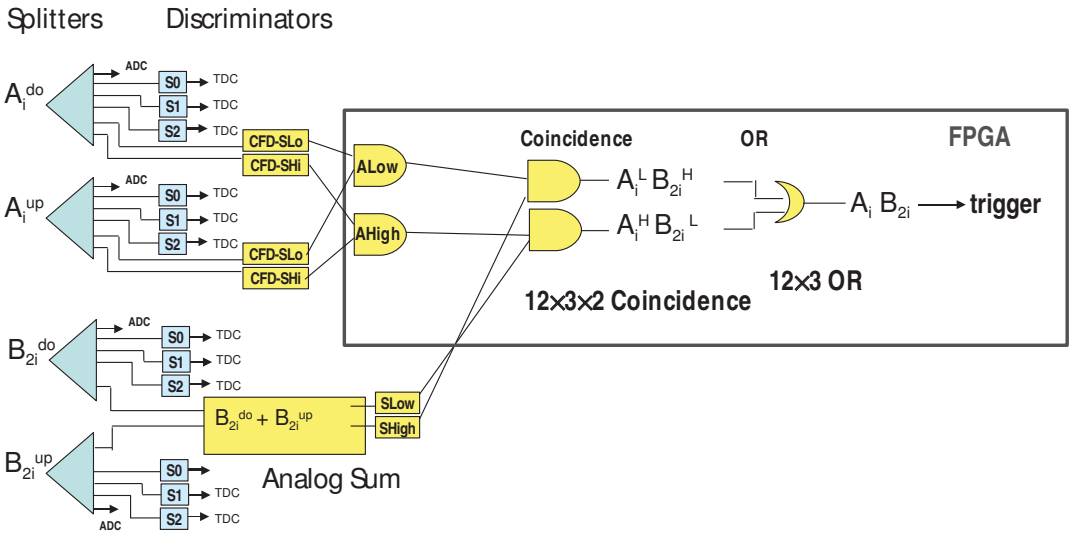


Figure 3.11: Schematic overview of the recoil proton trigger used with the small recoil proton detector installed in the COMPASS spectrometer during the 2008 and 2009 run [43].

readout modules. These modules merge and combine the received data and add detector channel information. At the same time these modules transmit the trigger information, received by the TCS[15], to the front-end units for data amount reduction. From the readout modules data is transmitted with a maximum data rate of 160 MByte/s to ROB[16]s via the S-LINK interface [46]. The ROBs have the functionality to buffer the incoming data from the front-end electronics.

In this state the experimental data is stored on different ROBs, depending on its detector origin. An event builder farm is installed to merge the data event by event in a round robin approach. The event builders PCs are connected to the ROB PCs via a Gigabit Ethernet switch. The merging process is performed continuously in the on and off spill phase. After merging the data, it is removed from the readout buffers and stored on the event builders. Next it is flagged ready to be transferred to the CDR[17] located on the main campus of the CERN facility some 6 km away. There the data is first stored on disks and finally transferred to magnetic tapes.

[15] Trigger Control System
[16] Readout Buffer PC
[17] Central Data Recording

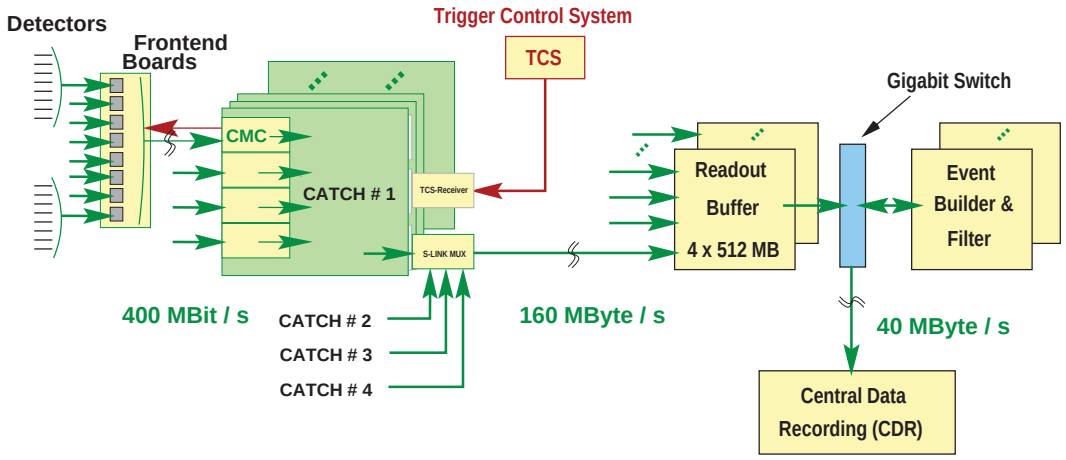


Figure 3.12: Schematic overview of the COMPASS data acquisition system [47].

3.5.1 Motivating the development of the GANDALF framework

The state of the art COMPASS data acquisition and front-end readout does include modules for the measurement of occurring detector signals with high precision time-to-digital conversion and simultaneous analog-to-digital conversion. Thus, for the readout of the planned CAMERA detector a new readout electronic solution had to be designed that fulfills the following tasks:

- Covering an electronic readout of up to 100 channels from the CAMERA detector.
- For time-of-flight measurements between the *Ring A* and the *Ring B* of the CAMERA detector: Determine the time information from the pulse shapes with fast rise times ($t_{rise} \approx 3.0\,\mathrm{ns}$) and a large dynamic range (input voltage from $0.0\,\mathrm{V}$ to $-4.0\,\mathrm{V}$). The time resolution of the readout system should exceed the detector resolution of $\sigma_t \approx 200\,\mathrm{ps}$.
- To enable a cut on the energy deposition of the particles in the CAMERA detector: Determine the maximum amplitude and integral information from the pulses.
- Due to the expected high rates in the detector: Perform the separation of near following pulses.
- Provide a possibility to generate a first level trigger signal on the information from the complete detector. Therefore, a possibility must be provided to compile the information from the entire CAMERA detector to a central unit for trigger processing.

These requirements could not be handled by one of the existing electronic readout modules. Therefore, the development of the GANDALF module was initiated with the work summarized in this thesis. The next chapter *The GANDALF Framework* will provide an overview of the GANDALF module and its capabilities to cover all above mentioned challenges.

4. The GANDALF Framework

The design goal for the GANDALF module was to create an electronic readout module which can perform the readout of the CAMERA detector for recoiled protons (see section 3.3.2). As mentioned in the preceding section, *Motivating the development of the GANDALF framework*, there are different challenges an electronic readout for the CAMERA detector has to master.

The response of the detector to a passing particle is an electrical pulse from the photomultiplier to which the electronic readout is connected to. Since both characteristics of such a pulse, the time as well as the amplitude, have to be extracted, it is important for the readout system to be able to process the full pulse shape.
With this requirement electronic designs focusing on time-over-threshold methods were excluded due to the loss of information of the pulse shape characteristics. In our case shaping or integration mechanism for the pulse shape processing is not an adequate technique since the expected rates of pulse occurrences from scintillation slats are high. Near following pulses would be smeared and could not be separated anymore.
Therefore, it was decided to choose a fast analog-to-digital conversion of the incoming pulse shapes from the detector channels. This enables detecting pulses which are close to each other or even may pile-up.

As the expected rise times of the pulses are of the order of $t_{rise} \approx 3.0\,\text{ns}$ the sampling rate of the analog input has to be of the same scale. To receive information about the possible time resolution depending on the pulse shape and sampling rate different simulations were performed in advance of the development stage of the module (see section 5.1). Based on this knowledge, a flexible analog-to-digital conversion unit was designed from off-the-shelf ADCs which reach sampling rates of up to 500 MS/s at a resolution of 12 bit.

The VME specification was chosen for the communication and power supply environment of the modules. This standard has an important extension, the VITA41.0 VXS specifications. It provides an additional communication between each of the attached modules with an additional central module. This data transfer is used by the GANDALF modules to solve the trigger generation challenge mentioned in section 3.5.1. The measured information from all detector channels of the CAMERA detector will be compiled in a central unit to perform trigger decisions as described in section 3.4.2. The VXS bus integrated into the VME crate backplane enables the necessary synchronous data transfer.

With these design constraints a 6U/VME64x VXS compliant module was designed, built and commissioned through the last four years of this thesis. GANDALF can host up to 16 analog readout channels placed on two exchangeable Analog Mezzanine Cards

(AMC). An additional mezzanine card establishes the connection of the module to the clock and trigger distribution system.
The processing of the digitized data to extract the time as well as the amplitude information online is performed with a Virtex-5 SXT FPGA which directly collects the data from the ADCs [48]. This FPGA was chosen to provide the amount of fast logic needed for the operation of the pulse shape processing algorithms. An additional FPGA is placed on the module with the functionality of a memory controller connected to 144 Mbit QDRII+ and 4 Gbit DDR2 memories. The configuration and data transfer can be done with a variety of interfaces like VME, USB2.0 or the S-LINK interface.
Including exchangeable mezzanine cards into the design of the GANDALF module a wide spectrum of electronic readout functionalities can be achieved due to this modularity. In combination with the re-programmability of the central FPGAs the spectrum for readout tasks can easily be extended. By exchanging the mezzanine cards with Digital Mezzanine Cards (DMC) the readout task can be completely changed e.g. to a 64 channel mean timer with coincidence matrix functionality as already performed and described in [42][1].

The main focus of the following sections will be put on the operation of the GANDALF module as a *transient analyzer* which covers the digitization of analog detector signals combined with online pulse shape processing algorithms. The parts of the GANDALF framework used for this configuration would be a GANDALF module with two Analog Mezzanine Cards and a GIMLI[2] card as shown in Fig. 4.1.

The *Hardware* section of this chapter will give an overview on these different electronic modules. It will focus separately on the mezzanine cards, interfaces and electronic devices which were designed within the GANDALF framework. A detailed description of the interfaces, clock structures and configuration modes of the module is given in this chapter. The provided information is also meant as a reference for experts working with the GANDALF module. All the design, development and simulation work was accomplished with in the course of this thesis.

Devices like FPGAs and other electronic parts will be mentioned in the following sections. To make a reference and location of the parts on the GANDALF module possible, the reference designators are given in brackets e.g. (*U9*). Together with the reference designators overview (see App. A.4) it is possible to locate the mentioned parts on the PCB. To clarify number bases, values represented in hexadecimal format are headed by $0x$, binary formats are enclosed by quotation marks e.g. '1001' and register notations indicate the binary width of the register in brackets e.g. $[HEXID(8)]$. Different data in binary or hexadecimal representation can be composed with an ampersand '&' to one expression e.g. $[HEXID(8)] = [SW1(4)]$ & $[SW2(4)]$.

4.1 Hardware

4.1.1 Board Interfaces

The GANDALF module is equipped with a variety of interfaces for configuration, communication, monitoring, clock and trigger signal distribution and data readout. A

[1] Please refer to http://hadron.physik.uni-freiburg.de/gandalf for more publications about the functionalities and applications of the GANDALF module

[2] The functionalities of the mezzanine cards and the GIMLI card are described in detail in 4.1.3

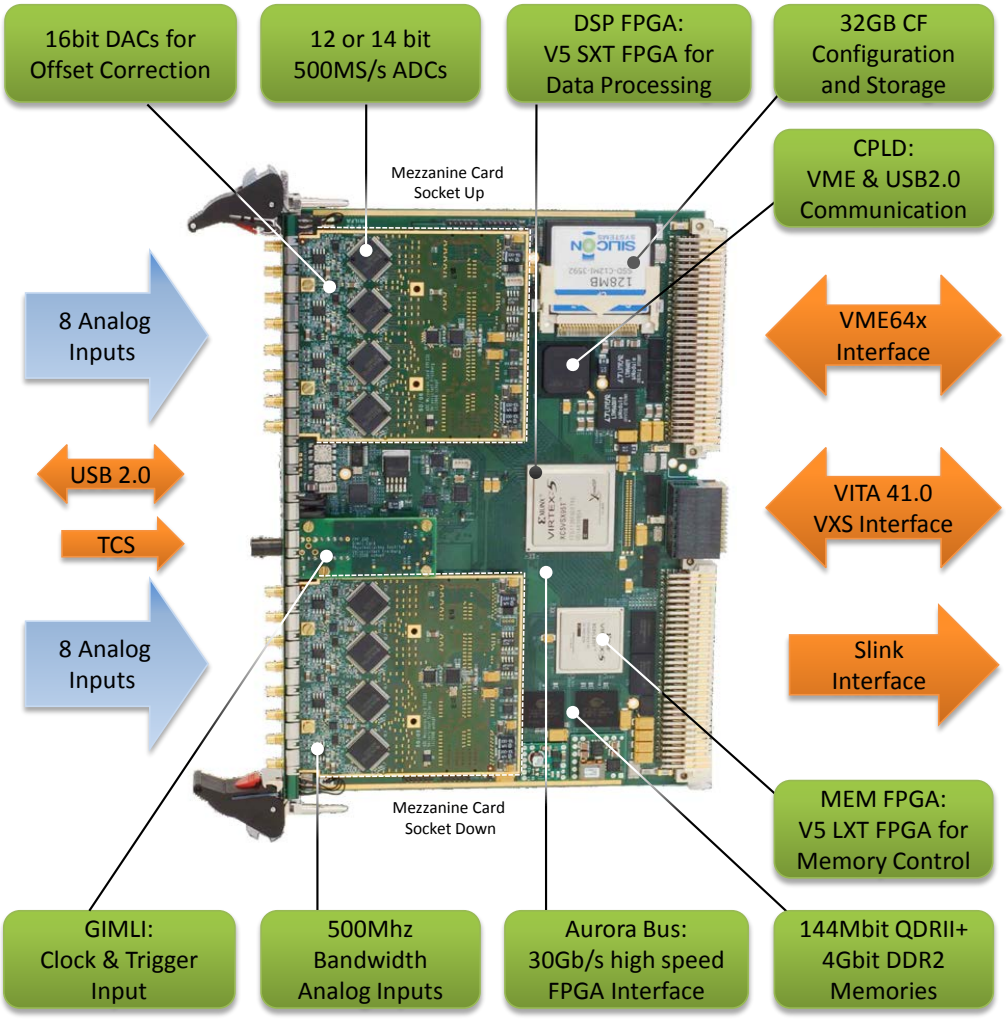


Figure 4.1: General overview of a GANDALF module used as transient analyzer. In this overview two AMCs are mounted for a connection of up to 16 analog input signals (blue arrows). The VME64x, VITA41.0, S-LINK and USB2.0 interfaces are shown in orange colored arrows and described in detail in section 4.1.1. The green boxes give an overview of the hardware components and technologies used with the GANDALF module and which are explained in this chapter. The white dashed lines surrounding the mounted AMCs represent the mezzanine card sockets *up* and *down*.

detailed description of the different interfaces is given below. In Fig. 4.2 the location of the different interfaces on the GANDALF module can be found.

- **VME Interface**

  The module was designed to be mainly operated in two environments, a multi module crate environment or in a standalone single module mode. For the op-

eration in a crate environment the GANDALF module is designed as a VME64x device which can share one common VME crate with up to 20 other devices depending on the crate type [49]. Communications with the GANDALF modules for configuration and monitoring are performed via the VME64x backplane bus. The bus master can be Linux CPU e.g. the *A20 - 6U VME 2eSST Intel® Core™ 2 Duo SBC* VME CPU which is also located in the VME crate placed at slot 1 (see Fig. 4.2, [50]). The VME64x specification permits a 64 bit wide address and data range for a data transmission of up to 80 MByte/s. As all slaves in a VME crate share the same bus a communication between the master (VME CPU) and one slave (GANDALF module) is possible at a time. To access the GANDALF module via a *VME command* the CPLD (*U8*) located on the GANDALF module has to read the address and data information applied to the VME bus. To perform a *VME write command* the user has to execute a *./vme_write* command on the VME CPU transferring the VME address and the data word[3]. The following command structure is used with the *./vme_write* command to write a 32 bit data word to a 32 bit VME address[4]

$$\#> ./vme\_write\ [VMEADDRESS(32)]\ \ [DATAWORD(32)],$$

where *[VMEADDRESS(32)]* is composed of *0xE0[HEXID(8)] [GADDRESS(16)]*. The *[HEXID(8)]* is used to address a dedicated GANDALF module. It is a selectable module address which can be changed using the DIP switches (*[HEXID(8)] = 0xSW2& SW1*, see Fig. 4.3). The *[GADDRESS(16)]* is chosen from the address sub-range for the communication with the internal software of the GANDALF modules. A detailed description for this communication is given in section 4.2.
For a *VME read command* the same syntax as for a *VME read command* is used:

$$\#> ./vme\_write\ [VMEADDRESS(32)],$$

The script then returns the corresponding read data word to the console. A more detailed description about the internal address structure *[GADDRESS(16)]* of the GANDALF module can be found in the software section of the VME CPLD interface (see section 4.2.2).

A dedicated *VME read command* is used to identify the number of modules installed in a VME crate as well as their slot number (see Fig. 4.2). The VME64x/VXS specification defines a geographic address bus which enables localization (slot number) of the dedicated module in the crate [51]. This geographic address bus is connected to the CPLD and the information can be read together with the serial number of the module using the command:

$$\#> ./vme\_write\ E0[HEXID(8)]00FC,$$

[3]The firmware for the VME communication can be found at http://hadron.physik.uni-freiburg.de/gandalf

[4]#> remarks the text input of the bash shell of the VME CPU.

The script will return the following information

$$[CONF(4)][HEXID(8)]'000'[GEOADD(5)]'00'[SN(10)],$$

where *[CONF(4)] = '11' [INIT][DONE]* gives the configuration status of all FPGAs on the GANDALF modules, where *[INIT]* is '1' when both FPGAs are ready to accept configuration data and *[DONE]* is '1' if the firmware download to both FPGAs is completed successfully. The *[GEOADD(6)]* gives the slot number inside the VME crate where the module with the serial number *[SN(10)]* is located. The serial number is binary hard coded on the GANDALF modules via a selection of placed $0\,\Omega$ resistors (*R20* to *R29*).
Two bus transmission modes exist for the data transfer: the single word transfer and the *blockread/blockwrite mode* [52]. The block transfer is done by a DMA access in the VME CPU and is used to transfer the configuration data for the FPGAs to the GANDALF module. It can also be used for *Spy FIFO* data readout from GANDALF module to the VME CPU (see section 4.2.2).

- **VXS Interface**

  The GANDALF module is designed to meet the additional VXS[5] specifications described in the VITA41.0 [51]. Therefore, an additional high speed serial backplane bus is defined to permit communication between the payload boards (GANDALF module) and the central switch module (TIGER[6] module, FPF339). This backplane bus enables synchronous serial data transmission of eight differential lanes from the central DSP-FPGA (*U9*) of each GANDALF module to each of the two TIGER modules. An overview of the bus structure is given in Fig. 4.2. The two TIGER modules also share another 16 lanes wide high speed bus for inter communication. With this configuration, it is possible to combine the data produced by up to 18 GANDALF modules with the two TIGER modules with very low latency time.

  This structure was chosen to allow for fast trigger decisions based on data measured by all GANDALF modules housed in a VME64x/VXS crate. The implemented protocol is not compliant to the VITA41.0 specifications, because it is designed to guarantee synchronous timing between payload and the TIGER boards, which is not covered by the specification. Additionally, the VITA41.0 specification defines an I2C bus which is included in the VXS connector for transmission of configuration information for the TIGER module or to realize the control of bus buffers for GANDALF or TIGER module insertion or removal [53].

- **Clock and Trigger Interface**

  Whenever more than one GANDALF module is used in experiment the synchronization of the modules must be guaranteed. Therefore, the GIMLI card was designed to establish an interface to the COMPASS Trigger Control System (TCS) [25, 54]. With the TCS interface, the experiment clock and trigger information is provided to the GANDALF module. It transfers a synchronous clock signal of

[5] VME Switched Serial
[6] **T**rigger **I**mplementation for **G**ANDALF **E**lectronic **R**eadout

155.52 MHz via an optical fiber with a Time Interval Error (TIE) below 60 ps. Due to a two channel data transfer protocol, it is possible to transmit a synchronous trigger signal and also information about the trigger type, event and spill number on one single optical fiber.

- **Transition Interface**

  The VME64x specification permits the board designer to choose dedicated user pins to define an interface for VME backplane transition cards. Here the S-LINK interface was chosen to make the GANDALF module compatible with the equipment used in the *COMPASS-II* experiment [32, 46]. As all bus lanes for the transition card communication are connected to both the DSP and MEM-FPGA (*U9*, *U25*) the internal logic can be adapted for other types of transition cards to enable several interfaces e.g. an Ethernet protocol compliant interface (see section 4.15). With the 32 bit data bus the S-LINK interface permits a data transmission rate of up to 160 MByte/s.

  Instead of using a single S-LINK source card, the S-LINK MUX module can also be used as transition card [55]. This module merges the data of up to four GANDALF modules for readout with one S-LINK source card. To use the S-LINK MUX module, the same data protocol as for the S-LINK card can be used as defined in the S-LINK specification with one exception [46]. A common reset on signal *SRESET* pin C30 (P2, [49], see Tab. B.2) has to be set by all (up to four) connected GANDALF modules at the same time. This can be applied for example during the synchronous BOS[7] signal (see section F.1).

- **USB2.0 Interface**

  As mentioned above, there are plenty of applications outside COMPASS for which one GANDALF module only can cover the entire readout challenges. This could be e.g. test facilities for scintillator slats or pattern generator tasks. The *GANDALF portable* can be used in cases where the user does not want to operate a complete VME crate to utilize only a single GANDALF module (see section 4.1.12). To access the CPLD (*U8*) for configuration or monitoring independent from the VME backplane, a USB2.0 interface can be used [56]. The front panel of any GANDALF module has an USB mini AB connector implemented which is connected to the *CY7C68001* EZ-USB SX2^{TM}High-Speed USB Interface Device. This USB device is used in other COMPASS electronic readout equipment like the *BalizaUSB* [57, 58]. A 16 bit interface bus establishes the communication between the USB Interface Device and the CPLD. The four 1 kByte FIFOs implemented in the *CY7C68001* (*U20*) at Endpoint 0 are used to derandomize the control commands between USB host and the CPLD. The Endpoints 2 and 6 are used for data transmission of the FPGA configuration bitstream files and the Spy FIFO (see section 4.2.2). The endpoint configuration for the *CY7C68001* is stored in the *24LC128* EEPROM[8] (*U24*) [59]. With the USB2.0 interface the configuration, the monitoring of the GANDALF module and the data readout via the *Spy FIFO* can be performed

[7] Begin Of Spill

[8] Electrically Erasable Programmable Read-Only Memory

identically like using the VME interface (see section 4.2.2). A GUI called "USB Toolbox" was created for these processes and is described in section 4.2.4 [60].

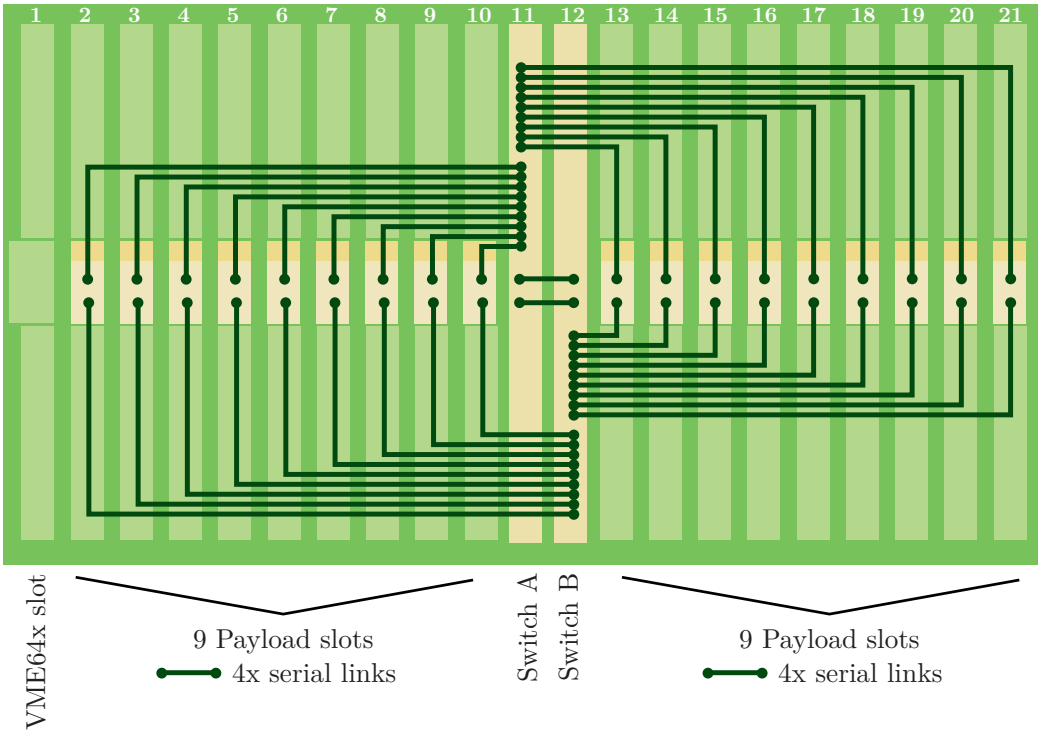


Figure 4.2: Schematic overview of the bus structure of a VXS crate. Any GANDALF module placed in slots 2 to 10 and 13 to 21 has eight high speed lanes to each TIGER module placed in slots 11 or 12. Slot 1 is reserved for the VME CPU [25].

4.1.2 Mezzanine Sockets

The main reason for the modularity of the GANDALF module is the possibility to mount different mezzanine cards onto the module to change its functionality. Each GANDALF module can host two separate mezzanine cards on two mezzanine card sockets (MCS) *up* and *down* and one clock and trigger mezzanine on the GIMLI mezzanine card socket (see Fig. 4.1).
Presently two types of mezzanine cards, dubbed AMC[9] and DMC[10] exist [25]. A third mezzanine card, the OMC[11] has reached production status during the publishing date of this thesis. Two different types of GIMLI[12] cards exist [25]. These cards are used for a synchronous input of clock and trigger signals. An overview of the different mezzanines will be given in the next section.

[9] Analog Mezzanine Card, FPF334
[10] Digital Mezzanine Card, FPF335
[11] Optical Mezzanine Card, FPF338
[12] FPF332 (fiber), FPF333 (copper)

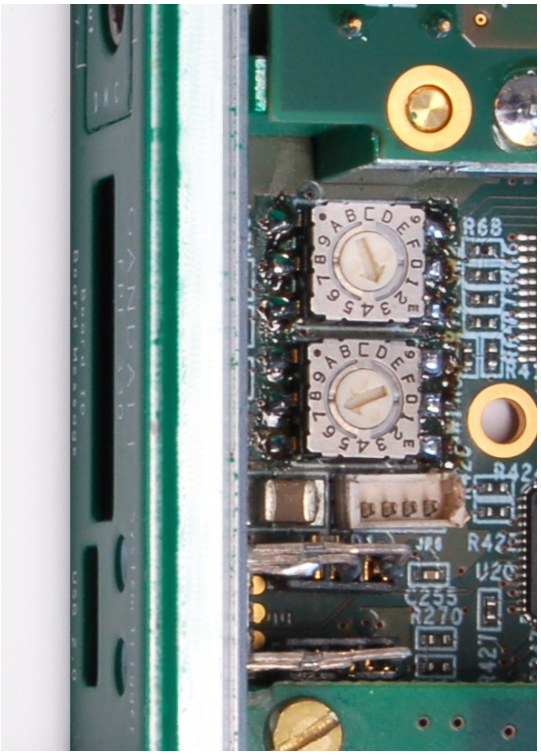


Figure 4.3: Picture of the DIP switches to select the *[HEXID(8)]* of the GANDALF modules. In this picture for example the $[HEXID(8)] = 0x37$ is set.

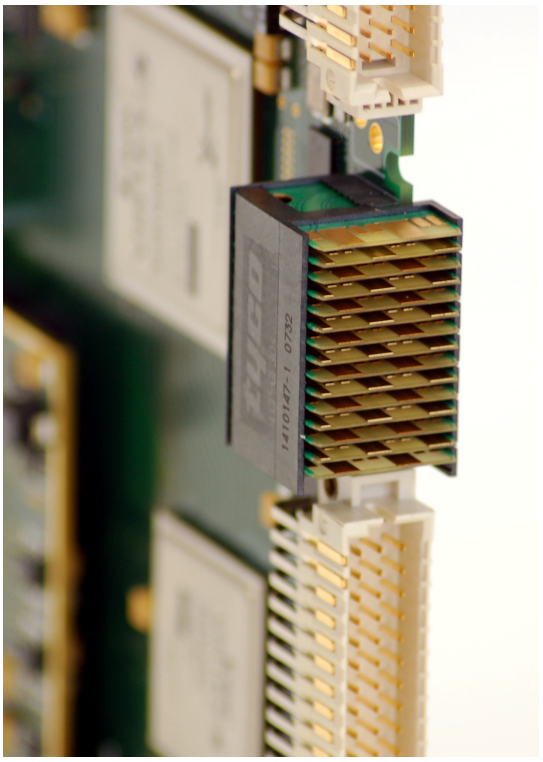


Figure 4.4: Picture of the VXS payload connectors located at the GANDALF modules between the VME connectors (*J1*) and (*J2*).

Each mezzanine card socket consists of two high density, differential pair sockets *QSH-080-01-X-D-DP-A* by *Samtec Inc.* which are labeled (*J5*, *J6*) for the mezzanine card socket *up* and (*J7*, *J8*) for the mezzanine card socket *down*. They interconnect different signal buses, clocks and power supply from the GANDALF module to the mezzanine card. The mezzanine card sockets *up* and *down* are totally symmetrical except one pin, located on Pin76 (*J6*) and Pin76 (*J8*), which identifies the socket. Pin76 (*J6*) (mezzanine card slot *up*) is connected to GND via a 4.7 kΩ resistor while pin Pin76 (*J8*) (mezzanine card slot *down*) is connected to $VCC3V3$ via a 4.7 kΩ resistor. This decoding is used to set different addresses to some electronic devices (e.g. the clock synthesizer) located on the mezzanines depending on the slot to which the card is mounted to.
The following list describes the different signal, clock and power buses available on each mezzanine socket:

- **Differential Pair Buses:** There are eight bus groups of 14 differential lanes from each mezzanine socket to data I/O pins of the DSP-FPGA (*U9*). One additional differential pair connects to a clock I/O of the same DSP-FPGA. The lengths of all differential pairs inside each bus group are matched. In total 112 differential data pairs and eight clock pairs comprise the bus between a mezzanine card socket (*up* or *down*) and the DSP-FPGA.
- **Clocks:** There are two clock sources available on each of the mezzanine card socket. A differential clock signal is provided by the *MC100EP210S* (*U10*) (see Fig. 4.14, [61]). This signal is a copy of the differential clock signal provided by the GIMLI mezzanine card. The frequency of this clock can be either
  - $f = 155.52$ MHz when using the fiber GIMLI card connected to the TCS (38.88MHz base frequency),
  - $f = 20$ MHz when using the copper GIMLI with an oven controlled oscillator (OCXO) or
  - any frequency up to $f = 80$ MHz when applying an external single ended clock signal to the clock input of the copper GIMLI (see section 4.1.3, [25]).

  The second clock signal is a single ended clock with LVTTL signal standard and is provided by a dedicated clock output buffer of the DSP-FPGA. Hence the frequency $f < 120$ MHz of this clock can be defined by the FPGA internal logic.
- **I2C Buses:** Two I2C buses are connected to each mezzanine card socket [53]. They are called the general purpose (GP) and the SI I2C bus. Each mezzanine card socket has its own GP bus to program and communicate with an EEPROM located on any mezzanine card. Additional I2C devices like temperature sensors or DACs[13] can be addressed on the same bus by the DSP-FPGA as I2C bus master [59]. The SI I2C bus is used to program the *SI5326* (*U11*) clock synthesizer chip located on the GANDALF module or the ones located on the mezzanine cards. Both mezzanine card sockets share the same SI I2C bus with the DSP-FPGA as master (see Fig. 4.12).

[13] Digital-to-Analog Converter

- **JTAG Buses:** For IEEE 1149.1 devices placed on the mezzanine cards, the JTAG chain bus routed from the CPLD can be used to interface the internal logic. The chain is connecting the JTAG interfaces on the mezzanine card socket *up* and *down* (see Fig. 4.26, [62]).

- **Single Ended Flags:** In case of a mounted AMC the *SI5326* clock synthesizer chip can transfer a "Loss of signal" or a "Loss of Lock" information via single ended flags. To be able to reset the synthesizer chips three more single ended flags are routed to the DSP-FPGA. If the 14 bit model of the AMC is used, an "ADC off" flag will enable a shutdown of the ADCs to save power. If a DMC is mounted, the single ended flags can be used to transmit the "NIM OUT" and "NIM IN" signal information.

- **Power Bus:** Different voltages are available for each mezzanine: +12.0 V, +5.0 V, +3.3 V and −12.0 V. In case of a mounted AMC the ADCs on this mezzanine are powered by separate digital and analog nets providing +3.3 V. This is done for reasons of noise suppression due to power supply noise and to balanced power consumption (see section 4.1.9). The maximum currents for the power rails of each mezzanine card are shown in Tab. 4.1.

Table 4.1: Maximum currents on the power bus of the mezzanine card sockets *up* or *down*.

Voltage	Net Name	Current
+12.0 V	VCC+12V	0.8 A
+ 5.0 V	VCA5V0	2.6 A
+ 3.3 V	VCA3V3	1.1 A
+ 3.3 V	VCC3V3	0.7 A
-12.0 V	VCC-12V	0.5 A
0.0 V	GND	15.0 A

The data in or output width between the DSP-FPGA and the mezzanine card sockets *up* and *down* of 244 differential pairs allows a possible maximum data rate of 14 GByte/s. A table for the detailed socket connections can be found in appendix B.2.
The central mezzanine card socket is designed to mount GIMLI cards to provide the GANDALF module with a common clock and trigger information. As mentioned above there are two types of GIMLI cards. In the following the differential signal and clock bus, flags and the power bus are described:

- **Clock:** A differential clock signal is provided by the mounted GIMLI card to the central mezzanine socket and is then routed to the *MC100EP210S* (*U10*) to distribute the clock signal to four targets: the two mezzanine card sockets *up* and *down*, the DSP-FPGA (*U9*) and the *SI5326* (*U11*), all located on the GANDALF module. The clock frequency f_{GIMLI} depends on the used GIMLI model (see section 4.1.3).

- **Data:** A differential data signal is provided which can carry the TCS decoded data in case of a mounted fiber GIMLI or directly transmits the signals given to the trigger input of a copper GIMLI (see section 4.1.3).
- **Single Ended Flags:** In case of a mounted fiber GIMLI, signals to transmit the "CLC016 locked" and the rate selection are routed to the DSP-FPGA (see section 4.1.3). In case of a copper GIMLI these flags are used as inputs to select between external clock source and the on board oven controlled oscillator (OCXO) *ASOF3S3* [63].
- **Power Bus**: There are two power nets available for each GIMLI mezzanine: +3.3 V and +5.0 V. The maximum currents are shown in Tab. 4.2.

Table 4.2: Maximum currents on the power bus of the central mezzanine card socket.

Voltage	Net Name	Current
+ 5.0 V	VCC5V0	0.4 A
+ 3.3 V	VCC3V3	0.5 A
0.0 V	GND	8.0 A

A table for the detailed socket connections of the central mezzanine card can be found in B.3.

4.1.3 Mezzanine Cards

In this section a short overview on the design ideas of the different mezzanine cards will be outlined.

- **AMC:** The analog mezzanine card was designed together with the GANDALF module to create a *transient analyzer* to digitize of time and amplitude information from analog pulses in high resolution. The design challenges are the following: fast, flexible, high resolution analog to digital conversion with continuous sampling combined with high channel density at a minimum noise level which both cause high power consumption and an immense data rate.
  An AMC can be operated in different modes. The PCB[14] design allows the assembling of two different types of ADC chips, the *ADS5463* and the *ADS5474* [64, 65]. Both chips are weighting average flash ADCs which allows for very fast sampling rates and simultaneous high resolutions of 500 MS/s at 12 bit or 400 MS/s at 14 bit, respectively. The data sheets of the both ADCs specify an ENOB[15] of 10.4 bit or 11.2 bit respectively.

  In the *normal mode* the type of ADC defines the maximum sampling rate. In this mode up to eight analog channels can be connected to one AMC, which summarizes to sixteen analog channels to be read out by one GANDALF module.

[14] Printed Circuit Boards
[15] Effective Number of Bits

To reach a higher sampling rate, the clock synthesizer chip on the AMC (*SI5326*) can be reprogrammed to feed two neighboring ADC chips with two clock signals of the same frequency, but a constant phase offset of 180°. At the cost of half the number of channels, the operation of two consecutive ADCs sampling the same input is possible in the *time-interleaved mode*. This causes a doubled sampling rate of 1 GS/s or 800 MS/s at a resolution of 12 bit or 14 bit respectively.

To change the sampling modes from *normal* to *time-interleaved mode* the electrical circuit of the analog signal input has to be changed to split the signal and provide it to the two ADCs operated in a *time-interleaved-mode*. The circuit change is performed by replacing resistors on the AMC which also assume the correct impedance for the split signal.

In the COMPASS configuration for the CAMERA readout the total dynamic range of the input circuit of each channel of the AMC is defined to $U_{tdr} = 4.0\,\mathrm{V_{PP}}$. Different pulse shape types from bipolar to negative unipolar can be processed and the input range can be shifted by 2.0 V with dynamic ranges from $-2.0\,\mathrm{V} \cdots +2.0\,\mathrm{V}$ to $-4.0\,\mathrm{V} \ldots 0.0\,\mathrm{V}$. This shift is performed with 16 bit DACs (*AD5665R*) and can be programmed by using the general purpose I2C bus (see section 4.1.4, [66]). With the replacement of resistor networks from the analog input circuit the gain of the amplifiers can be increased and other values with $U_{tdr} < 4\,\mathrm{V_{PP}}$ can be chosen. The detailed correlation between ADC value, DAC value and input voltage is described in appendix D.

Due to the very high channel density of the design and the large power consumption of the ADCs and the sensitivity of the ADC gain to heat, special attention was given to the cooling functionality and the temperature monitoring of the AMC. For this extensive, thermal simulations were performed to optimize the cooling system of the GANDALF module used with AMCs including the air flow through the heat sinks (see Fig. 4.5). Two *TMP175* temperature sensors are located on each AMC to be able to monitor the temperature behavior. They can be read out via the general purpose I2C bus (see sections 4.1.6 and 4.1.4, [67]).

As on any mezzanine card designed for the mezzanine card socket *up* or *down* an EEPROM for storage of serial number, digitization mode, resolution, default DAC values is also a member of the general purpose bus (see Fig. 4.13, [59]).
A picture of the AMC is given in Fig. 4.7. A much more detailed description of the design and the performance of the AMC can be found in [25]. Detailed measurements confirming the digitization capability of expected pulse shapes with the AMCs are given in section 5.2.

- **DMC:** The digital mezzanine card was designed to permit the usage of the logic of the DSP-FPGA for a wide range of functionalities. This mezzanine card provides the possibility to adapt up to 64 digital channels in LVDS or LVPECL signal standard directly to the user I/O of the DSP-FPGA. Using DMCs the performance of different readout tasks within the FPGA logic like time-to-digital conversion, mean timer application, trigger decision matrices, fast scalers and pattern generators is possible. With the possibility to re-program the FPGA logic, a combination of the

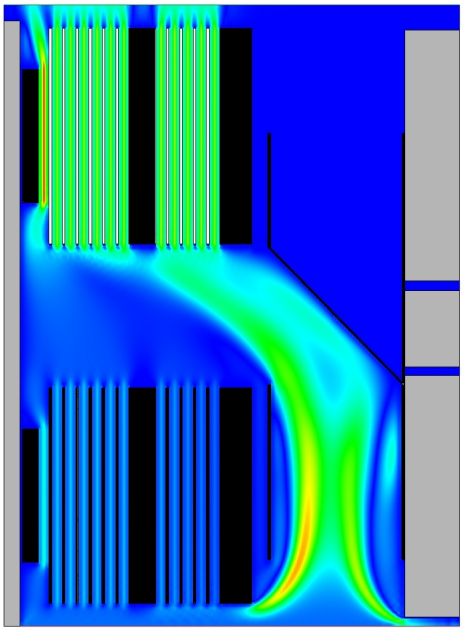


Figure 4.5: Airflow simulation for the heat sinks of a GANDALF transient analyzer. To maximize the cooling of the upper mezzanine card, an air guide was developed for the heat sink of the GANDALF module (right side). The colour represents the air flow velocity (dark blue $< 10.0\ LFM$ to red $\approx 30.0\ LFM$) [68].

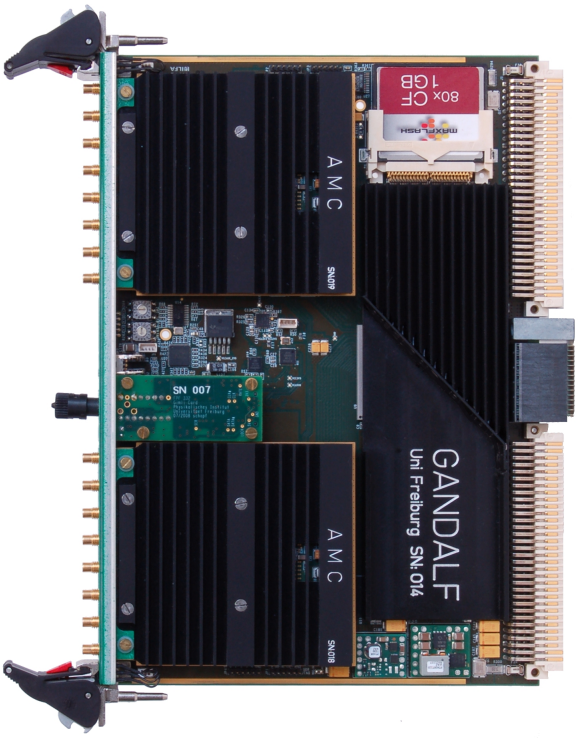


Figure 4.6: Picture of the GANDALF module used as transient analyzer with heat sinks for the AMCs and the GANDALF module. The main board possesses on single heat sink which is designed to allow passing air from the crate fans to the upper AMC.

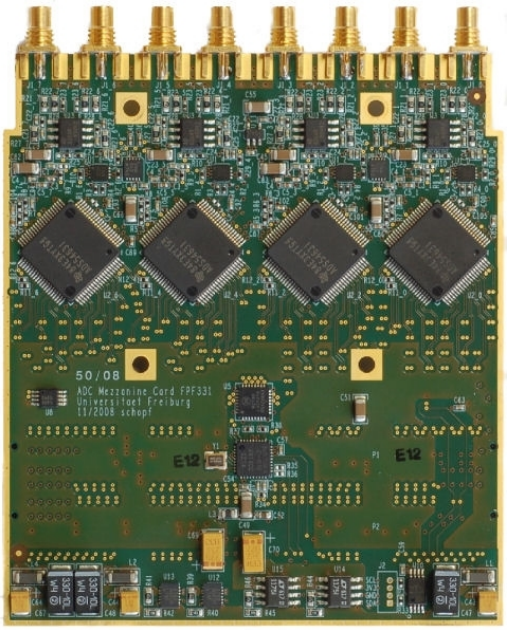


Figure 4.7: Picture of the analog mezzanine card (AMC).

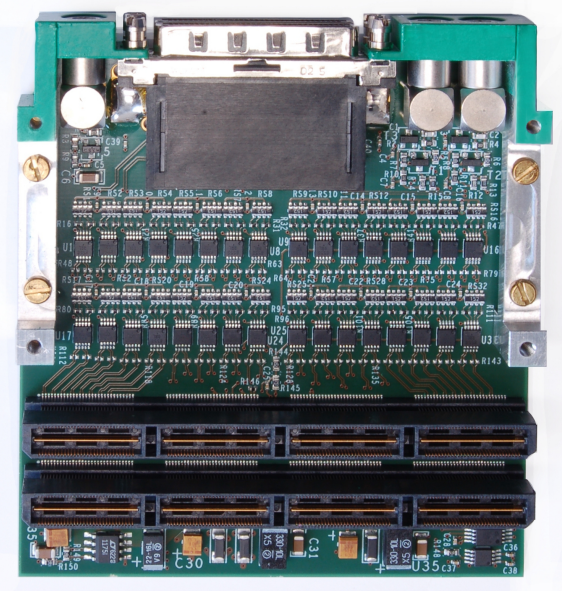


Figure 4.8: Picture of the digital mezzanine card (DMC).

mentioned functionalities can be programmed and the readout can be adapted to the given detector characteristics.

The same PCB for the DMC can be used to produce two versions of the mezzanine by a rotation of the signal buffers plus the exchange of some dedicated parts. Hence, it is possible to operate the DMC as a 64 digital channel input card or 64 digital channel output card.

This summarizes to 128 digital I/Os for a complete GANDALF module equipped with two DMCs. The interface to the DMC is realized by two 32 channel differential VHDCI *HDRA-ED136LFZGT* connectors [69]. The signals are buffered by *NB4N855S* buffers which show a high performance in signal transfer RMS jitter of 1 ps [70]. To be able to include external gate or trigger information into the FPGA logic, a NIM input and two NIM outputs LEMO connectors are located beneath the VHDCI connectors. A picture of the DMC is given in Fig. 4.8.
First operational applications using the DMC are a 150 ps meantimer and a 128 channel TDC with 160 ps time bins [42, 71].

- **OMC:** An optical input mezzanine card will extend the mezzanine family allowing the GANDALF module to perform as a data merger, concentrator and acquisition device. The designed OMC will be equipped with four 3.25 Gbit/s transceivers to be able to receive already digitized information from front-end cards. Data preprocessing functionalities inside the DSP-FPGA are planned with the data received from the OMC.
  The optical link will be used to transmit synchronous clock and trigger information

to the front end module.

- **GIMLI:** The GIMLI mezzanine card can be placed on the central mezzanine card slot. There are two models of the GIMLI card available. The fiber GIMLI card has the possibility to adapt an optical fiber to the *HFBR-2119TZ* receiver to accept clock and trigger information [72]. In the case that the GANDALF module is installed at the COMPASS -II experiment, the clock and trigger distribution can be done by the TCS [54]. In this standard the incoming data pattern includes trigger, event number, spill number and other dedicated information [73]. The clock signal has to be recovered by this data pattern with the use of the *CLC016* chip located on the fiber GIMLI card. For the clock recovery a phase locked loop with a given center frequency is used. To switch between the 38.88 MHz TCS base frequency used at COMPASS and the 40.08 MHz frequency used at LHC[16] experiments the "RATE" input pin of the GIMLI mezzanine has to be set respectively to '1' or '0' (see section 4.1.2). The *CLC016* indicates if the PLL has locked into the recovered frequency by applying '1' to the "LOCKED" pin on the central mezzanine connector. If the TCS signal is available in an electric signal standard and not in an optical medium the optical fiber receiver can be replaced by an LEMO connector. A picture of the fiber GIMLI card is given in Fig. 4.9.

  The copper GIMLI card model can be operated if no TCS is used and the clock and trigger signals are attached by electrical cables using single ended NIM[17] signal standards. This GIMLI card is equipped with two LEMO inputs, for clock and trigger. In this case the signals are directly buffered to the differential clock and trigger outputs of the central mezzanine connectors. If no external clock is connected the on board oven controlled oscillator (OCXO) with a base frequency of 20 MHz and a jitter of below 2.3 ps can be selected instead. In case of a mounted copper GIMLI mezzanine card the "RATE" pin has the following functionality: If set to '0', the external clock source can be chosen, if set to '1' the internal OCXO will be used as clock source.
  A picture of the copper GIMLI card is given in Fig. 4.10. A more detailed description of the design and the performance of the GIMLI mezzanine card family can be found in [25].

4.1.4 Board Configuration

The main logic capabilities of the GANDALF module are covered by two FPGAs, the central DSP-FPGA and the MEM-FPGA. Both are volatile, therefore, the FPGAs have to be configured with its firmware after every power up of the GANDALF module. The configuration of the FPGAs is performed by loading two bitstream files into the FPGA defining the placement and entanglement of the firmware logic. The bitstream files can be loaded via external interfaces or from the on-board CF memory.

Using the external interfaces like VME or USB2.0 (see section 4.1.1), the CPLD accepts the two bitstream files for each FPGA and transfers it to the configuration interface of the

[16] Large Hadron Collider, CERN
[17] Nuclear Instrumentation Module

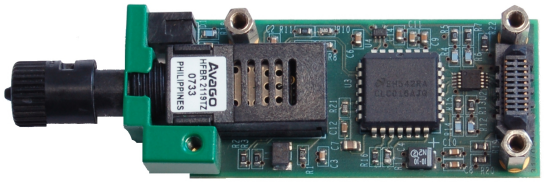


Figure 4.9: Picture of the fiber GIMLI.

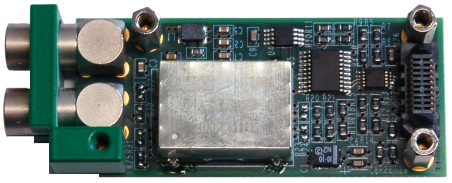


Figure 4.10: Picture of the copper GIMLI.

respective FPGA. For this communication two eight bit wide *select map* configuration buses are used. The configuration data rate is 40 MByte/s (40 MHz, 8 bit bus). In both cases, using either the VME or the USB2.0 interface, the configuration of a GANDALF module is completed in less than 500 ms. The flag *SYSCFGMODE* in the CPLD firmware has to be set to '1' to perform configuration via the external interfaces.

In the case that 18 GANDALF modules expect the same bitstream files and share a common VME64x/VXS crate, a broadcast configuration can be performed. Therefore, all boards which should listen to the broadcast configuration receive a reset signal from the VME CPU. The boards are ready to receive the configuration data after power up and the bitstream for the DSP-FPGA can be written to the VME address *0xE0[HEXID(8)]8000* in *blockwrite* mode (see section 4.1.1). The configuration data for the second FPGA will then be written to the VME address *0xE0[HEXID(8)]00014*. Where *[HEXID(8)]* is the value from the rightmost board in the crate. This board will perform the acknowledgment to the VME CPU of the received data. All other boards which were reset in the beginning of the process will configure their FPGAs with the same data written to the VME bus in parallel.

With this technique, a complete VME crate with GANDALF modules can be loaded in $t_{conf} < 500$ ms [60]. It has to be mentioned that the VME64x VITA-1.1-1997 specification has not foreseen such a procedure [49].
As an alternative approach, the configuration files can be stored on the on-board CF memory card. In this case the $XilinxSystemACE$ configuration environment is managing the configuration of the FPGA. Up to eight different firmware versions can be stored on the CF card. The configuration data is transferred via a serial link into the FPGAs. To use this mode, a hex file combining the binary files of the DSP and MEM-FPGA has to be generated first by the Xilinx ISE development software [74]. The flag *SYSCFGMODE* in the CPLD firmware has to be set to '0'.

After the configuration of the DSP-FPGA, the configuration memory (see section 4.2.3) is ready to accept individual register settings for the different GANDALF modules like serial number, experiment source ID, trigger and window settings and thresholds.
Besides the configuration of the FPGAs different power supply control and clock chips have to be configured. These devices can be separated into volatile and non-volatile devices. The volatile devices have to be reconfigured after any power up, where the non-volatile parts need only one configuration during the initial operation.
The non-volatile devices placed on the GANDALF module are the *UCD9081* (*U29*)

power sequencer and the *CDCE949* (*U14*) low frequency synthesizer chips [75, 76]. They are usually programmed on the first start operation of a GANDALF module and can be accessed via an I2C bus chain. The files are loaded via an I2C programming tool by *Texas Instruments* connected to I2C CON 2 (*JP6*) (see Fig. 4.12). The CPLD which controls the VME and USB2.0 interface can be configured by loading the bitstream file via the USB platform cable manufactured by *Xilinx Inc.* connected to JTAG 2 connector (*JP2*) (see Fig. 4.26). A script was written to perform a complete setup process for the commissioning of GANDALF modules, guiding the user to connect the different interface cables for configuration[18].

An additional non-volatile part on the GANDALF module is the *SI5326* clock synthesizer [77]. It is programmed by the *SI IF VHDL* module (see section 4.2) via a separate I2C lane (see Fig. 4.12). The content of the SI registers, defining the TCS synchronous high frequency clock provided to both FPGAs on one hand and defining the operation clock for the AURORA interface on the other hand, will be loaded after a toggle of *Fast Register* $[FR\_ADDR] = 0x028$ and at any startup (see Tab. E.2). The *SI5326* registers are saved in the *Configuration Memory* (see section 4.2.3).
For each AMC the *SI5326* devices for the sampling clock generation can be programmed via the common I2C bus for each mezzanine. For the configuration of the DACs, performing the baseline correction of the analog input circuits (see section 4.1.3), a second I2C bus per mezzanine is accessed with the *GP IF VHDL* module (see section 4.2). This chain is designed for any general purpose devices located on the mezzanine cards. That can be temperature sensors and includes the EEPROM for individual information about the mezzanine card. As a standard for all mezzanine cards designed for the GANDALF module, an EEPROM (*24LC128*) has to be attached to the general purpose I2C bus [59]. The address of the device has to be set to '1010100' (see Fig. 4.13).

4.1.5 Clock Structure

To adapt an external reference clock signal, the GIMLI card is mounted on a GANDALF module (see section 4.1.3). The clock signal with the frequency f_{in} is transmitted to the clock distribution chip *MC100EP210S* (*U10*) which provides one copy to a *SI5326* (*U11*) clock synthesizer and jitter attenuator chip located on the GANDALF module and another copy to the DSP-FPGA (*U9*). Two more synchronous copies of this clock signal with the same frequency f_{in} are connected to the two mezzanine card sockets (*up*/*down*). On the AMC, these clock signals will be transferred to another *SI5326* clock synthesizer. Cleaning the jitter of the incoming clock signal is the main purpose of the *SI5326* clock synthesizers. The synthesized clock signals need to be synchronous to the incoming clock f_{in} and must have a TIE[19] below $\sigma_{TIE} < 5\,\text{ps}$ on the outputs of the *SI5326* chips over a large bandwidth from a few kHz up to 500 MHz. This makes the generation of synchronous clock signals with a programmable frequency in a range of up to $f_{SI} \approx 500\,\text{MHz}$ possible.

[18] The script is located in */sc/gandalf/board_configuration* and can also be downloaded from http://hadron.physik.uni-freiburg.de/gandalf

[19] Time Interval Error, is defined as a phase difference between the measured clock signal and an ideal reference clock.

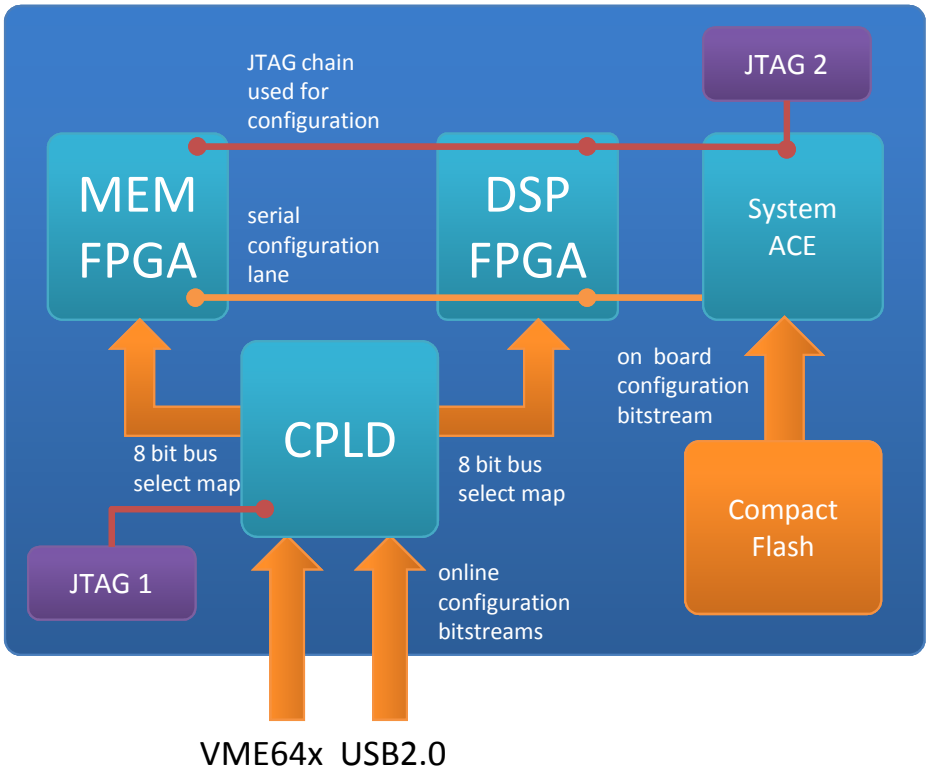


Figure 4.11: Schematic overview of the different FPGA configuration chains on the GANDALF module. The on-board FPGAs can be configured either via external interfaces (VME64x or USB2.0) or by reading the configuration data from the locally installed compact flash card. By using the external interfaces the data is written into the FPGAs by the CPLD using the 8 bit Select Map bus.

As long as all clock synthesizers are connected to the same clock source f_{in} via GIMLI modules, the clock outputs of the *SI5326* are synchronous, even across different GANDALF modules or AMCs (see Fig. 4.14, [77]). Verification measurements for the synchronous distribution of the clock signal over several GANDALF modules are given in section 5.2.2.
The clock synthesizer *SI5326* makes the jitter cleaning possible on the one hand and also is used for selecting the clock frequency for e.g. the sampling ADC mounted on the AMC. However, on the other hand it also provides the clock for the dedicated GTX transceiver clock inputs for the high speed link between the DSP and MEM-FPGA (*U9*, *U25*). For the operation of the Aurora link, described in section 4.1.8, a frequency of the order of $f_{GTXCLK} \approx 75\,\text{MHz}$ has to be provided by the *SI5326* on the GANDALF module.

Besides the input clock signal provided by the GIMLI mezzanine card, there are other non-synchronous clock sources used for devices like the USB interface, the *SytemACE*

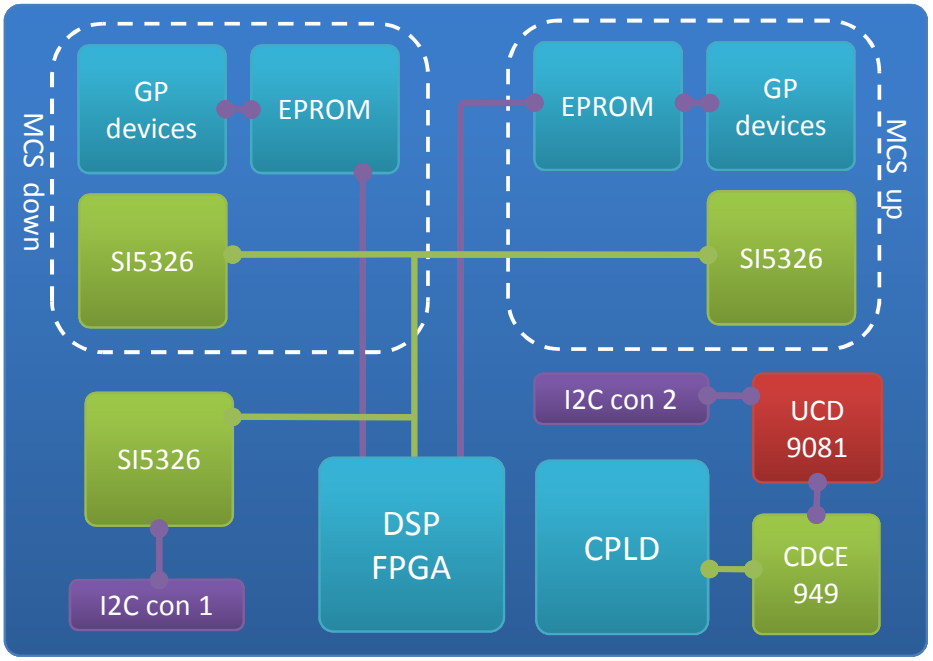


Figure 4.12: Schematic overview of the different I2C configuration chains on the GANDALF module. The green colored I2C bus lanes are for the configuration of clock generation devices. The violet I2C lanes are the general purpose buses. The DSP-FPGA is the bus master driven by the logic of the *SI IF VHDL* module and the *GP IF VHDL* module (see section 4.2.1).

configuration environment and switching converters. These clock signals are provided by a re-programmable *CDCE949* (*U14*) clock manager. A special treatment concerns the CPLD which receives a clock signal from the *CDCE949* and from an independent oscillator. The later provides a fixed frequency of $f_{OSC} = 40\,\text{MHz}$ [76]. The additional oscillator clock signal permits the communication with the GANDALF modules via the VME interface independently form the status of the clock chips on the GANDALF module.

4.1.6 Board Monitoring

The ability to monitor operation parameters to guarantee a stable operation of modules is important, when GANDALF modules are used in extended facilities like the COMPASS-II experiment. Hence, possibilities to monitor all important parameters like operational voltages and temperatures of individual chips and air flow have been realized in the design. As mentioned in section 4.1.3, the AMCs are an intense heat source due to the large power consumption of the pipelined sampling ADCs. Therefore, temperature sensors on the AMCs and on the GANDALF modules can be used to produce a helpful

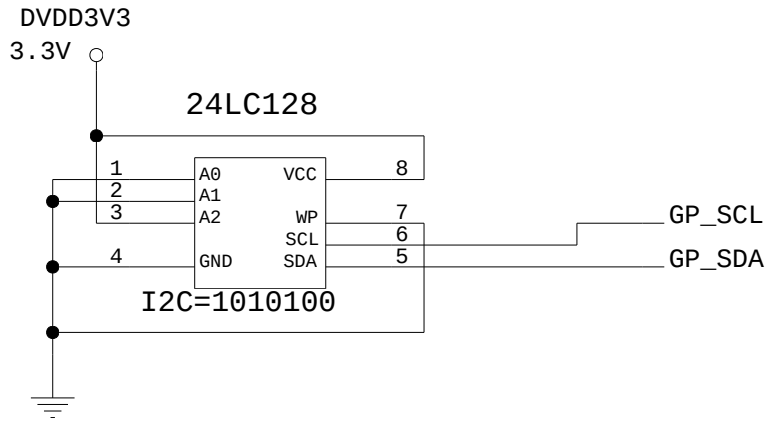


Figure 4.13: Schematic drawing for the 128k EEPROM (24LC128) located on any GANDALF framework mezzanine card [59]. A (*24LC128*) has to be chosen for any future mezzanine card designed for the GANDALF framework. The *GP_SCL* and *GP_SDA* signals must be connected to Pin11 and Pin13 of connector *J6* for mezzanine card socket *up* or *J8* for mezzanine card socket *down*. The termination of the *I2C* bus is located on the GANDALF module [53].

overview of the boards' status. In the following the different monitoring devices and their respective system parameters will be introduced.

- **Texas Instruments UCD9081:** To control and monitor most of the power rails available on the GANDALF module, the *UCD9081* (*U29*) was chosen. This device enables 8 different power rails in a programmable sequence and later monitors these rails. The monitoring data can be transmitted by an I2C bus with the CPLD (*U8*) or an external *I2C* controller connected to (*JP6*) as bus master. The monitor range of the *UCD9081* is 0.0 V to 2.5 V. Resistor networks are used to align the monitored voltages to this range. Further, the *UCD9081* may generate an alarm if the voltage of the power rails move outside a predefined voltage range. In this case an alarm flag is applied to the general purpose output Pin1 of the *UCD9081* device and the CPLD connected to this pin can take action. A table of the monitored voltages is given in Tab. 4.3 [75].

- **Xilinx SXT FPGA:** The Virtex-5 FPGA family includes a system monitoring core which is available on any chip and can be accessed from a VHDL module [78]. The system monitoring core permits to monitor the core voltages $VCC1V0$ and $VCCAUX$ and the die temperature of the FPGA. The resolution of the internal ADC inside the FPGA which is used for digitizing the voltage and temperature values, is 10 bit and operates with a sampling rate of $f_{ADC\_FPGA} = 10\,\text{Hz}$. The maximum and minimum of the monitored values are memorized, starting from the time of the last configuration of the FPGA. The system monitoring VHDL core which is sub ranged in the general purpose VHDL module (see section 4.2.1) is able

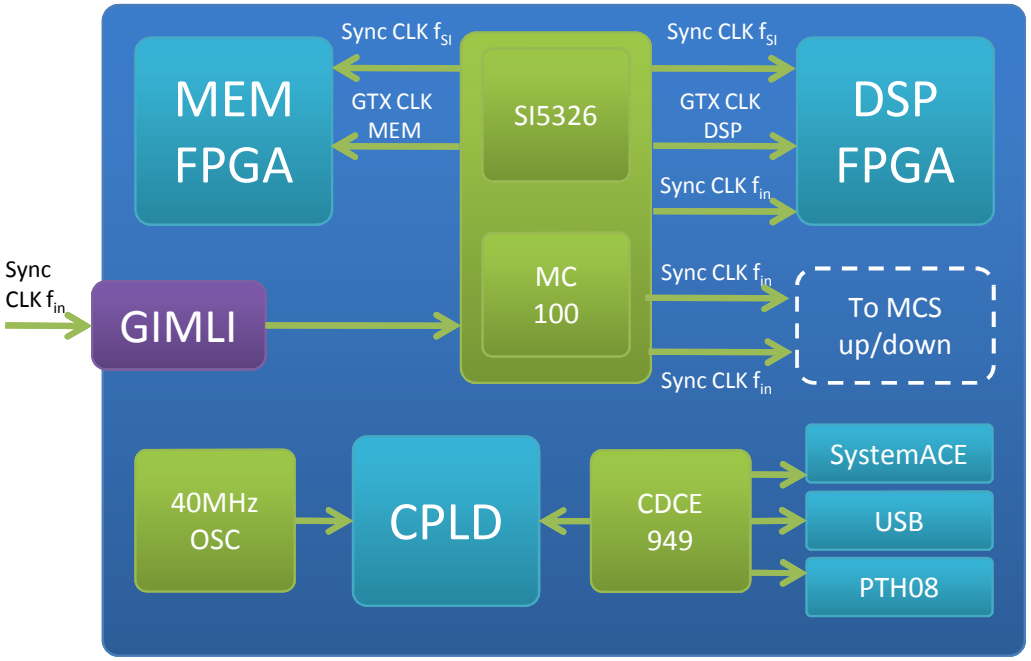


Figure 4.14: Schematic overview of the clock structure of the GANDALF module. The 40 MHz clock source is available to the CPLD in any setup of the GANDALF module to guarantee the communication via the VME interface. The *CDCE949* generates the clocks for the USB, SystemACE and FPGA communications [76]. The *Sync CLK* f_{in} given to the GIMLI card clock input is synthesized and distributed by the *SI5326* and *MC100EP210S* (in this Figure denoted by MC100) devices to generate *Sync CLK* f_{SI} and *GTX CLKs* [77, 61].

to access these information by toggling the *Fast Register* $[FR\_ADDR] = 0x014$ (please refer to section 4.2.2 for detailed information about the *Fast Registers*). Utilizing this feature, the available voltages at the FPGA and the die temperatures and the respective maximum and minimum values are read from the system monitoring core. These values are then written into the *Configuration Memory* to the registers $TEMP0$ (32), $VCCAUX0(32)$, $VCCINT0(32)$ in the data structure (see Tab. E.2):

$$'00' \;\&\; maxval(29 \;\ldots\; 20) \;\&\; minval(19 \;\ldots\; 10) \;\&\; value(9 \;\ldots\; 0)$$

To calculate the corresponding voltage or temperature information, one has to follow these equations [78]

$$U(\text{Volt}) = \frac{ADC\ code}{1024} \times 3.0 \tag{4.1}$$

Table 4.3: Voltage rails monitored by the *UCD9081*. If the monitored voltage extends the defined range, an error flag will be set by the *UCD9081*.

Rail	Net Name	Voltage	defined range	resistor network
1	VCC1V0	+1.0 V	± 0.05 V	N/A
2	VCC1V8	+1.8 V	± 0.05 V	N/A
3	VCC2V5	+2.5 V	± 0.10 V	3.3 kΩ/3.3 kΩ
4	VCA5V0	+5.0 V	± 0.10 V	20 kΩ/100 kΩ
5	VCA3V3	+3.3 V	± 0.10 V	3.3 kΩ/10 kΩ
6	VCC3V3	+3.3 V	± 0.10 V	3.3 kΩ/10 kΩ
7	VCCAUX	+2.5 V	± 0.10 V	3.3 kΩ/3.3 kΩ
8	VCC-12V	-12.0 V	± 0.20 V	10 kΩ/100 kΩ

and

$$T(^{\circ}C) = \frac{ADC\ code \times 503.975}{1024} - 273.15\ , \tag{4.2}$$

where the System Monitor is operational in the temperature range of -40 °C to +125 °C.

- **Texas Instruments TMP175:** Two $TMP175$ temperature sensors are placed on each ADC mezzanine to monitor the prevailing temperature on the AMC due to the power consumption of the ADCs. One is placed on the top side and the other on the bottom side of the PCB. This allows for a measurement of the temperature gradient between both mezzanine sockets *up* or *down*, respectively. The distance between the up and down sensors on each side is about 5 cm. The temperature sensors are connected to the general purpose $I2C$ bus and use the $I2C$ address '1001000' or '1001001' for the sensor on top or bottom, respectively. With the *Fast Register* command $[FR\_ADDR] = 0x010$, a temperature readout of all sensors on both AMCs is initiated and the returned values are written into the *Configuration Memory* registers: $TEMP0(32)$ for each AMC (see Tab. E.2). The register detail covers both temperature values: AMC_TMP_TOP (10) and AMC_TMP_BOT (10). The 10 bit information provided by the $TMP175$ is given in two's complement and can be calculated back to temperature value with [67]:

$$T(^{\circ}C) = ADCcode \times 0.25 \tag{4.3}$$

4.1.7 Memory Devices

There are two Virtex5 FPGAs located on the GANDALF module. First, the DSP-FPGA (*U9*), a member of the Virtex5 SXT family, has an increased number of DSP48E slices for fast calculations [79]. This allows for complex algorithm processing and powerful logic decisions. Second, the MEM-FPGA (*U25*), a member of the Virtex5 LXT

family, is providing additional cache memory with fast access to buffer intermediate calculation results. After the data processing, it is also important to own large output buffer capabilities to save the data locally on the GANDALF module before it is sent to the data acquisition system. This can also be handled by the MEM-FPGA connected to the DSP-FPGA via a high speed link to establish fast transfer for data buffering (see section 4.1.8).

This FPGA owns the functionality as a memory controller and also manages the data output to the data acquisition system using the S-LINK interface. As shown in Fig. 4.15, two types of RAMs are connected to this FPGA. The two *CY7C1515V18* QDRII[20] (*U18, U19*) memory devices have the functionality as cache for calculations with a depth of 144 MBit in total [80]. The broad dual port bus interface of 72 bit (36 bit for each memory device) provides write and read access at the same time with a very fast data throughput of 4.5 GByte/s. The bus can be driven with a frequency of up to 250 MHz double data rate. The used signal standard for the data transfer is HSTL[21].

The second type of RAM used with the MEM-FPGA are two *HYB18T2Gx02BF* DDR2 (*U18, U19*) devices. They share a common 8 bit bus with 250 MHz double data rate to read and write the output data [81]. The output memory can buffer up to 4 Gbit and has a data throughput of up to 500 MByte/s. The signal standard for the communication between the DDR2 RAM and MEM-FPGA is SSTL[22].

A simulation of the memory bus system is needed to guarantee the correct length matching of the memory lanes and to maintain signal integrity despite the high density of neighbored memory devices and MEM-FPGA. This has been performed in advance to the production of the PCB, verifying the signal integrity meets the memory signal standard specifications.
The MEM-FPGA is directly connected to the S-LINK interface and provides the data for the transmission to the readout buffers of the data acquisition system [46]. As shown in Fig. 4.15 an optional connection from the DSP-FPGA to the S-LINK interface provides a direct interface from the DSP-FPGA to the S-LINK. In both cases only one FPGA can access the S-LINK bus at a time while the output buffers of the other FPGA are set to high impedance.

4.1.8 FPGA Interconnection: The Aurora Link

The Virtex5 FPGA SXT and LXT family contain *Rocket IO GTP* Transceivers for high speed serial data transmission [82]. These cores are implemented in hardware and are adapted to the FPGA logic to permit serial data transmission with up to 3.125 Gbit/s per lane. There are 8 lanes in transmitting and 8 in receiving direction connected between the DSP-FPGA and MEM-FPGA. These lanes have a data throughput of 25 Gbit/s for each direction between the both FPGAs. The data protocol used for the high speed data

[20] Double Data Rate (DDR) combined with a Dual Port Memory is called Quad Data Rate (QDR). DDR: the data gets latched on the rising and falling edge of the clock signal; Dual Dort Memory: this type of memory has separate buses for data input or output.
[21] High Speed Transceiver Logic
[22] Stub Serial Terminated Logic

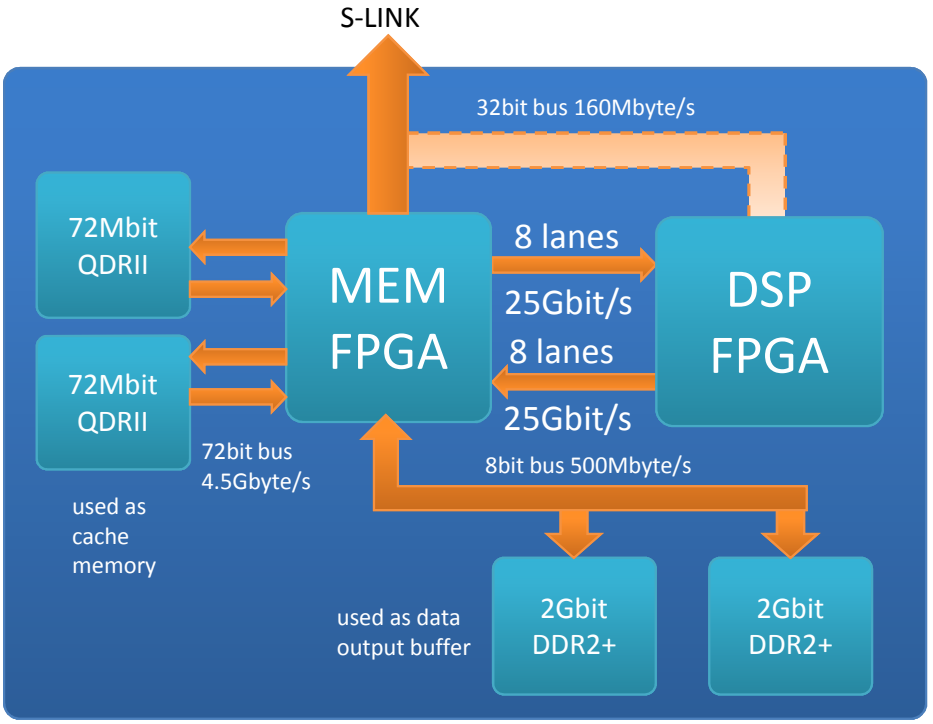


Figure 4.15: Schematic overview of the different memory devices. The QDRII devices possess a dual port access and can be used as fast cache memories. The deep 4 Gbit DDR2+ RAMs provide output buffer capabilities. Here the data can be stored before it is transmitted to the data acquisition system via the S-LINK interface.

transmission is the Aurora protocol [83]. It is an open source protocol and establishes FPGA-to-FPGA communication with constant data streams and unlimited frame sizes.

To use the link, the GTP units of both FPGAs need a separate low jitter clock signal which is provided by the on board *SI5326* clock synthesizer (see section 4.1.5, [77]). The high speed transmission used on the link also requires a separate low noise power supply which is performed by *TPS74801* LDOs[23] [84]. Beneath the strong constraints on the power supply and clock signals the additional routing constraints of the lanes have to be considered to prevent electrical reflections due to impedance inhomogeneities. Such may result in degraded signal integrity and can cause bit errors within the data transfer. The routing of the high speed bus only addresses the top layer *TOP* and the first signal layer of the PCB *SIG1* (see App. A.2). Both are impedance defined to the ground plane *GND1* which is staggered in between *TOP* and *SIG1*. The interconnections between the signal planes *TOP* and *SIG1* are realized with blind vias. Hence, reflections were minimized by not using vias which pass all other lanes for the interconnection and by using acres only for the routing of the lanes from the transmitting to the receiving pins

[23] Low Dropout Regulator

of the FPGA (see section 4.1.10 and Fig. 4.17). For these interconnections simulations have been performed prior to the PCB production to guarantee proper signal integrity on this high speed bus. These *HSPICE*[24] simulations include the electric characteristics of the Xilinx Vitrex-5 GTP tiles and the characteristics given by the impedance of the routed interconnection. Figure 4.18 shows the simulation results. It can be seen that the signal levels for a 3.125 GHz rate data transfer do not cross the "eye" which defines the minimum time and voltage distances needed between two valid state changes.

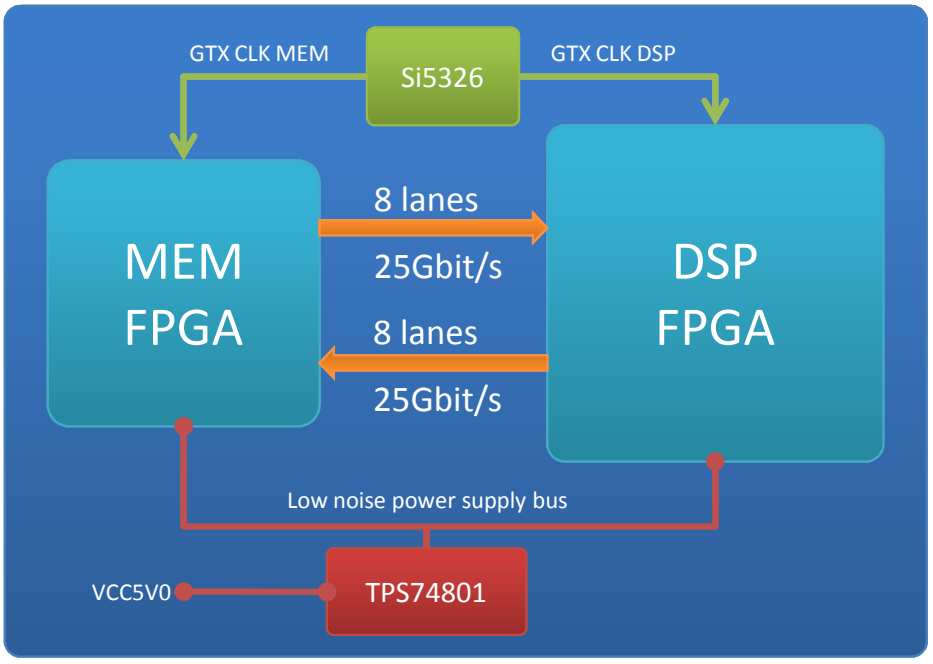


Figure 4.16: Schematic overview of the link between DSP and MEM-FPGA on the GANDALF module. There are 8 lanes for each direction between the two FPGAs. The dedicated clocks for the GTP tiles are generated by the *SI5326* clock synthesizer. The low noise low dropout regulator is supplied from the *VCC5V0* power net.

4.1.9 Power Supply

By using analog mezzanine cards with the GANDALF module, it has the functionality as a transient analyzer by sampling the incoming analog signals with a very high precision: 1 GS/s at a resolution of 12 bit. The Texas Instrument *ADS5463* sampling flash ADC was chosen for the design because it convinces with the high level of SNR and low THD at a large bandwidth. Due to the flash architecture, this ADC needs a certain amount of power (2.2 W) which is challenging for the power supply due to the

[24] High Speed Simulation Program with Integrated Circuit Emphasis

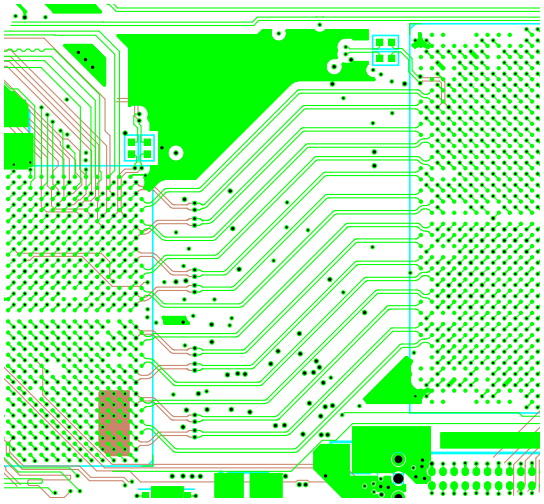


Figure 4.17: View of the routed signal lanes for the high speed Aurora Bus. The green coloured connections are located on the top layer (TOP) of the PCB, the brown connections on the third layer (*SIG1*) of the PCB. Please refer to App. A.1 for the detailed stackup description

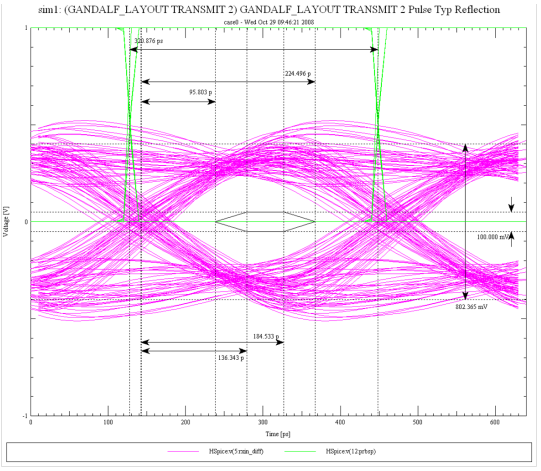


Figure 4.18: Results for the *HSPICE* simulation of the aurora lane circuit. The simulation takes the PCB layout and routing into account with data rates up to 3.125 GHz. The black "eye" gives the minimum distance in time and voltage to guarantee an error free data transmission from a transmitting to a receiving GTP tile [82].

dense number of channels realized on a GANDALF module. With up to 16 channels per module, a power consumption of 35.2 W for the ADC part only has to be taken into account. Summarizing all other devices a consumption of ≈ 80 W can be expected for one GANDALF module running with maximum functionality.

The main bottlenecks for the power transfer from the VME Crate Power Supply to an inserted VME module are the power connector pins. They tolerate a maximum current of $I_{pin} = 2A$ per pin. To reach the huge power transfer, the user voltages U1 and U2, which are defined with four additional power pins, are selected to +12 V for the use of GANDALF modules in VME64x/VXS Crates [49]. In this configuration four voltages are provided by the VME64x crates power supply: +12.0 V, +5.0 V, +3.3 V, −12.0 V (see Fig. 4.19). The *VCC+12VIN* net is only used to provide the power for the ADCs. Therefore, the corresponding voltage level is generated on the GANDALF module by two DC/DC converters *LTM4602* and *LTM4600* (*U50*, *U51*). They can provide a power of 20.0 W on the *VCA3V3* net and 50.0 W on the *VCA5V0* net. These two nets are connected to the analog power supply inputs of the ADCs via the mezzanine connectors. The *Texas Instruments ADS5463* needs an additional 3.3 V supply for the digital inputs; these are provided by the *VCC3V3* net which originates in the VME power supply as defined in the VITA1.1 VME64x specification [49].

Additional voltages, which are generated on the GANDALF module, are the supply voltages for the FPGAs and RAM devices. The *VCC+5VIN* is used to produce the $VCCINT = 1.0$ V core voltage for the FPGAs and the $VCC1V8 = 1.8$ V for the HSTL

and SSTL signal standards used for data transmission between memories and MEM-FPGA (see section 4.1.7). The *PTH08T220W* and *PTH08T230W* (*U38*, *U39*) can produce up to 16.0*W* and 10.0*W* power for the supply of the FPGAs and memories. These power values were obtained by simulations in advance to estimate the type of power devices to be included in the development of the module.

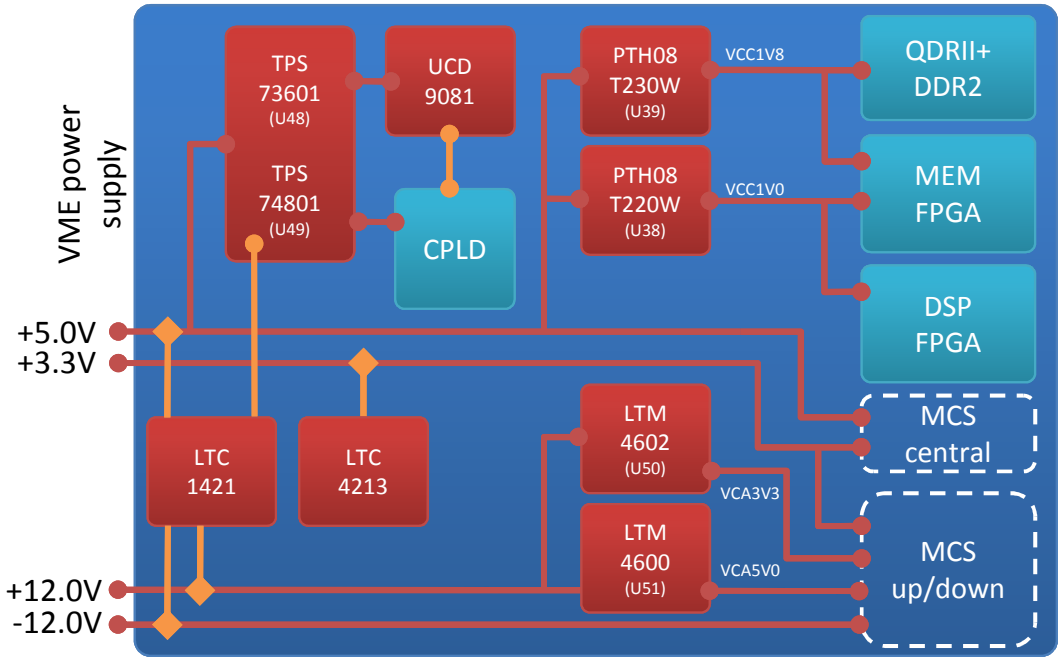


Figure 4.19: Schematic overview of the power supply nets on the GANDALF module. The orange squares symbolize the power MOSFETs used to enable the external power nets provided by the VME64x/VXS crate power supply. In the startup sequence the CPLD and *UCD9081* are switched on first. Then the *UCD9081* enables all remaining nets. For clearness not all 22 power nets on a GANDALF module are shown in this schematic.

After a GANDALF module is plugged into a VME64x/VXS crate payload slot and the switches inside the handles are closed the *LTC1421* Hot Swap Controller (*U27*) starts the power-up process [85]. During this procedure the Power MOSFETs[25] (symbolized in orange squares in Fig. 4.19) for the voltages +12.0 V, +5.0 V, +3.3 V, −12.0 V provided by the VME64x crate power supply are switched on by the Hot Swap Controller. The *LTC1421* ramps the +12.0 V, +5.0 V and −12.0 V up, and monitors the current on the +12.0 V, +5.0 V power rails during this process. The voltage of the −12.0 V is monitored by the *UCD9081* (*U29*). After a successful ramp up, the power supply for the CPLD (*U8*) and the *UCD9081* is enabled. From this state all other voltage rails can be enabled

[25] metal oxide semiconductor field-effect transistor

with programmable time delays using the output enable flags of the *UCD9081*. The external *VCC3V3* voltage rail, which is defined by the VITA1.1 VME64x specification is controlled by a *LTC4213* (*U47*) power sequencer chip [86]. The *LTC1421* and the *LTC4213* possesses the additional functionality as an electrical circuit breaker which monitors the current on the +12.0 V, +5.0 V, +3.3 V lanes and breaks the circuits by switching the dedicated MOSFETs off in case of over-currents.

There are two red LEDs located on the bottom side of the GANDALF PCB (*LED13*, *LED14*) signalizing if an over current situation has occurred. The −12.0 V lane is protected by a fast resettable fuse breaking at $I_{break} = 2\,\mathrm{A}$. All power input lanes from the VME64x crate power supply are additionally protected by slow safety fuses (*F37, F38, F39, F48*). The output buffers for the VME bus are enabled after the power up sequence of the GANDALF module has completed.
When switching off the module by turning the handles, the *UCD9081* gives an immediate power off signal to all power converters to avoid undefined power down schemes during the removal of the module.
For the sake of clarity, only some of the 22 different power nets on a GANDALF module were shown in Fig. 4.19. Additional power nets are e.g. the low noise power supplies for the GTP tiles inside the DSP and MEM-FPGA to establish the Aurora bus interface (see Fig. 4.16) or the reference voltages for the reference levels of HSTL or SSTL inputs.

4.1.10 PCB Layout

During the PCB layout process many constraints have to be considered: At first, it is important to guarantee the signal levels and integrity of up to 244 differential bus pairs which have to be interfaced from the mezzanine cards to the central DSP-FPGA (*U9*). They have to meet careful length matching constraints to satisfy the timing for the logic inputs. At second, a stable and low noise power supply to minimize the noise on the digitized data caused by coupled noise from the power supply must be realized.

To meet the signal integrity issues, the software package *Allegro 16.3* was used to route the interconnections and simultaneously control the signal integrity by using *SPICE*[26] simulations [87]. To set up such a simulation environment, a feasible stack-up for the PCB has to be chosen first. Many different factors are important to select from various stack-up combinations. The total maximum width of the PCB has to be taken into account with the signal density reached in certain areas. This defines the number of signal layers. The highest density is reached on the PCB for the GANDALF module next to the DSP-FPGA package where, among others, the 244 differential strip lines from the mezzanines are connected to the FPGA fan-out in an area of $10,2\,\mathrm{cm}^2$. A noise reducing 18 layer PCB stack-up was defined to realize the high density routing (see App. A.2).

Another constraint to reach satisfactory signal integrity is the impedance of each signal pair. This has to be $Z = 100\,\Omega \pm 5\%$ for the given *LVDS*[27] signal standard. To reach this value, the width of each strip line, the spacing between the two strip lines creating a differential pair, and the distance to the dedicated ground plane to the differential pair

[26] Simulation Program with Integrated Circuit Emphasis
[27] Low Voltage Differential Signaling

has to be chosen correctly. This defines the total width of a single plane. Changes of these parameters must allow to stack up the given number of signal and ground planes without exceeding the limit of the maximum PCB width of $d = 1.6\,\text{mm}$. The calculation for the impedances includes the dielectric constant of the preimpregnated fiber material (FR4[28]) which is used as PCB spacing material. An impedance of $Z = 100\,\Omega \pm 5\%$ for the differential pairs is reached on all layers except the top and bottom layer of the GANDALF module PCB, with a strip line width of $w = 100\,\mu\text{m}$ and a spacing of $s = 200\mu m$. For the distance between a signal layer and ground layer distance of $h = 100\,\mu\text{m}$ was chosen (see Fig. 4.20). The thickness for the top and bottom layers differs due to the production process (thickness top/bottom layer: $d \approx 40\,\mu\text{m}$, thickness inner layers: $d \approx 17\,\mu\text{m}$) and also the dielectric constant differs on the top layer from the internal PCB spacing material due to the soldermask material (solder mask: thickness $d = 40\,\mu\text{m}$, $\epsilon_r = 3.0$, preimpregnated fibers: thickness $d = 100\,\mu\text{m}$, $\epsilon_r = 4.5$). This concludes in a spacing of $300\,\mu\text{m}$ between the differential pairs routed on top or bottom layer.

In some specific situations the spacing between the differential pairs has to be changed to be able to pass a dense mesh of vias. This occurs for example while routing the signals to the input pins of the DSP-FPGA. The SX95T FPGA uses a $FF1136$ package with 1136 pins and a 1 mm pitch [48]. The vias which are used to interconnect different layers have a diameter of $200\,\mu\text{m}$ and a $400\,\mu\text{m}$ pad diameter and need safety spacing to the neighboring strip lines of $250\,\mu\text{m}$. These constraints exclude the routing of a differential pair with a total width of $400\,\mu\text{m}$ in between. In these extreme cases the routing is performed in neck mode which reduces the impedance by less than 3% but still reaches the input pins without separating the signals around the placed vias. In neck mode the strip line width is reduced to $90\,\mu\text{m}$ and the spacing between two pairs is $120\,\mu\text{m}$. An example for signals routed in neck mode is given in Fig. 4.21. It shows the differential signal pair bus, arriving the DSP-FPGA on the bottom layer of the PCB.

For single ended strip lines an impedance of $50\,\Omega$ is reached with choosing a width of $100\,\mu\text{m}$. All single ended strip lines are routed next to a ground plane enabling back-flow currents to use the shortest distance between signal source and target.

As mentioned before, a main challenge in the board layout is the routing of the large number of differential pairs below the DSP-FPGA package. A helpful technique which is used to simplify this task is to use blind vias. Due to the placement of the FPGA device on the top layer of the PCB, all signals which should be connected to the FPGA pins finally have to be routed to the top layer. The signals reach the region below the FPGA package on any of the remaining seven signal layers and, therefore, a through via from any of these layers to the top layer has to be placed below the FPGA. Such a placed through via, to establish the connection from e.g. the bottom layer to the top layer, prevents a routing of signal strip lines on all remaining layers in its area following the minimum spacing constraints. Hence a mesh of 1136 through vias complicates the routing to the inner pins.

Blind vias, compared to the through vias, do not cross through all layers of the PCB, but only from the e.g. top layer to the first or second following one (see Fig. 4.22). Such

[28] Specification for flame resistant fiberglass expoy laminate

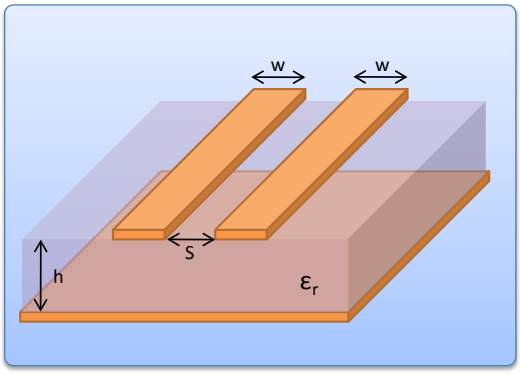


Figure 4.20: Schematic view of a micro strip differential pair. Where s is the spacing, w the width of one copper strip line and h the height of the dielectric with dielectric constant ϵ_r.

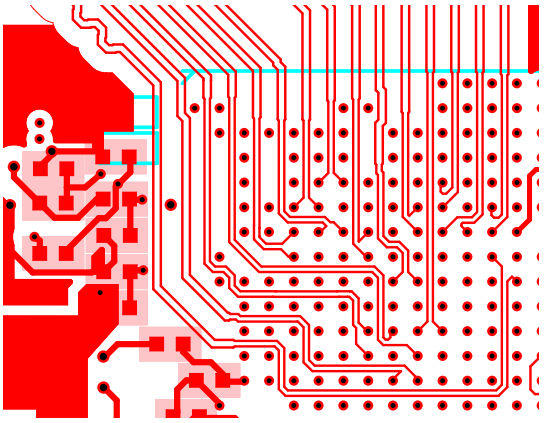


Figure 4.21: This Figure of the bottom layer of the GANDALF PCB gives an example for the routing of differential pairs in neck mode. To be able to pass the mesh of vias the spacing and width of the differential pairs is changed by keeping the change of the impedance of the signal pair below 3%.

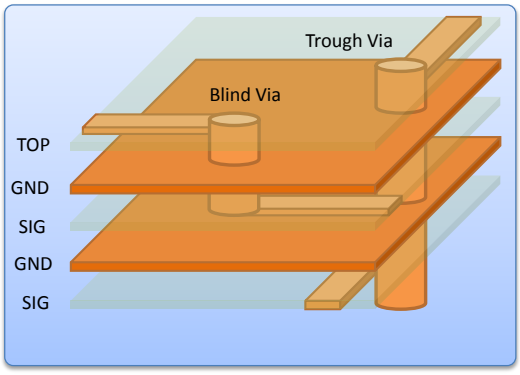


Figure 4.22: Schematic view of a through via and a blind via. A through via passes all layers of the PCB and it interconnects from any to any layer. A blind via only connects all layers between the top level and a layer in the PCB. The depth of the via is defined by the "aspect ratio" between width and depth of the via (1 : 1). On layers below a blind via routing can be performed independently to the location of the via.

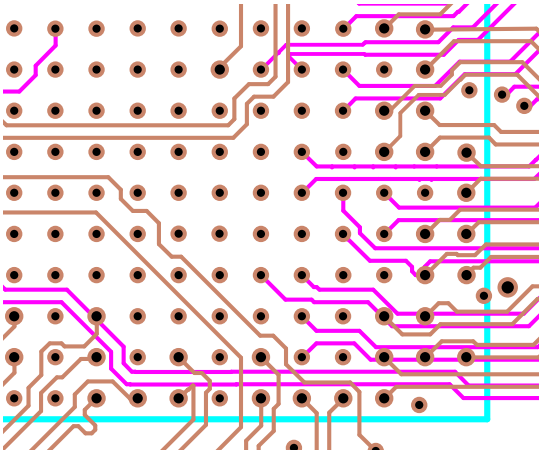


Figure 4.23: An example for blind vias used to connect from layer SIG2 (brown lanes) to the top layer (not shown). Signals from other layers (here for example SIG7 in magenta) can be routed independently from the placed blind vias (lower right part of the Figure).

vias are used on the GANDALF module PCB to interconnect strip lines routed on the layer SIG2 to the FPGA pins. Due to PCB production constraints, blind vias can only be drilled with a given aspect ratio of 1 to 1 in diameter to depth. Therefore, the SIG2 layer was the only one which can be addressed using blind vias. The drill diameter of the used blind vias is 250 μm compared to 200 μm for the through vias.
An example on how this technique helps to simplify the routing process is shown in Fig. 4.23. The brown colored signal strip lines are routed on layer SIG 2 and blind vias for the interconnection to the top layer are used. The magenta colored signals on layer SIG7 can pass directly below the placed blind vias (lower right corner of Fig. 4.23). Therefore, it is possible to reach much higher routing density on the layers SIG3, SIG4, SIG5, SIG6, SIG7 and the bottom layer, despite the used via from SIG2 to the top layer.

A further challenge for the PCB layout of the GANDALF module is the power distribution for the main power consumptive parts on the GANDALF module; these are both FPGAs and the ADCs if AMCs are mounted. In the following, the net *VCCINT* will be used as an example for the routing procedure of these power supply planes which interconnect the current sources (DC/DC converters) with the sinks (the FPGAs) of a power net. This net provides the $VCCINT = +1.0\,\mathrm{V}$ internal voltage for both FPGAs, the DSP (*U9*) and the MEM-FPGA (*U25*). The simulation tool XPower provided by *Xilinx Inc.*, estimates the power consumption for each FPGA under the given design constraints. This tool was used to calculate the maximum amount of current which has to be provided on the net *VCCINT* if the FPGAs operates at maximum performance and usage.

The power net *VCCINT* is routed first from the top layer where it is connected with the power output pin of the *PTH08T220W* (*U38*), thereafter, the net is routed in a plane on layer VCC2 (see App. A.10). Due to the 14 layer stackup of the PCB, the thickness of this plane is 17 μm (see App. A.2). With such a thin layer, the resistance of the power plane has to be taken into account due to the conductivity and the expected current. Through the resistance of the power plane a voltage drop from the source to the sinks (here the both FPGAs) is expected. The *PTH08T220W* features low current sense inputs which are separately routed to the sinks of the power plane, and readjusts the output voltage to +1.0 V measured on this sense input. Concerning the voltage drop U_{drop} over the power plane, the voltage on the power outputs of the *PTH08T220W* is $U_{out} = +1.0V + U_{drop}$. The shape of the power plane and, therewith, the resistance of the plane is defined that U_{drop} is below 50 mV. The voltage drop behavior on the two dimensional plane can be simulated and solved with the finite element method using the *IDrop Sim* software package provided with the *PCB editor* by *Cadence Inc.*. A simulation result for the *VCCINT* plane is given in Fig. 4.24.

Another factor which comes with high currents in thin power planes is the energy deposition and, therewith, the temperature increase T_{inc} of the power plane. The *IDrop Sim* also simulates the temperature increase due to current flow and resistance, depending on the shape of the power planes (Fig. 4.25). The shape of the *VCCINT* plane was designed to prevent a temperature increase T_{inc} of more than $+2.0°C$. All 22 power nets implemented on the GANDALF module where simulated and evaluated prior to production to keep voltage drops below 50 mV and temperature increases due to current flows below $+2.0°C$.

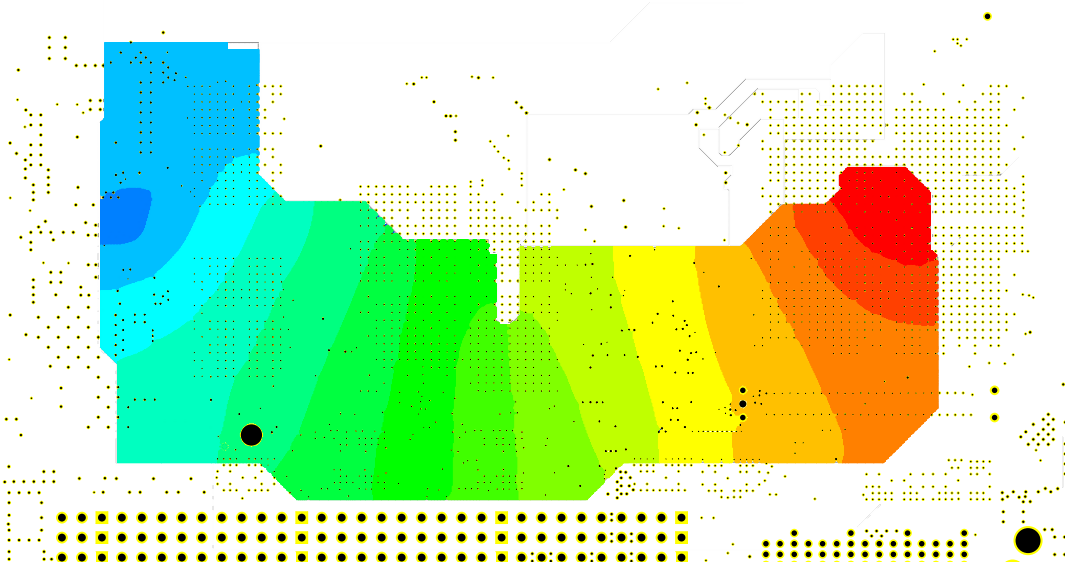


Figure 4.24: This Figure shows the two dimensional drop of the voltage U_{drop} for the power plane *VCCINT* in relation to the power source (*U38*). In blue regions the voltage is dropped by 2 mV, in red regions 45 mV.

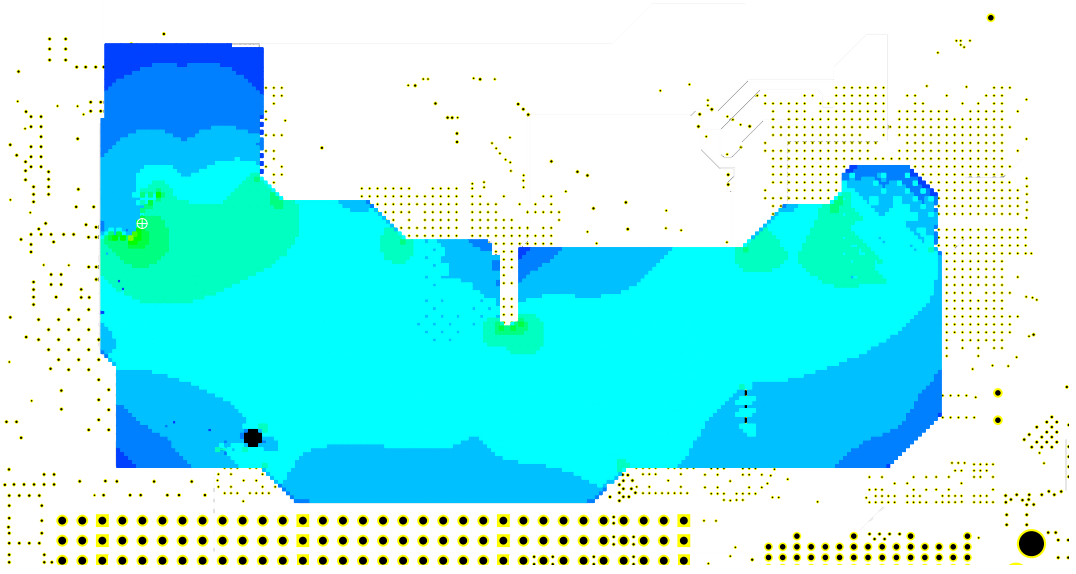


Figure 4.25: This Figure shows the two dimensional temperature increase T_{inc} for the power plane *VCCINT* relatively to the surrounding temperature. In blue regions the temperature is increased by $+0.05°C$, in green regions by $+1.5°C$.

4.1.11 JTAG: Electronic Verification

In the production of modules of such high complexity as it is realized for the GANDALF module it is absolutely necessary to provide a test environment to identify possible errors during the production of the PCB or the assembly of the electronic components. The shape of BGA[29] packages and the utilization of blind vias do not allow to reach same signal strip lines externally for debugging purpose. Therefore, the *IEEE-1149.1* Standard Test Access Port and Boundary-Scan Architecture, also known as JTAG[30], is implemented with the GANDALF module [62].

The JTAG test mainly covers device to device interconnection checks and low level logic functionality. An advantage of the test is that not any device has to meet the JTAG specification to test an intra-connection, as also passive reactions of the non-JTAG devices is needed to perform the test sequence. The required components inside a JTAG device for an intra-connection test like boundary-scan cells and serial interface are implemented in some of the logic devices used on the GANDALF module. These are the Xilinx devices: the DSP and MEM-FPGAs (*U9, U25*), the CPLD (*U8*), the SystemACE device (*U7*) and also the QDRII+ memory devices (*U18, U19*) [80]. They are connected to three JTAG chains as described in Fig. 4.26. Adapted to the core power supplies of these devices the chains *JTAG1* and *JTAG3* use the 1.8 V standard and the *JTAG2* the 3.3 V standard.

A test procedure which covers different tests from intra-connections (74% net coverage) and low level logic tests of devices, like the DDR2 RAMs, the display and the LED tests were implemented using the ProVision[31] software environment [88]. The chains *JTAG1* and *JTAG2* are used for the configuration of the CPLD and the FPGAs, respectively. With the chain *JTAG2* it is also possible to read monitoring data from the System Monitoring (see section 4.1.6) implemented inside the Virtex5 FPGAs.

4.1.12 GANDALF portable

The GANDALF module is designed to meet the ANSI/Vita 41.0 (VXS) specification [51] and, therefore, it can be used in different crate generations covering corresponding VXS crates with the high speed serial star type backplane bus. If the functionality of the VXS interface is not needed, it can also be operated with VME64x crates.
In some applications with a marginal number of channels, e.g. less than 16 analog readout or less than 128 digital channels, only a single GANDALF module can be used. In such cases the operation of a VXS or VME crate covering up to 20 modules can be inefficient. Therefore, the GANDALF portable environment was designed for mobility, installation and commissioning of local data acquisitions with a single GANDALF module (see Fig. 4.27) .
The designed cover for the GANDALF portable can house one single GANDALF module together with a power supply. For the housing a *RiCase* by manufactured *Rittal GmbH*

[29] Ball Grid Array
[30] Joint Test Action Group
[31] JTAG technologies Inc.

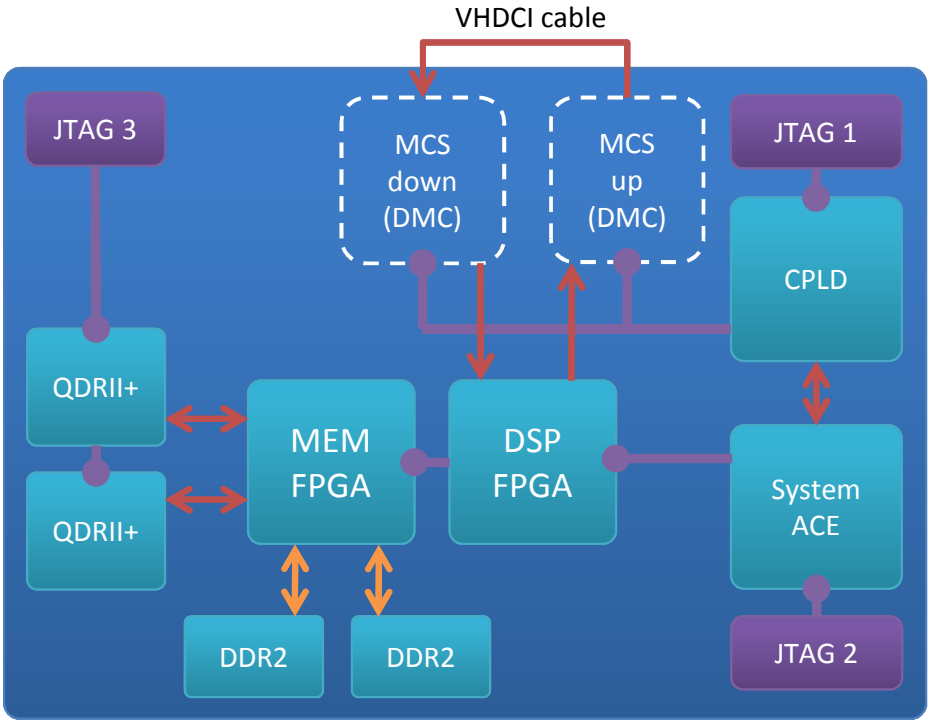


Figure 4.26: Schematic overview of the JTAG structure of the GANDALF module. Connections symbolized by red arrows are testable by intra JTAG tests between different JTAG chains. Connections symbolized by orange arrows are testable by passive JTAG tests where only one device is connected to a JTAG chain. Interconnections between parts which are members of the same JTAG chain are not drawn.
By mounting a DMC with outputs and a DMC with inputs to the mezzanine card sockets (MCS in this figure) an interconnection test can be performed with the DSP-FPGA. Therefore VHDCI cables connect the DMC on MCS up with the one on MCS down.

was chosen to assemble the GANDALF module together with the *SS-250SU* power supply unit [89]. The power supply unit is connected to the GANDALF module via small backplane power connector cards. An Ethernet interface card can be mounted to the transition connector of the GANDALF module for fast data connection to a remote computer.
For the data readout with the GANDALF portable, the USB2.0 interface can be used with a desktop computer. For such the GANDALF module USB driver and the *USBToolbox* for data acquisition have to be installed on the readout PC (see section 4.2.4).

Figure 4.27: Picture of the GANDALF portable. A GANDALF module can be installed into this environment for the operation of a single module. Any combination of mezzanine cards can be mounted to the GANDALF module.

4.2 Software

4.2.1 GANDALF VHDL Simulation Environment

The development of an electronic readout system with a high level of complexity is demanding a simulation environment where the functionality of the used algorithms and its parameters can be evaluated a priori. A simulation of the surrounding electronic devices which are connected to the *device under test* is important to check the I/O response.

The descriptive language for the programming of the FPGA firmware of GANDALF is VHDL[32]. The VHDL language has the opportunity to cover both: One can generate a code, implementable in FPGA hardware, which describes the algorithms e.g. the waveform analysis. Additionally the language has the capability to generate a complex simulation environment to test and verify the FPGA firmware. Therefore the devices like clock synthesizer, the sampling ADCs and the CPLD, connected to the DSP FPGA can be easily simulated within VHDL modules.

An overview of the generated VHDL modules is given in Fig. 4.28. The test bench for simulation includes the VHDL module programmed for implementation inside the

[32] **V**ery High-Speed Integrated Circuits **H**ardware **D**escription **L**anguage

FPGA (red box in Fig. 4.28). This code can be compiled for implementation and is the firmware used inside the FPGA. It includes a functionality dependent VHDL module (green box). In the case the GANDALF module is used as a *transient analyzer* this part performs the data readout from the AMCs and the waveform analysis.

The other VHDL modules located in the implementation part are common and needed for the board communication and operation (orange boxes). They are implemented in any GANDALF firmware. The *TCS IF* module enables the trigger and clock management with the data received from a GIMLI card. The *VME CPLD IF* module establishes the communication between the GANDALF module and the USB2.0 or the VME host PC. The *S-LINK* module describes the connection to the S-LINK source card. The clock synthesizer chip programming and the general purpose I2C bus communication is implemented in VHDL modules, too. All modules in 4.28 represented by orange colors are common modules which need to be included in any other firmware for board operation.

If all interfaces and functionalities surrounding the VHDL code for FPGA implementation are described, a simulation of the functionality of the FPGA logic is possible. The VHDL language has extended capabilities for the description of parts for simulation only. These VHDL modules are not designed to be implemented inside FPGA logic, but cab be used to describe the physical behavior of parts interfaced to the FPGA. The *pulse generation* module e.g. includes the mathematical description of pulse shapes and their digitization. This virtually generated and digitized data can, be transferred to the waveform analysis core to test the functionality of the algorithm (violet box in Fig. 4.28). To complete the test simulation environment, the trigger and clock generation performed by the *TCS controller* was implemented for simulation. The *Data Acquisition* VHDL module accepts the generated data and stores data in the COMPASS data format (see section F.1). Thus the simulated data can be directly processed with the same data decoding tools which are used in the real experimental setup. For the simulation of the GANDALF module VHDL test-bench, the *ModelSim SE 6.4a* software package was used [90].

4.2.2 VME CPLD Interface

The VME or USB2.0 interfaces can be used to communicate with a GANDALF module for configuration, monitoring, data readout and command execution. The logic unit which establishes the connection between the interfaces and the central DSP-FPGA (*U9*) is the CPLD (U8). This type of device was chosen to benefit from the non-volatile logic which is active directly after the power-up of the module. The CPLD has to be programmed only once at initial commissioning and needs no additional bit-stream file for operation.

For communication with the DSP-FPGA from one of the interfaces, VME or USB2.0, a generic VHDL module was created which has to be included in any VHDL project to be operated inside the DSP-FPGA[33]. After the configuration of the DSP-FPGA (see section 4.1.4) with a bitstream file, which includes the VME CPLD interface, *VME*

[33]The firmware for the VME CPLD interface can be found at http://hadron.physik.uni-freiburg.de/gandalf

commands and data can directly be addressed to VHDL modules used within the DSP-FPGA firmware.
The VME CPLD interface covers the allocation and control of the *Configuration Memory* (see section 4.2.3), the clock infrastructure, the *Fast Register* commands, the general reset logic and the *Spy FIFO*. A short overview of these parts will be given below:

- **Clock Infrastructure:** For a high data transfer rate between CPLD and DSP-FPGA, the read and write cycles for the *RAMB36* unit used for *Configuration Memory* are performed at a five times higher frequency than the bus communication. Therefore a 120 MHz and 240 MHz clock signal is needed. This is solved by converting the 40 MHz clock signal provided by the *CDCE949* (*U14*) using FPGA internal PLLs.
  The usage of the *IODELAY* units located at any differential pair from the mezzanine sockets needs the instantiation of *IDELAYCTRL* units (see section 4.1.2, [48]). The *IODELAY* units are mandatory to reach the timing constraints due to the difference in length of the 244 differential input pairs from the mezzanine socket. To operate the *IODELAY*s properly a clock signal with $f_{IODELAY} = 200\,\text{MHz}$ has to be connected to the *IDELAYCTRL* unit.

- **Reset Logic:** Three levels of generic resets are provided by this VHDL module. The triggers for the first and second reset signal are based on the lock status of the PLLs used for the clock generation mentioned above. The third reset signal is triggered by a successful startup of the S-LINK interface.

- **Fast Register:** To set flag signals or trigger logic sequences and operations inside the DSP-FPGA, e.g. the configuration of the *SI5326* clock synthesizer chip, the *Fast Registers* were implemented into the CPLD VME interface. A *Fast Register* can be interpreted as an active signal which can be set to three states: constant '0', constant '1' or a '1' pulse with a width of one clock cycle of the 40 MHz clock signal provided by the *CDCE949*. The *VME command* to access the *Fast Registers* is:

  $$\#> ./vme\_write\ E0[HEXID(8)][GADDRESS(16)]\ \ [PULSE\_TYPE(4)],$$

  where

  $$[GADDRESS(16)] = [CMD\_SEL(4)][FR\_ADDR(12)],$$

  and $[HEXID(8)]$ is the selectable module address which can be changed using the DIP switches (*SW1*, *SW2*, see Fig. 4.3). $[CMD\_SEL(4)]$ covers the command for the GANDALF module and has to be *0x7* to activate the *Fast Register*. [FR_ADDR(12)] selects the *Fast Register* address. With the $[PULSE\_TYPE(4)]$, the type of *Fast Register* can be defined: *0x0* sets the *Fast Register* to '0', *0x1* sets the *Fast Register* to '1' and *0x2* generates a pulse with a width of one clock cycle (see Tab. E.2).

- **Spy FIFO:** This FIFO is implemented in the CPLD VME interface to derandomize the data for readout via the VME or the USB2.0 interface. A copy of all data sent to the *S-LINK* interface is written into this 32k deep FIFO. The data words in the FIFO can be requested by using the *VME command*:

$$\#> ./vme\_write\ E0[HEXID(8)]3000$$

  This returns the first valid 32 bit data word stored in the output of the *Spy FIFO* (see Tab. E.1).

4.2.3 Configuration Memory

The modularity of the GANDALF module makes the operation in a variety of different application fields possible e.g. as a fast analog sampler, TDC or data acquisition module. Therewith come registers which can be set for a flexible configuration of the module. A 32 bit wide and 1024 deep RAM (*RAMB36*, [48]) is instanced in the VME CPLD interface (see section 4.2.2) to access these registers via the VME or the USB2.0 interfaces (see section 4.1.1). This memory can directly be accessed by the VME interface using the *VME commands* as explained in section 4.1.1. A subgroup *[CFMEM_ADDR(12)]* of the VME address range is reserved for the *Configuration Memory*. The 1024 *Configuration Memory* registers have a width of 32 bit and can be addressed with the following *VME command*:

$$\#> ./vme\_write\ E0[HEXID(8)][GADDRESS(16)]\ \ [DATAWORD(32)],$$

where

$$[GADDRESS(16)] = [CMD\_SEL(4)][CFMEM\_ADDR(12)],$$

and $[HEXID(8)]$ is the selectable module address which can be changed using the DIP switches (*SW1*, *SW2*, see Fig. 4.3), $[CMD\_SEL(4)]$ covers the command for the GANDALF module and has to be *0x2* for communication with the *Configuration Memory*. $[CFMEM\_ADDR(12)]$ is the "VME address" mapped to the *Configuration Memory* and $[DATAWORD(32)]$ can obtain the data which has to be written to the selected *Configuration Memory* address. If no $[DATAWORD(32)]$ is set, the corresponding word from the *Configuration Memory* is read and returned by the *VME command* script.
The *Configuration Memory* is separated in three register subgroups. Two of the subgroups with a depth of 256×32 bit register words, are reserved for the status information and configuration registers concerning the mounted mezzanine cards. A third subgroup with a depth of 512×32 bit register words is reserved for the GANDALF module itself (see Tab. E.3).

There are configuration registers of identical types like serial number, measured temperature values, which are used with both, the mezzanine cards and the GANDALF

module. They are combined into address subgroups. Hence these values are located on the same *[CFMEM_SUBADDR(12)]* with a defined address offset ($SUBGRP\_OFFSET$) of *0x000* for the mezzanine located in mezzanine card socket *up*, *0x400* for the mezzanine located in mezzanine card socket *down* and *0x800* for the GANDALF module.
The temperatures measured on the GANDALF module, for example, are located on *[CFMEM_SUBADDR(12)] = 0x040*. Then, the addresses for the temperatures measured on the AMCs are *0x040* and *0x440*, the address for temperatures measured with the SystemMonitor on the GANDALF module is *0x840* (see Tab. E.1).
To address the registers of the memory from the FPGA logic, the mapping of the RAMB36 is used, which differs from the VME address range. To calculate the address offsets, the following rule is used:

$$\begin{aligned}[RAMB36\_ADDR(12)] \times 4 &= [CFMEM\_ADDR(12)] \\ &= [CFMEM\_SUBADDR(12)] + SUBGRP\_OFFSET.\end{aligned}$$

Where $[RAMB36\_ADDR(12)]$ is the address value for RAM access from the FPGA internal VHDL code with a range of *0x3FF*, [CFMEM_ADDR(12)] has a range of *0xFFF* and [CFMEM_SUBADDR(12)] has a range of *0x3FF* for the mezzanines subgroups and *0x7FF* for the GANDALF subgroup. It has to be noted that the VME address structure only uses any fourth valid address in VME32 mode [49].

As any mezzanine card designed for the GANDALF framework contains a *24LC128* EEPROM connected to the GP I2C chain, the subgroup registers of the corresponding mezzanine are imaged there (see section 4.1.4, [59]). After a power up of the GANDALF module, an image of the EEPROM content is saved in the subgroup *Configuration Memory* registers, after toggling the *Fast Register* command on address $[FR\_ADDR] = 0x018$ and $0x020$ (see Tab. E.2). Now the GANDALF FPGA firmware has access to the individual data of any mezzanine stored in the EEPROM like serial number or card specific settings. If changes have to be done on these registers, it is performed by changing the values in the *Configuration Memory* by using the *VME command* mentioned above. After this modification, the complete subgroup registers in the *Configuration Memory* can be written to the EEPROM by toggling the *Fast Register* command on address $[FR\_ADDR] = 0x01C$ and $0x024$. This data will be preserved on the EEPROMs after a power cycle.

The monitoring data, which includes the temperatures and voltages measured by the DSP-FPGA, and the temperature values measured on the AMCs are written into the *Configuration Memory* and can be updated via the *Fast Register* command $[FR\_ADDR] = 0x010$. This monitoring data, located in the *Configuration Memory* registers, can be accessed by monitoring software like *Eye of Sauron* or *USB Toolbox* (see section 4.2.4). A table of all *Fast Register* commands and their description can be found in Tab. E.2. The complete *Configuration Memory* register map[34] is given in Tab. E.3.

[34] Refer also to http://hadron.physik.uni-freiburg.de/gandalf for updates

4.2.4 Additional Software

- **Eye of Sauron:** This software tool might be used to control, monitor and configure GANDALF modules located in a VME crate [91]. There are two communication paths used by the software. For crate environment communications like power supply voltages and currents, speed of the cooling fans and crate remote control functions are performed via SNMP[35] [92]. For communication with the GANDALF modules the VME backplane and a VME CPU as bus master located in slot 1 of the VME crate are used as physics layer.

  The Eye of Sauron software tool offers *VME commands* to realize a GUI-based configuration of the FPGAs, programming of the EEPROM contents of the mezzanine cards or to visualize the board locations inside the VME crate (see Fig. 4.29). A simultaneous broadcast to selected GANDALF modules in parallel can also be performed with this user interface.

  The software can also be used to controls the crate air temperature by regulating the fan speeds of the fans located below the GANDALF modules. In the *monitoring mode* the software reads all possible monitoring data from the GANDALF modules inside the crate. Temperature and voltage profiles can be displayed from the monitoring data stored in a MySQL database automatically.

- **USB Toolbox:** To access a GANDALF module which is not connected to a VME backplane, this software tool establishes an USB2.0 interface to perform communication and data readout [60]. The USB driver provided with the *CY7C68001* EZ-USB SX2^{TM}High-Speed USB Interface Device (*U24*) is used for communication [57]. The USB Toolbox offers a GUI which provides an overview of the GANDALF modules connected to the host PC via the USB2.0 interface. After selecting a dedicated module, connected to the USB host, it is possible to configure the FPGAs and, afterwards, to load general configuration registers into the *Configuration Memory*.

  To perform data readout with the GANDALF module, artificial BOS[36] and EOS[37] signals are sent to the GANDALF module via *Fast Register* commands when starting or stopping the acquisition. The data complies with the COMPASS data format [73].
  The USB Toolbox also offers online analysis of the recorded data. Histograms over the measured amplitudes, integral values, hit-rates and measurement results of the time-of-flight between selectable channels are possible.

[35] Simple Network Management Protocol
[36] Begin of Spill
[37] End of Spill

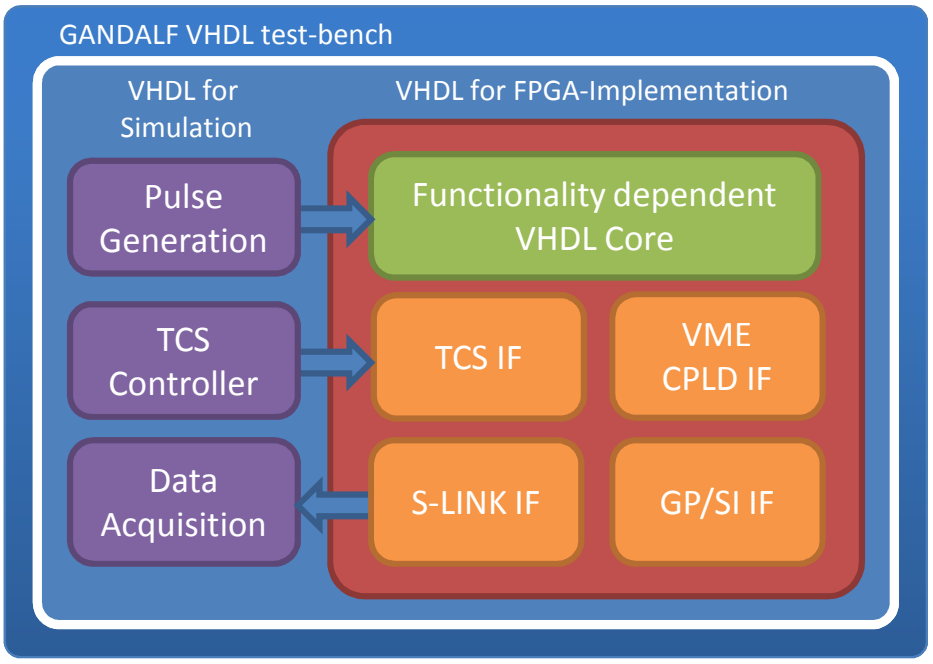


Figure 4.28: Schematic overview of the VHDL software simulation environment. The red box symbolizes the VHDL module for implementation inside the DSP-FPGA. It includes the functionality dependent VHDL core (green box). This can be the readout mechanism for the ADCs and the waveform analyzing algorithm. This part changes in dependency on the mounted mezzanine card or the functionality. The orange boxes symbolize the VHDL modules which are used in any design. They include the *TCS IF* for trigger and clock management, the VME *CPLD IF* for external communication (see section 4.2.2), *GP/SI IF* for the configuration of the *SI3526* clock synthesizer and other general purpose devices, and the *S-LINK* interface for data readout. The violet-colored boxes are pieces of VHDL code to simulate signal generation and I/O functionalities.

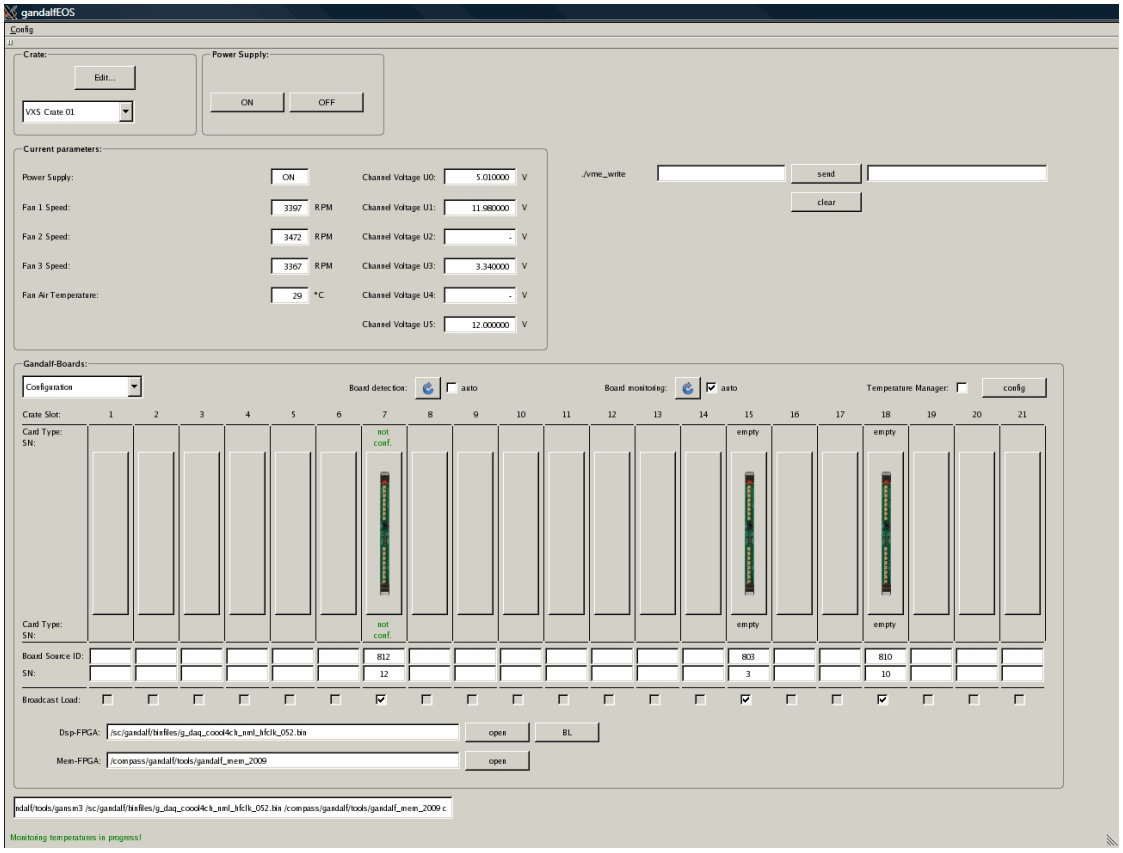


Figure 4.29: Screen-shot from the Eye of Sauron monitoring software [91]. The software configures the GANDALF modules installed to a VME crate via the VME bus. Temperature and voltage monitoring for the GANDALF modules is possible. The monitoring data is saved in a MySQL database.

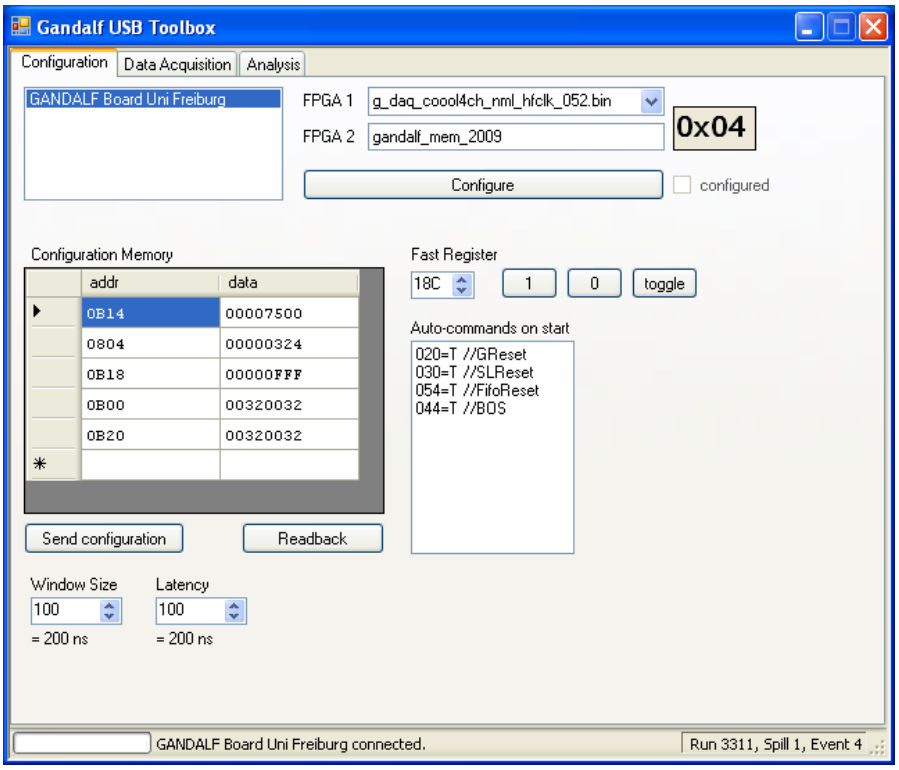


Figure 4.30: Screen-shot from the USB Toolbox configuration and analysis software [60]. This software tool configures the GANDALF module via the USB interface. Data readout and online data analysis and statistics are also possible. The generated raw data is stored in the COMPASS online data format [73].

5. Pulse Shape Analysis

In comparison to the functionality of a *transient recorder* - an electronic readout module, which is capable to digitize pulse shapes and record this data - the GANDALF module used with AMCs extends this functionality by owning the ability to analyze this data online. The digitization process is followed by an analyzing process which is realized in the huge logic capability inside the on board FPGA. Performing the electronic readout with online processing the GANDALF module is called in this functionality a *transient analyzer*.

As a preparation prior to the development stage of the GANDALF module and its mezzanine cards, the design constraints for the upcoming electronic readout challenges had to be defined. In the case of the use of the GANDALF module as a transient analyzer, it has to be clarified which quantization resolutions in time and amplitude for the digitizing process have to be chosen. Related to this, simulations have to be performed on algorithms to study the effect on the time resolution which could be achieved. The answers to these questions have to meet the technical feasibility of such algorithms inside FPGA logic.

Constraints for the development of the GANDALF module are defined by the CAMERA detector: The measured electronic pulse shape is expected to range from 0.0 V to -4.0 V and the rise time of the pulse is in the order of 3.0 ns depending on the energy deposit in the scintillator. The mathematical concept for the pulse shape analysis and different algorithms are described in the following. In the section *Verification* (5.2) an overview of different test measurement setups and the obtained results will be given. A first operation of the GANDALF module, analyzing real pulses from prototype scintillator slats of the CAMERA detector is described in the last section of this chapter.

5.1 Theory and Simulation

5.1.1 Mathematical description of the pulse shapes

For the simulation of the detector response a function has to be assumed which allows to compare the different scenarios simulated. This function has to describe the important characteristics of the pulse shape like amplitude, rise time and width. The mathematical description also has to be self-similar to the pulse shapes of real data. In all following simulations the Moyal distribution function is used [93]:

$$f(t) = c + A \cdot exp\left(-\frac{1}{2}\left(\frac{((t+t_s)-t_0}{\omega}\right) + exp\left(-\frac{(t+t_s)-t_0}{\omega} - 1\right)\right) + \epsilon_{noise}, \quad (5.1)$$

where A is the amplitude, c the baseline and t_0 is the time offset of the center of the signal. The value t_s is the sweep parameter. It is any random real number $t_s \in (-\tau/2, \tau/2]$ where $\tau = 1/f_s$ and f_s is the sampling frequency. This sweep parameter guarantees that any possible sampling configuration of the pulse shape occurs. The value ω defines the width of the signal shape and is connected to the rise time $t_{rise} = \omega/k$. For Moyal distributions the factor $k = 0.691$ [94]. The parameter ϵ_{noise} defines a contribution of Gaussian distributed thermal noise. In Fig. 5.1 four example pulses with different rise times and constant amplitudes are shown, digitized with a sampling frequency of $f_s = 1\,\mathrm{GHz}$. The amplitudes of the pulses are given in units of the relative dynamic range (rdr). This is the maximum digitization range of the analog input.

In a first assumption the sampling rate of the digitizing process has to be in an order of magnitude that the rising slope of the pulse shape is sampled with three or more samples. The four example pulses in Fig. 5.1 have rise times of $t_{rise} = \{2\,\mathrm{ns}, 4\,\mathrm{ns}, 6\,\mathrm{ns}, 8\,\mathrm{ns}\}$, an ϵ_{noise} of 0.25‰ß,rdr and are sampled with 1 GS/s.

To define an additional constraint for the analog circuit of the AMCs - the input bandwidth - the Fourier transform of the pulse shapes have to be studied. Therefore, a discrete Fourier transform over the simulated pulse data $S = \{s_0, \ldots, s_{n-1}\}$ was performed, following

$$f_k = \sum_{j=0}^{n-1} s_j e^{-\frac{2\pi i}{n} kj} \quad k = 0, \ldots, n-1. \tag{5.2}$$

The discrete Fourier transformations $F = \{f_0, \ldots, f_{n-1}\}$ for the four example pulses are given in Fig. 5.2. In the frequency domain the pulse shape has its main contribution ($> -40\,\mathrm{dB}$) in the frequency range of up to $f_{BW} = 100\,\mathrm{MHz}$. The significant part of the pulse shape reaches the noise level of $-62\,\mathrm{dB}$ (0.25‰ rdr)[1] at $f_{BW} = 150\,\mathrm{MHz}$ for the fast pulses of 2 ns rise time and $f_{BW} = 300\,\mathrm{MHz}$ for the pulses with 8 ns rise time. Following the sampling theorem the spectra in Fig. 5.2 are symmetrically distributed at $f_{BW} = 500\,\mathrm{MHz}$ for a sampling frequency of $f_s = 1\,\mathrm{GHz}$.
For a comparison of the mathematical description used for the simulations with real data, a pulse shape recorded with 1 GS/s sampling rate is given in Fig. 5.3. The corresponding discrete Fourier transform of this pulse data is given in Fig. 5.4.

More studies comparing the mathematical description of pulse shapes using the Moyal distribution with real data from a CAMERA detector prototype can be found in [94]. A detailed discussion about the time extraction methods from simulated pulses in comparison with real data can be found in the following sections.

5.1.2 The CFT algorithm

To associate a time stamp to a sampled pulse shape, different methods can be applied. They have to be selected from different criteria like the characteristics of the pulse shape (rise-time, dynamic range), the characteristics of the recording process (analog or digital, sampling rate, noise), and also the definition of the interesting time is important.

[1] relative dynamic range

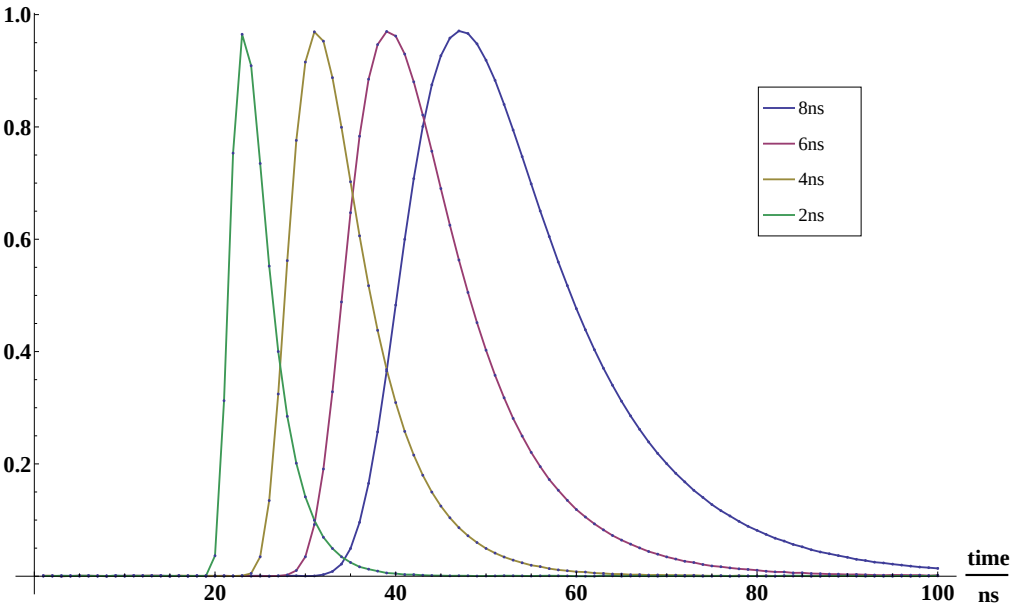


Figure 5.1: Four example Moyal distribution pulses with different rise times of $t_{rise} = 2\,\text{ns}, 4\,\text{ns}, 6\,\text{ns}, 8\,\text{ns}$ and a sampling frequency of 1 GHz (5.1). A noise level of $V_{noise} = 1\,\text{mV}$ is assumed here.

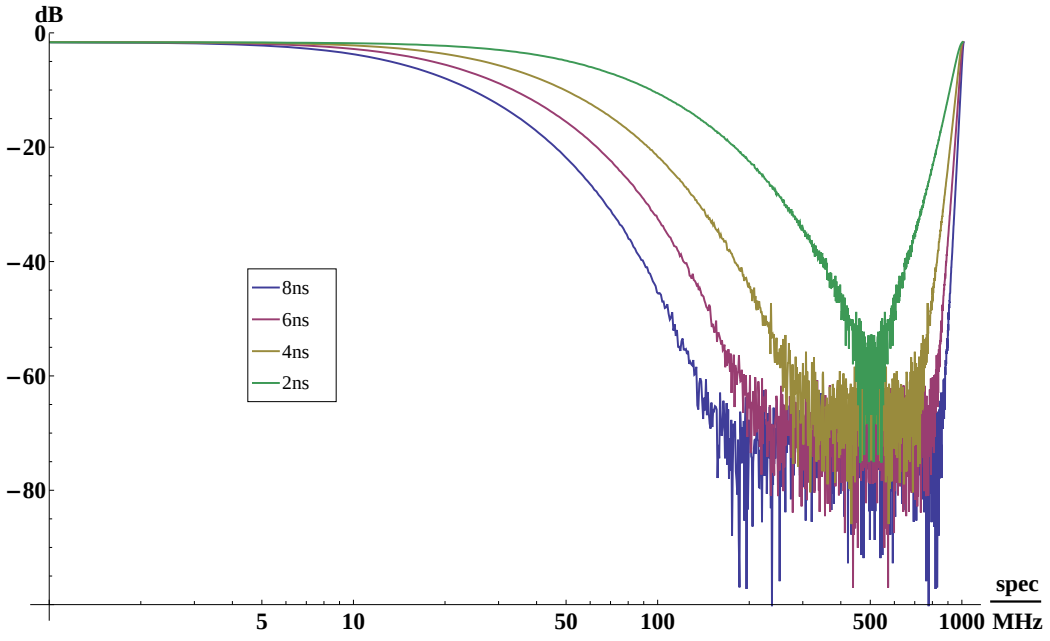


Figure 5.2: Four discrete Fourier transformations of the example Moyal distribution pulses plotted in Fig. 5.1. The noise level of $V_{noise} = 1\,\text{mV}$ produces the base level at $-62\,\text{dB}$.

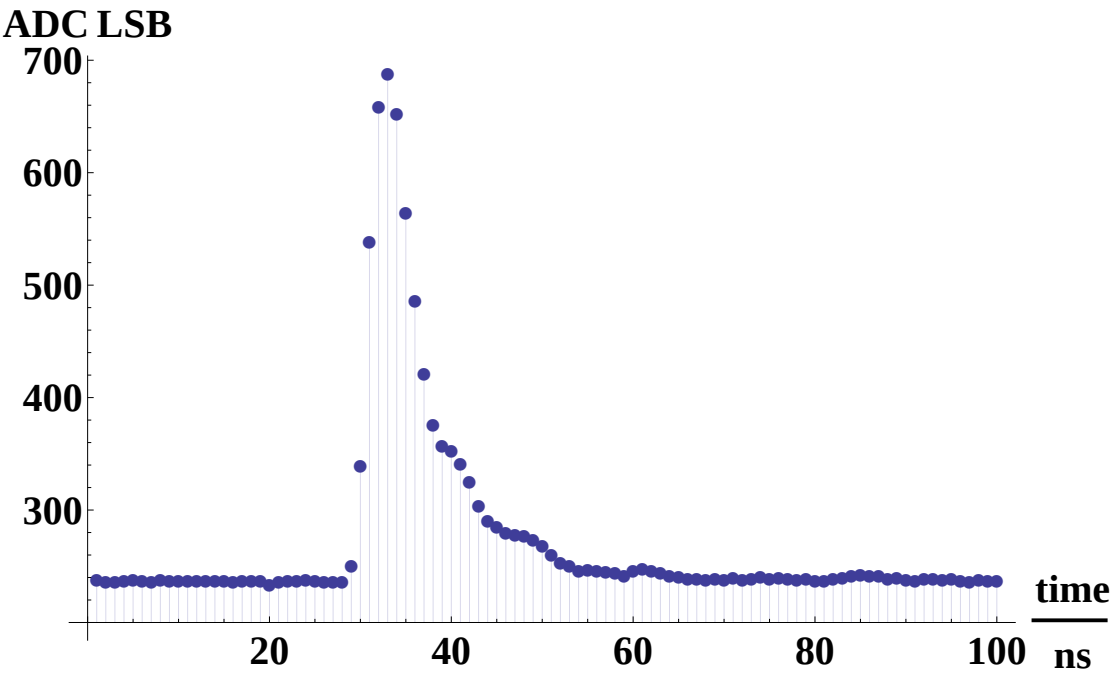


Figure 5.3: Plot of a sample pulse from real data sampled with 1 GS/s.

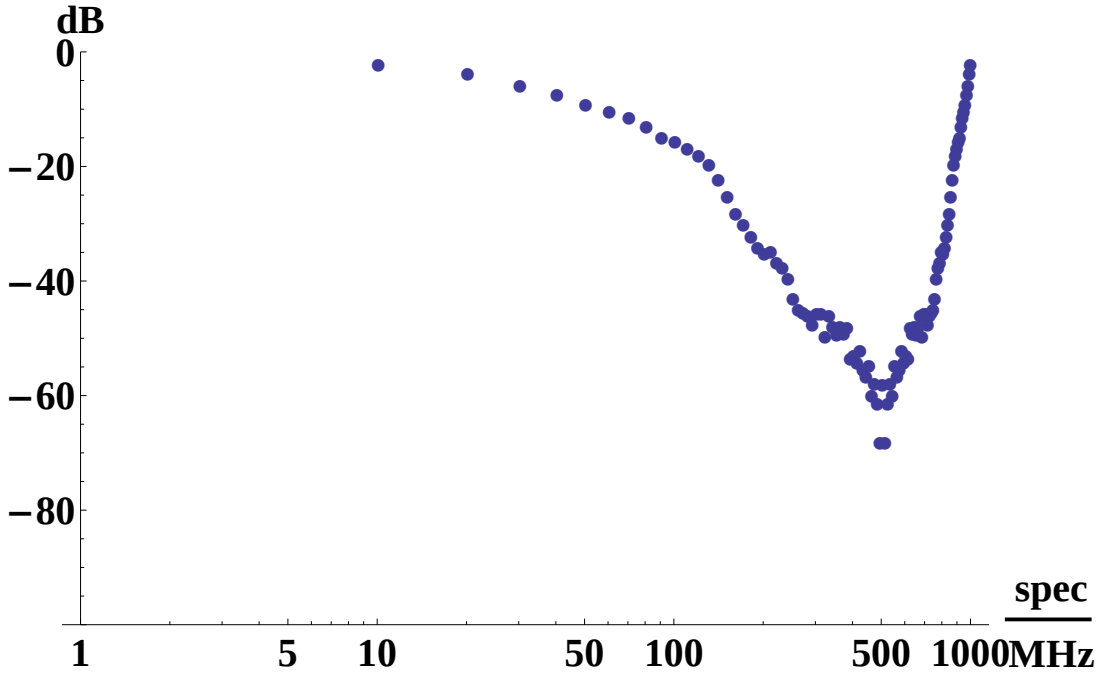


Figure 5.4: Discrete Fourier transform of sample pulse data.

Does the method have to determine the time of the maximum amplitude or the initial beginning of the pulse shape? In general these methods have to prevent effects which increase the resolution of the time measurement - they should be independent from parameters like amplitude or rise time.

In general a major source of uncertainty in a discriminator based time measurement is the "time walk". Different times t_1 and t_2 will be measured for pulses of different amplitudes, if a constant amplitude threshold is applied (see Fig. 5.5). This effect can be prevented by using a constant fraction threshold (CFT) algorithm. Here the threshold defining the time information t_{meas} is variable and is correlated with the maximum amplitude of the pulse shape. This avoids time walk effects, if the time information is given while the pulse crosses a constant fraction k_{thresh} of its maximum amplitude.

Due to the selectable fraction value k_{thresh}, this method brings another advantage with it: It is possible to select in which part of the rising edge the time of the pulse is measured. This can be an important possibility when looking beneath the mathematical description of the pulse to the physical origination. Due to reflections in the scintillating material the best timing can be reached at different regions of the rising edge. And secondly, this method is sensitive to the rising edge of the pulse only. The falling edge of the pulse can include parts from reflections inside the detector structure. This can be used for characterizing the initial particle of this pulse but has less time resolution than the rising part.

Using the constant fraction threshold algorithm with digitized data, one important effect concerning the maximum amplitude has to be taken into account. As the digitization process will generate data sampled in equidistant times and the pulse shape can occur in any correlation to these sampled times, the largest maximal sample value is unlikely the maximal value of the real pulse. This uncertainty depends on the width of the pulse and its sampling rate. A visualization of this problem is given in Fig. 5.6.

Looking on the implementation of this method in a FPGA the CFT algorithm brings slight disadvantages with it, because a data processing in a pipelined mode is preferred. This means in an ideal case that data can be loaded into the algorithm sample by sample and the process can progress the calculations without reprocessing the sampled data. The CFT method first has to check the data for maximum values then calculate the fraction threshold and afterwards continue to detect the time t_{meas}. If pile up pulses occurred in this process, it is impossible to gain the correct thresholds for these pulses.

5.1.3 The dCF algorithm

Another algorithm to determine the time information t_{meas} from a pulse shape preventing the "time walk" effect is the digital constant fraction (dCF) algorithm. Let us assume a pulse shape which is sampled at equidistant times $t_0, \ldots, t_{n-1}$ generating $n \in \mathbb{N}$ recorded data samples $S = \{s_0, \ldots, s_{n-1}\}, s_j \in [0, N], j \in \mathbb{N}$ where N is the maximum ADC code. A copy of the sampled data set S is produced and the values of this data set are inverted and divided by the fraction factor $k_{frac} \in \mathbb{R}^+$ to receive the inverted data sample set $I = \{i_0, \ldots, i_{n-1}\}, i_j \in [-M, 0], i_j \in \mathbb{R}$ where

$$i_j = -\frac{1}{k_{frac}} \times s_j, \quad \forall j = 0, 1, 2, \ldots, n-1. \tag{5.3}$$

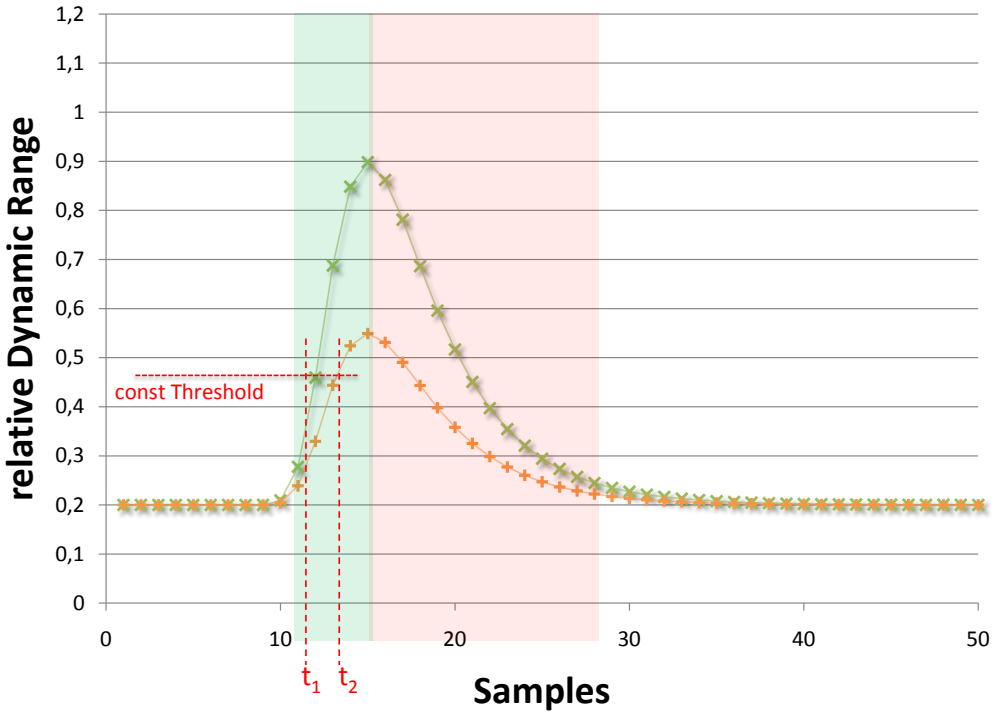


Figure 5.5: Time walk example for the constant threshold method. The red horizontal line gives the constant threshold value. The times t_1 and t_2 will be measured for pulses with different amplitude using this method, generating a time walk $t_w = t_2 - t_1$. Here and in the following plots, the time distance between the samples plotted on the x axis depends on the sampling frequency.

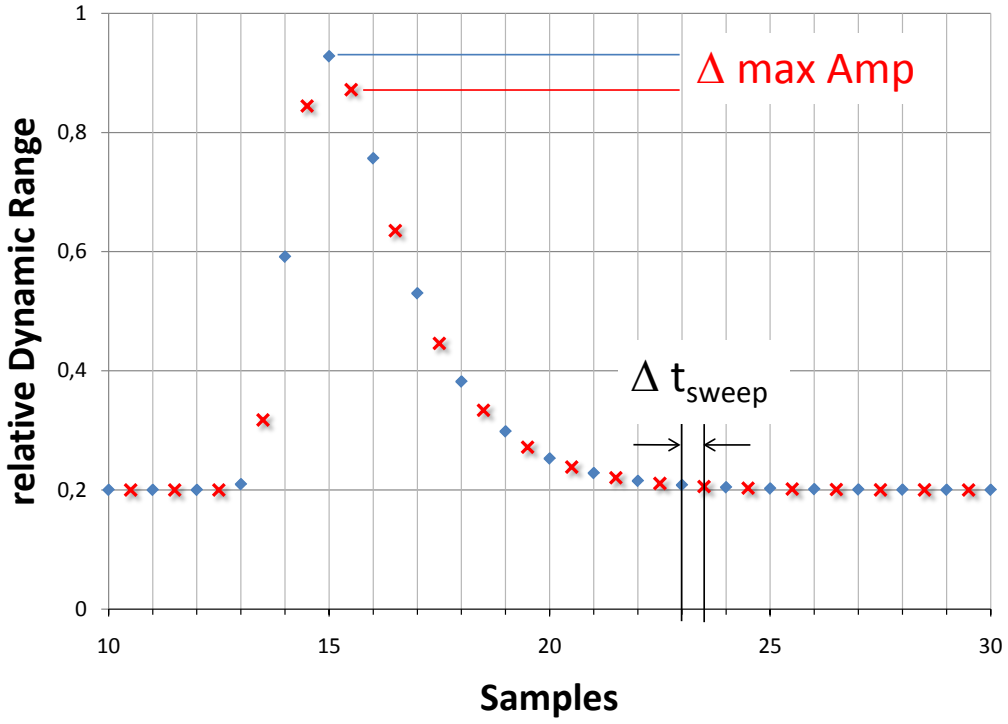


Figure 5.6: Determination of the maximum Amplitude for a sampled pulse. The maximum can either be defined by a Gaussian fit or by selecting the maximum data sample. In the second case the width of the pulse compared to the time between two equidistant samples has to be taken into account.

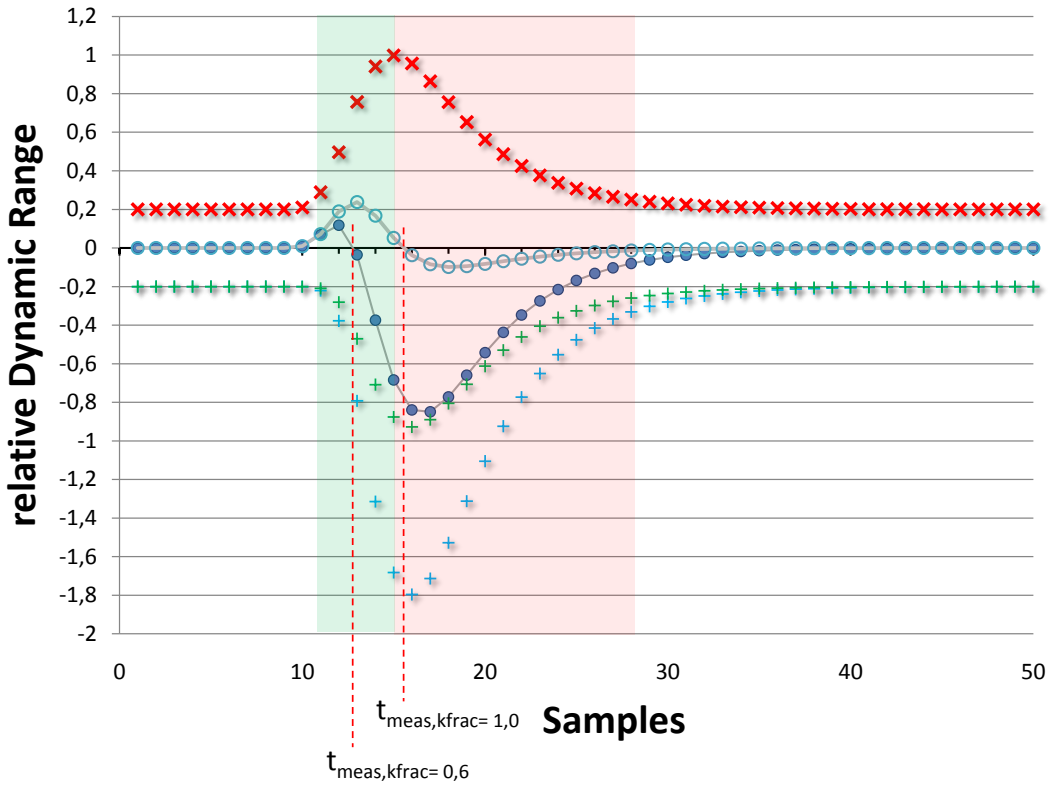


Figure 5.7: Example for time measurements in leading and trailing edge. For fraction factor $k_{frac} = 1$ and delay $m = 1$, the measurement of the time t_{meas} takes place in the trailing edge of the pulse which leads to worse time resolutions for real physical pulses (red region). Instead, for a fraction factor $k_{frac} = 0.5$, the time resolution can be optimized (green region).

This data set is delayed by an integer amount $m < n$ of time distances $t_{sampl} = t_j - t_{j-1}$ defined by the sampling frequency to generate the set of delayed data samples $D = \{d_0, \ldots, d_{n-m-1}\}$:

$$d_j = i_{j+m}, \quad \forall j = 0, 1, 2, \ldots, n - m - 1. \tag{5.4}$$

The sum of the values from the data set S and D then gives the set of data $C = \{c_0, \ldots, c_{n-m-1}\}, c_j \in [-M, N], c_j \in \mathbb{R}$ which is used to calculate a "time walk" free time information of the pulse expressed by S:

$$c_j = s_j + d_j, \quad \forall j = 0, 1, 2, \ldots, n - m - 1. \tag{5.5}$$

It is important to mention that the number of samples in the data set C is reduced depending on the delay value m. For a fraction value of $k_{frac} = 1$ and a delay value of $m = 1$, the data sample set C expresses a discrete derivative of the pulse shape given in S.
To determine a good time stamp of the occurring pulse the algorithm can check for the zero crossing between two data points c_l and c_{l+1} in the data sample set C. To receive the time information, a linear interpolation is performed between the smallest positive sample $c_l \in (0, N]$ and the consecutive negative sample $c_{l+1} \in [-M, 0]$. The zero crossing of the interpolation gives the time between the two consecutive sample times and is the extracted time t_{meas} from the pulse shape. In the special case $c_l = 0$, the time $t_{meas} = t_l$ is given by the algorithm as extracted time from the pulse shape. In Fig. 5.8 an example pulse and its digital constant fraction data is shown. The data set S is given in red crosses ($\times$). The delayed data set D is shown in blue crosses ($+$). The dark blue unfilled squares give the data set C where the time t_{meas} can be determined.

To be able to set constraints for the digitizing process, simulations were performed by changing the sampling rate and the amplitude resolution. Values used for these simulations were chosen in dependence on available market solutions. The analog to digital conversion chips from Texas Instruments $ADS5463$ and $ADS5474$ were focused after a preselection concerning the maximum sampling frequency and the signal-to-noise ratio [64, 65]. In Fig. 5.9 results of the simulations for different sampling parameters and modes are given. The x axis gives the amplitude of the digitized pulse in units of the relative dynamic range of the digitization process, the y axis the time resolution of the time measurement process. The dependence of the time resolution on the amplitude and, therefore, on the slope of the pulse can clearly be seen in this figure. As our design constraints demand for a time resolution below the time-of-flight measurement resolution of $\sigma_{t,det} \approx 200\,\text{ps}$, the time extraction algorithm should be able to reach resolution below $\sigma < 50\,\text{ps}$.
All results given in Fig. 5.9 of the simulated configurations show this expected resolution. To stay flexible all four simulated configurations can be performed with the designed GANDALF module hardware using either the $ADS5463$ or $ADS5474$ chips in normal or time interleaved mode (see section 4.1.3).

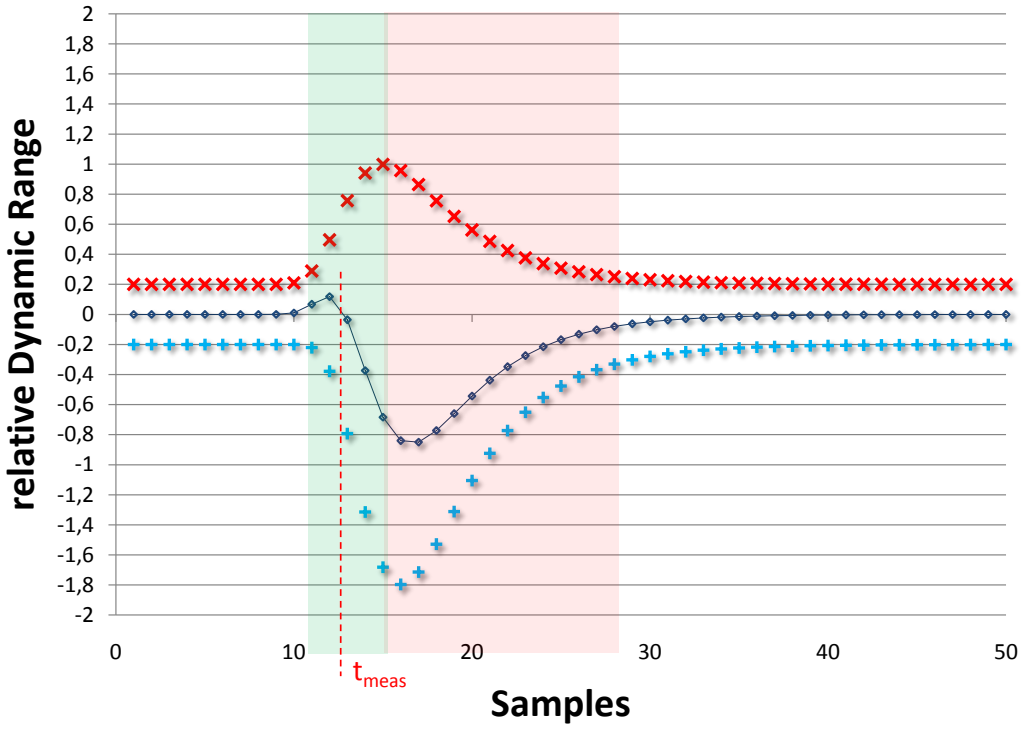


Figure 5.8: Implementation of the digital Constant Fraction algorithm performed on an example pulse. The red crosses (×) show the samples from the digitization of the example pulse S, the blue crosses (+) the delayed data set D. The dark blue unfilled squares give the data set C where the time t_{meas} can be calculated from by determining the zero crossing of the blue interpolation line.

Due to thermal and quantization, noise on the input of the real pulse shape is not adequate for the algorithm to check for zero crossings of consecutive data samples, because noise will produce such situations without any occurring pulse. Therefore, another constraint is obliged to the algorithm to select pulses above the noise level properly. The zero crossing will only be calculated if two consecutive data samples $c_i \in C$ are beyond a fixed threshold c_{tresh}.
To simulate how the time resolution changes by applying different levels of thermal noise, the dCF algorithm was performed on a set of 10^5 artificially generated pulses. The function describing this pulse shape is given in equation (5.1). The results of these simulations are plotted in Fig. 5.10 for different contributions of $\epsilon_{noise} = \{0.125, 0.25, 0.5, 0.75, 1.0\}$ ‰ rdr. These values correspond to a noise sigma of $\epsilon_{noise} = \{0.5, 1.0, 2.0, 3.0, 4.0\}$ mV for a dynamic input range of 4.0 V_{PP}. For the planned setup with the CAMERA detector, a noise level of $\epsilon_{noise} = 0.98$ mV is measured. The contribution to time resolution performance due to this distortion has to be mentioned. Other distortion factors like jitter and phase error on the sampling clock ($t_{jitt} < 1$ ps, $t_{phase} < 5$ ps) were also

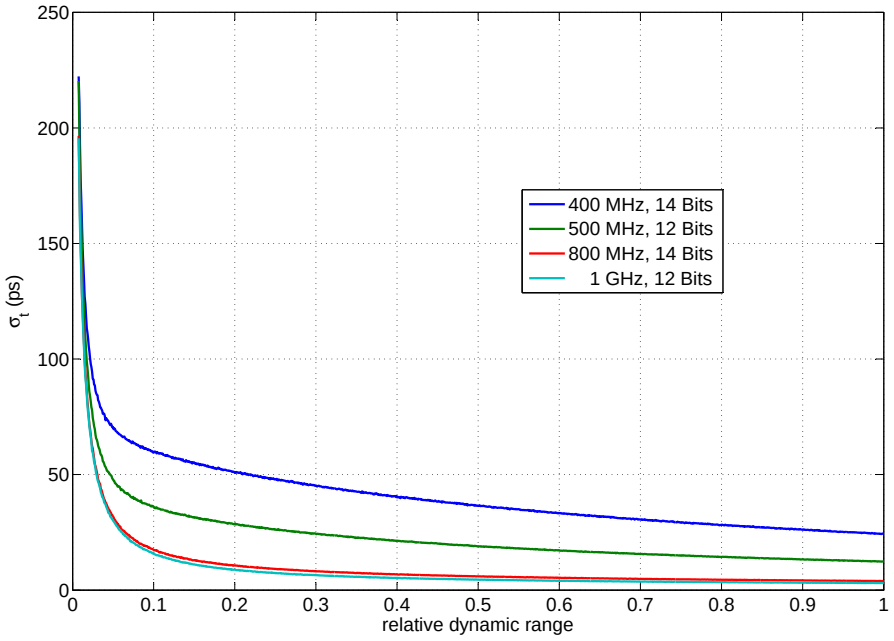


Figure 5.9: Time resolution compared to the amplitude of the pulse using the dCF algorithm. The x axis gives the amplitude of the digitized pulse in relative dynamic range of the digitization process, the y axis the time resolution of the time measurement process. The simulations were performed by using sampling parameters of the $ADS5463$ and $ADS5474$ analog to digital conversion chips in normal and time interleaved mode [68].

taken into account on additional simulations. The results have shown that no visible effects due to those distortions could be recognized [68].

In Fig. 5.11 simulation results for time resolutions for pulses with a rise time of 3 ns and a sampling rate of $f_s = 1\,\mathrm{GS/s}$ are given. The x axis gives the amplitude of the pulse in relative dynamic range, the y axis the fraction factor k_{frac} and the z axis gives the corresponding time resolution in ps. For the mathematical description of the pulses, an optimum fraction factor of $k_{frac} = 0.6$ can be identified using the optimum delay value of $m = 1$.

From the physical point of view, the time information given by the pulse response of a PMT has its best resolution in the leading edge of the pulse. The trailing edge can be distorted by e.g. reflections or secondary interactions inside the detector. Therefore, the time extraction algorithm may not be sensitive in the time range of the trailing edge of the pulse. In Fig. 5.7 two examples are given for the fraction values $k_{frac} = 1.0$ and $k_{frac} = 0.5$ and a delay value of $m = 1$. For the fraction value $k_{frac} = 1.0$, the zero crossing can be found in the time range of the trailing edge (red region in Fig. 5.7). The time measurements will show worse resolutions for the reasons mentioned above. To move the zero crossing point into the region of the trailing edge (green region in Fig.

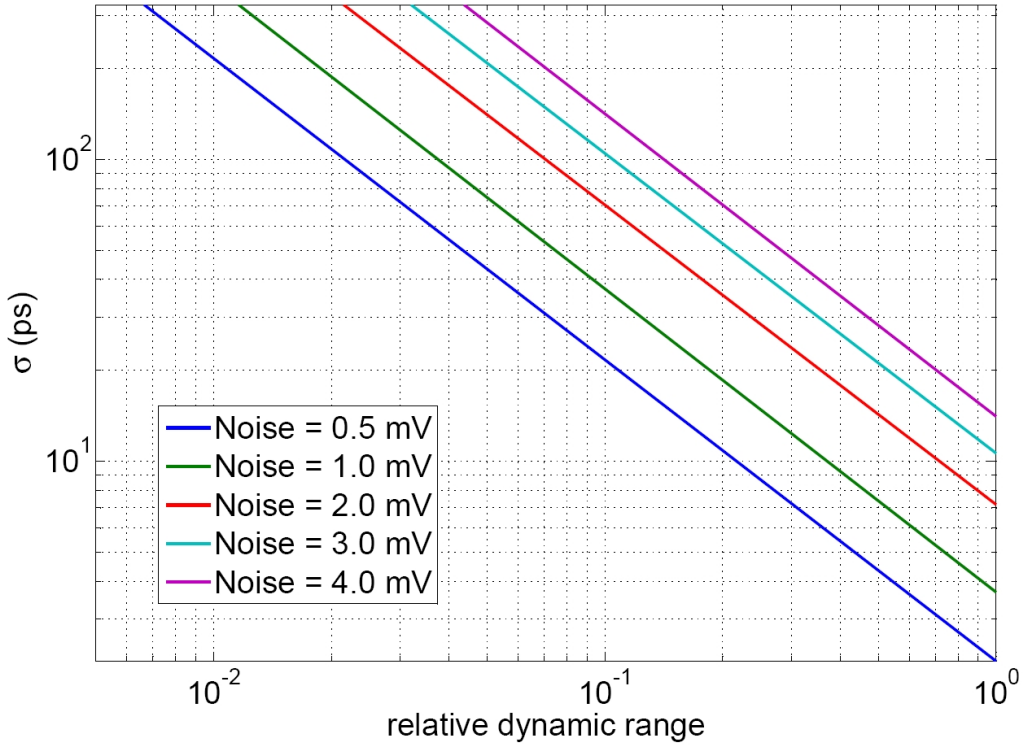


Figure 5.10: The time resolution of the dCF algorithm compared to thermal noise on the input signal. The results of simulations with 10^5 randomly generated pulse shapes sampled with 1 GS/s is plotted for different contributions of $\epsilon_{noise} = \{0.125, 0.25, 0.5, 0.75, 1.0\}$‰ rdr. These values correspond to a noise sigma of $\epsilon_{noise} = \{0.5, 1.0, 2.0, 3.0, 4.0\}$ mV for a dynamic range of 4.0 V [68].

5.7), the fraction factor has to be changed to $k_{frac} = 0.5$.

Concluding the simulation results for the time resolution of the dCF algorithm, following parameters for the digitization unit of the GANDALF module can be summarized: The time resolution of the readout electronics has to be better than the resolution of the CAMERA detector (≈ 200 ps) for a large region of the relative dynamic range. Therefore, the dCF algorithm must reach better time resolutions for pulses with rise times of 3 ns, a bandwidth of $f_{BW} < 200$ MHz and a signal noise level of $\epsilon_{noise} = 0.25$ ‰ rdr, which are the characteristics of the pulses expected from the CAMERA detector. The simulations have shown (see Figs. 5.9, 5.10, 5.11), that these resolutions can be reached with the digitization units selected for the design of the GANDALF *transient analyzer*.

5.1.4 Pile-up pulse processing

Full scale GEANT 3 Monte Carlo simulation of the planned CAMERA recoil proton detector and the M2 muon beam predicts a hit rate in the range of up to 5 MHz. De-

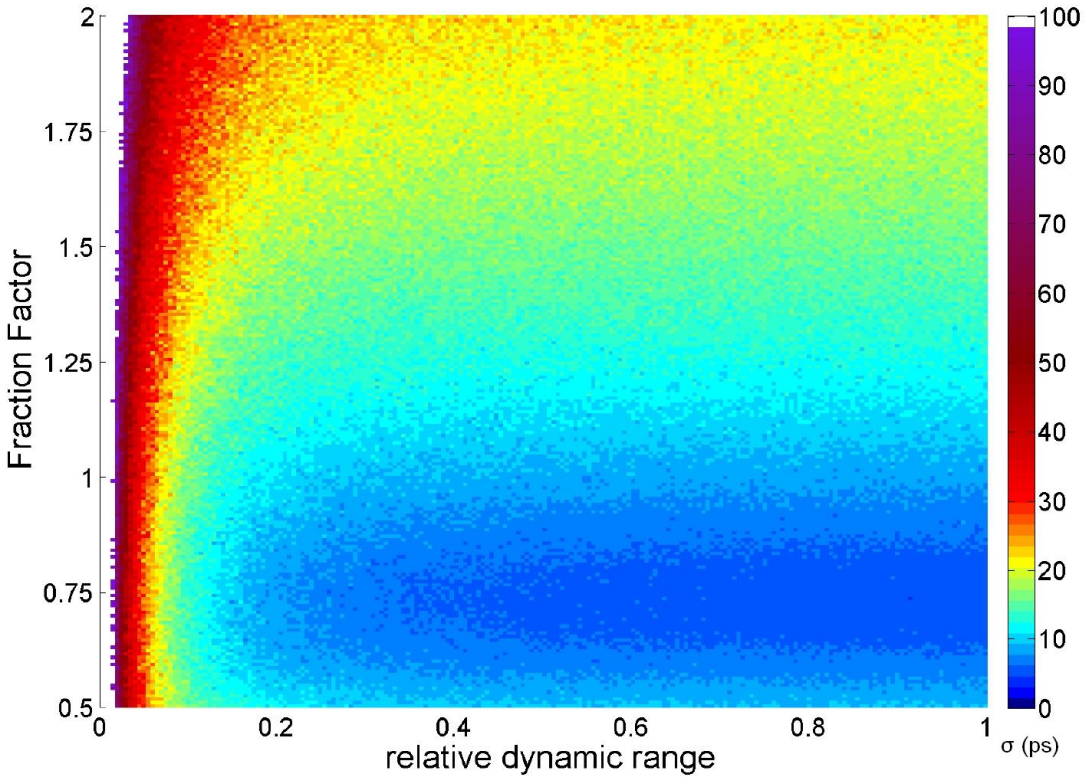


Figure 5.11: Time resolution of the dCF compared to different fraction factors. The x axis gives the amplitude of the pulse in relative dynamic range, the y axis the fraction factor k_{frac} and the z axis gives the corresponding time resolution in ps. The simulations were performed for pulses with a rise time of 3 ns, a noise level of 0.25 ‰ rdr and using the dCF with a delay value of $m = 1$. [68].

pending on the beam intensity pile-up due to δ-electrons and beam halo particles may occur. This pile-up is the most important reason for the design of the GANDALF transient analyzer to perform direct digitizing units without using any shaping or integrating components to reduce the sampling frequency and, therefore, the data amount to process. With any shaping procedure, time information of possible piled-up pulses would be lost. Only sampling the fast pulses with $t_{rise} \approx 3\,\text{ns}$ combined with a dedicated time extraction algorithm, the time information of the piled-up pulses can be obtained.

The digital Constant Fraction algorithm provides capabilities to separate closely timed pulses when using the discrete derivative $C = \{c_0, \ldots, c_{n-m-1}\}$ (see section 5.1.3). An example for two piled-up pulses is given in Fig. 5.12. On the trailing edge of the first pulse (starting at sample s_{10}), a second pulse is piled-up (starting at sample s_{27}). The open squares in dark blue represent the data samples $C = \{c_0, \ldots, c_{n-m-1}\}$ calculated as mentioned in the previous section. The open circles in green show the discrete derivative $C' = \{c'_0, \ldots, c'_{n-m-1}\}$ of the data samples C. Calculated by:

$$c'_j = c_{j+1} - c_j, \quad \forall j = 0, 1, 2, \ldots, n - m - 2. \tag{5.6}$$

The zero crossings with a positive slope of the linear interpolation of the data samples in C' can be used to determine the times for any consecutive pulses $t_{meas,1}$ and $t_{meas,2}$ (see Fig. 5.12).

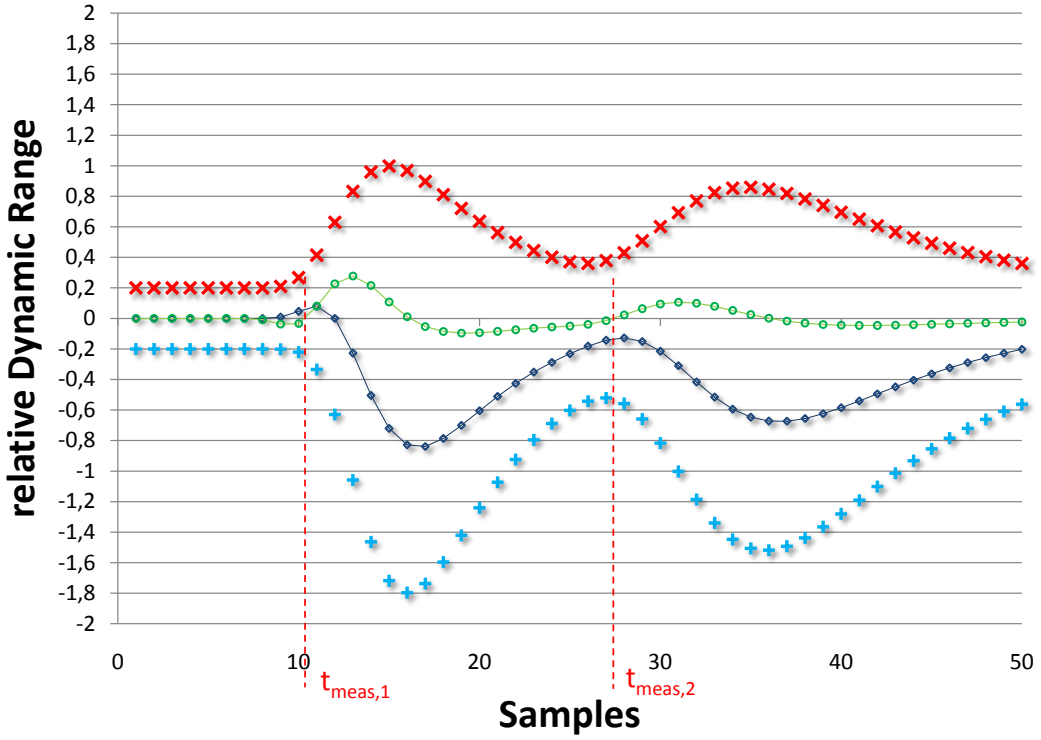


Figure 5.12: Implementation of the digital Constant Fraction algorithm performed on an example of two piled-up pulses. The red crosses (×) show the samples from the digitization of the example pulses S, the blue crosses (+) the delayed data set D. The dark blue unfilled squares give the data set C and the green open circles the data set C' where the times $t_{meas,1}$ and $t_{meas,2}$ can be determined.

Simulations with two near following pulses were performed to characterize the capability of the digital constant fraction algorithm on pile-up pulses. The separation power depends on the distance in time t_{dist} between consecutive pulses and on the amplitudes of the two pulses $A_{max,1}$ and $A_{max,2}$. A pulse with a small amplitude e.g. $A_{max,2} = 1\%\,\mathrm{rdr}$ will be hard to detect on the trailing edge of a pulse with $A_{max,1} = 90\%\,\mathrm{rdr}$. Simulations were performed generating consecutive pulses with different amplitudes. The distance in time t_{dist} between the pulses was first kept to a minimum so that the two pulses are recognized as one single pulse by the algorithm. Then the time distance is increased until the algorithm starts to detect two separated pulses. This value for t_{dist} is stored for each amplitude relation $A_{rel} = A_{max,1}/A_{max,2}$. The pulse generation process for the simulation uses the same simulation pulse shape parameters

$t_{rise} = 3.0ns, t_{jitt} < 1ps,\ t_{phase} < 5ps,\ \epsilon_{noise} = 0.25‰$ rdr as mentioned in section 5.1.3. The results for these simulations are given in Fig. 5.13. In this plot x axis shows the amplitude of the first pulse, the y axis the amplitude of the second pulse (both in relative dynamic range) and the z axis gives the distance in time from which the algorithm starts to separate the two pulses. Due to the asymmetric shape of the Moyal distribution (5.1), the separation is easier if the amplitude relation is $A_{rel} < 1.6$, which means a configuration where the first pulse has a small amplitude and the following pulse has a large amplitude, can be better separated than in the other case ($A_{rel} > 1.6$). If the amplitude relation is $A_{rel} \approx 1.6$ and if the time distance is $t_{dist} \geq 2 \times t_{rise}$, a separation is possible.

To complete the simulation results, the Figs. 5.14 and 5.15 give the time resolution for the detected pulses given in Fig. 5.13. For each time resolution value shown in these plots the smallest possible time distance between two pulses. Whenever two pulses are detected at the minimum time distance t_{dist}, the time resolution for the first pulse is plotted in Fig. 5.14 and the time resolution for the second pulse in Fig. 5.15. The time for the first pulse can be calculated with a higher precision in the region $A_{rel} > 1.6$ and the same can be seen for the second pulses for $A_{rel} < 1.6$.

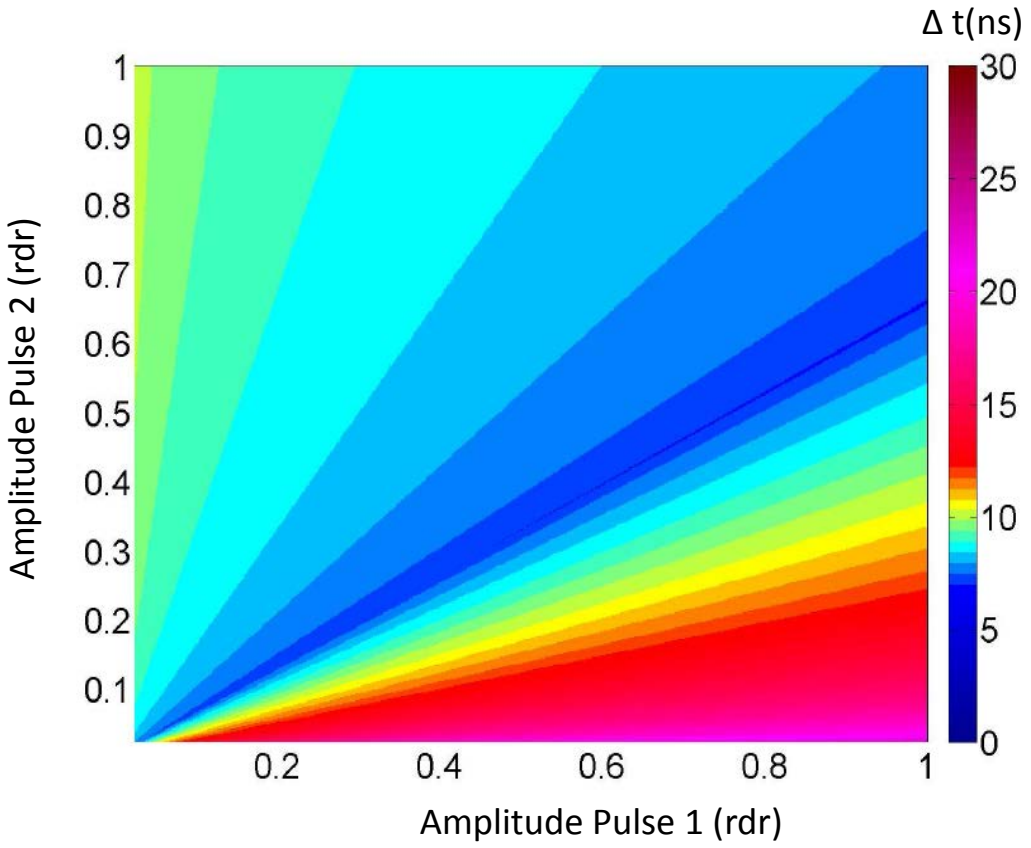


Figure 5.13: Simulation results for the resolution of two consecutive pulses. The x axis gives the amplitude of the first pulse, the y axis the amplitude of the second pulse. The risetime of the pulses is 3 ns at a sampling rate of 1 GS/s and a resolution of 12 bit. The values are given in relative dynamic range [68].

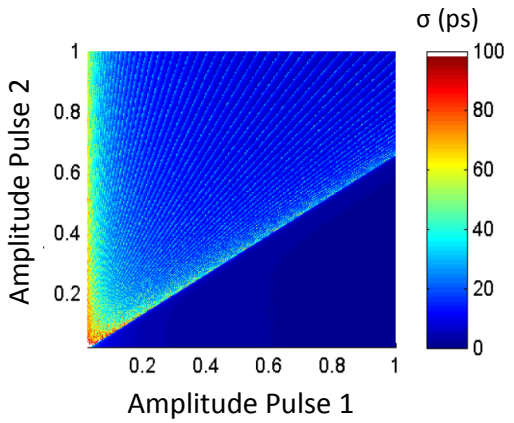


Figure 5.14: Simulation results for the time resolution for the first separated pulse. The x axis gives the amplitude of the first pulse, the y axis the amplitude of the second pulse. The values are given in relative dynamic range [68].

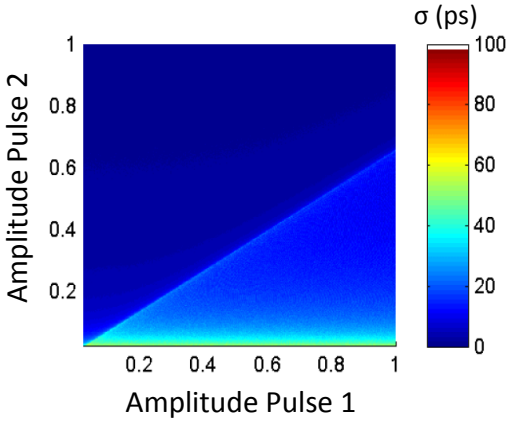


Figure 5.15: Simulation results for the time resolution for the second separated pulse. The x axis gives the amplitude of the first pulse, the y axis the amplitude of the second pulse. The values are given in relative dynamic range [68].

5.2 Verification

5.2.1 ENOB Measurements

The design constraints for the GANDALF module used as a transient analyzer to determine information like time, energy deposition and characteristics from the pulse shape, have to take into account the linearity and the noise on the recording process. The following measurement points on the verification of the reached bandwidth and noise characteristics for the analog inputs of the AMC used with the GANDALF module. In Fig. 5.16 an overview of the measurement setup is given. To determine the characteristics of the analog input circuit the signal-to-noise ratio at different bandwidths have to be analyzed. Therefore, the digitization of sine waves with frequencies in the interesting range is performed. The digitized data is then Fourier-transformed to extract the signal-to-noise ratio which is additively generated by the analog circuit and the digitization process. The measurement allows for classifying the design quality concerning noise increase due to jitter on the sampling clocks, power supply noise and crosstalk due to the high channel density on the AMC.

As a signal source for sine waves covering a frequency range of 21.4 MHz to 240 MHz, an *AFG3251* was used [95]. The signal-to-noise ratio for the signal output of this device is given to $< -90\,\mathrm{dB}$ [95]. To suppress harmonics of the sine wave which is provided to the analog input of the GANDALF module, high performance bandpass filters produced by *LORCH Inc.* and *Mini-Circuits* were used. The center frequency and bandpass width of the filters were chosen to the following values:

Table 5.1: Used bandpass filters for the measurements of the signal-to-noise ratio by screening the analog input bandwidth.

Filter Type	Center Frequency	3 dB Bandwidth	Manufacturer
SBP-21.4+	21.4 MHz	± 2.2 MHz	Mini-Circuits
SBP-70+	70.0 MHz	± 7.0 MHz	Mini-Circuits
4BC-150/5-S/SM	150.0 MHz	± 5.0 MHz	LORCH Inc.
5BC-200/5-S/SM	200.0 MHz	± 5.0 MHz	LORCH Inc.
5BC-240/5-S/SM	240.0 MHz	± 5.0 MHz	LORCH Inc.

In Fig. 5.17 results for the signal-to-noise measurements for the given frequencies defined by the filters center frequency, are given in SNR[2] and ENOB[3]. The measurement was performed in two sampling modes, with $f_s = 505.44\,\text{MHz}$ and $f_s = 1010.88\,\text{MHz}$. The record length was $t_{rec} = 128\,\mu\text{s}$ to be able to study the results for a phase range down to a few MHz.

In Fig. 5.17 filled green squares give the results for a sampling of the sine waves with $f_s = 505.44\,\text{MHz}$ which reach values above 10.0 LSB ENOB. The blue dashed line gives the same results for a measurement performed with $f_s = 1010.88\,\text{MHz}$. A decrease of the signal-to-noise ratio in this sampled data is caused by an error on the phase shift between the two clocks connected to the two ADCs for the time-interleaved sampling mode. As mentioned in section 4.1.3, a sampling rate in the GHz domain can be reached on the GANDALF module by using two adjacent ADCs on the AMC digitizing one common input signal. Therefore, the clocks for this ADCs have to be phase shifted by precisely $\phi = 180°$. However, unknown small delays between the two clock lanes, caused by chip or placement variations, can occur in a slight phase change $\phi + \xi$. A correction of the data can be done offline by using the following transformation of the sampled data $S = \{s_0, \ldots, s_{n-1}\}$ sampled at the times $T = \{t_0, \ldots, t_{n-1}\}$:

$$s_i = sin(\omega t_i) \rightarrow s_i' = sin(\omega t_i + \xi), \quad i = \{0, 2, 4, \ldots, n-2\}, \tag{5.7}$$

where $\omega = 2\pi f_{sin}$ and f_{sin} is the frequency of the sine signal. The number of samples n is per definition even in this sampling mode. For all measurements with different frequencies f_{sin} the same time offset $t_\xi = \frac{\xi}{2\pi f_{sin}}$ is expected. From the recorded data t_ξ was calculated offline and then used to correct the data (see blue data points in Fig. 5.17). The performance of the analog input circuit together with the digitization process shows conformance to the requirements given by the simulation constraints. The analog input circuit designed within the AMC used together with the GANDALF module has a resolution better than 10.0 LSB ENOB over the important analog bandwidth. Compared to the values given from the data sheet of the $ADS5463$ (red triangles in Fig. 5.17) the measurement shows a reduction of the resolution which is less than 0.3 LSB ENOB

[2]Signal-to-Noise Ratio

[3]Effective Number of Bits. $ENOB = \frac{SNR-1.76}{6.02}$ [96]

despite the high channel density and high power consumptive environment on the AMC mounted on a GANDALF module.

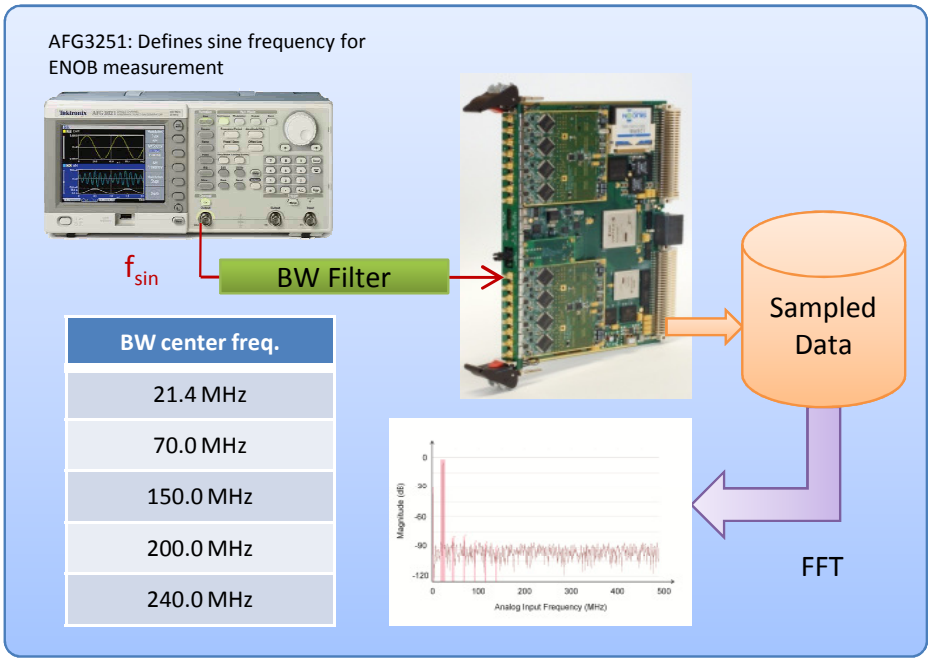


Figure 5.16: Schematic overview of the setup for the ENOB measurement. An AFG3251 function generator was used to generate sine functions with frequencies of $f_{sin} = \{21, 71, 150, 199, 240\}$ MHz. Different filters were used to guarantee optimal signal-to-noise ratios for the input signals (Tab. 5.1). The sampled waveform data is collected with a data acquisition system for offline fast Fourier transformation and phase corrections for the data recorded in time-interleaved mode.

These measurement results can also be used to testify about the jitter of the sampling clocks used for the digitization process. Jitter is the aberration in time for the digitization from an ideal time. This error in the sampling time results in an error for the measured voltage which depends on the slope of the signal. Using a sine wave as input signal for the digitization process the jitter on the sampling clock, the quantization error and thermal noise results in a signal-to-noise ratio [97]:

$$SNR = -20log\left((2\pi\ f_{sin}\ t_{jitter,rms})^2 + \left(\frac{1+\epsilon}{2^N}\right)^2 + (V_{noise,rms})^2\right), \qquad (5.8)$$

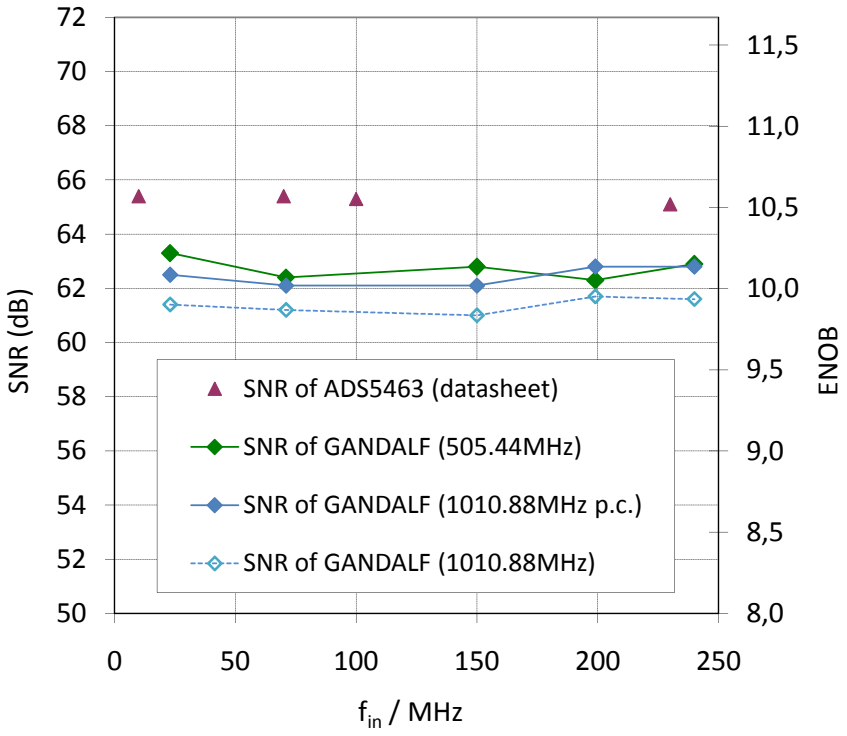


Figure 5.17: Measurement results for the signal-to-noise ratio of the analog input circuit. The green line is representing the SNR measured with the GANDALF module and a sampling frequency of $f_s = 505.44\,\text{MHz}$. The blue dashed line with a sampling frequency of $f_s = 1010.88\,\text{MHz}$. The blue line is describing the SNR after the correction of the data with the phase offset ξ (see (5.7)). The red triangles are representing the values given in the data sheet for the chip itself [95].

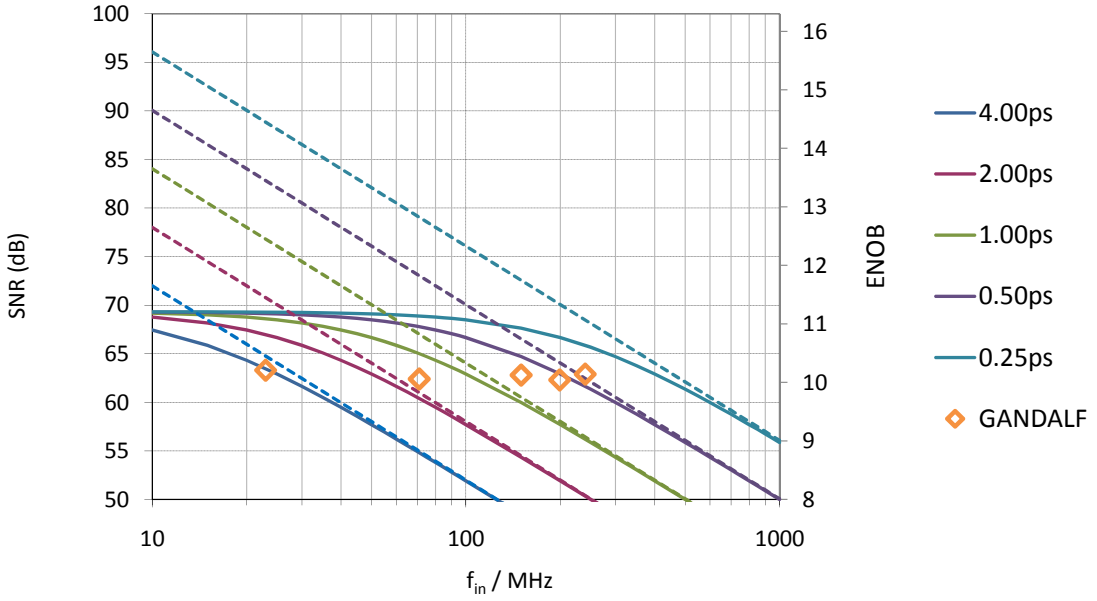


Figure 5.18: Simulation results to estimate the maximum jitter contribution of the sampling process. The different signal-to-noise relations for different jitter values from 0.25 ps to 4.00 ps are given. The dashed line does not consider the quantization error of the $N = 12$ bit ADC (5.8). For a comparison the orange squares represent the measurement results given in Fig. 5.17.

where f_{sin} is the sine frequency, $t_{jitter,rms}$ the rms value of the jitter of the sampling clock, $\epsilon = 0.25\,LSB$ the DNL of the ADC [64], $N = 12$ the number of bits and $V_{noise,rms} = 0.25‰$ which is the expected detector noise.

The signal-to-noise ratio is plotted in Fig. 5.18 for different jitter values $t_{jitter,rms} = \{0.25, 0.50, 1.00, 2.00, 4.00\}$ ps. The dashed lines show the behavior contribution to the noise by jitter only. The full lines represent the behavior including the quantization error. The contribution of $V_{noise,rms} = 0.25‰$ is small compared to the contributions from jitter and quantization error. To be able to compare this proposition with the measurement results obtained from the sine digitization with the GANDALF module the values are plotted in orange squares. Reaching a signal-to-noise ratio above 10.0 LSB ENOB at 240 MHz concludes in jitter performance of the sampling clock better than $t_{jitter,rms} = 500$ fs.

A phase noise measurement at the output of the $SI5326$ is given in Fig. 5.19 to determine the jitter of the sampling clock. The measurement was performed by using a 155.54 MHz input clock and generating a 622.08 MHz output clock [98]. The jitter contributing to the output clock depends on the observed frequency bandwidth in which digitization measurements take place. In Tab. 5.2 obtained jitter values for several frequency bands are listed [98]. This information on the jitter of the $SI5326$ can be compared with ENOB measurement results in Fig. 5.18. As the record length with the GANDALF module is $t_{rec} = 128\,\mu$s, this results in a digitizing bandwidth of $f_{min} =$

$\frac{1}{t_{rec}} = 7.81\,\text{MHz}$ to $f_{max} = f_s = 500\,\text{MHz}$. The jitter contribution $t_{jitter,rms}$ can be calculated from the phase noise with [99]:

$$t_{jitter,rms} = \frac{\sqrt{2 \cdot \int_{f_2}^{f_1} L(f)df}}{2 \cdot \pi}. \tag{5.9}$$

Where f_1 and f_2 are the frequencies defining the measurement bandwidth, and $L(f)$ the function resulting from the phase noise measurement ([99]). The values given in Tab. 5.2 for such ranges are in agreement with a jitter value of better than $t_{jitter,rms} = 500\,\text{fs}$ as derived from Fig. 5.18.

Table 5.2: Clock output jitter obtained by phase noise measurements, integrated over different jitter bands [98].

Jitter Band	Jitter, RMS
100 Hz to 100 MHz	1.279 ps
12 kHz to 20 MHz	315 fs
20 kHz to 80 MHz	335 fs
80 MHz to 500 MHz	240 fs
4 MHz to 80 MHz	194 fs

5.2.2 Deconvolution Method

To verify the time resolution of the GANDALF module used as a transient analyzer using the digital Constant Fraction algorithm as explained in section 5.1.3, a special measurement method was developed. The following section will give an overview of the *Deconvolution Method* to determine the time resolution of the transient analyzer. Fig. 5.20 gives an overview of the setup for this timing performance measurement.
The basic measurement consists of the calculation of the time difference of two digitized pulses given to two analog input channels. For the measurement of a single event two pulses $P1$ and $P2$ are generated with an *AFG3252*[4] function generator using the following expression defining the output function [100]:

$$f(t) = c + A \cdot exp\left(-\frac{1}{2}\left(\frac{t-t_0}{\omega}\right) + exp\left(-\frac{t-t_0}{\omega} - 1\right)\right), \tag{5.10}$$

where A is the amplitude, c the baseline and t_0 is the time offset and center of the generated signal. ω is the width of the signal shape. As described in 5.1, this Moyal distribution is used for any pulse generation, for simulations as well as for the generation of pulses with function generators.

In the next step, the artificial generated pulses were given to two analog inputs of the AMCs mounted to the GANDALF module. There, the pulses get digitized and afterwards transferred to the DSP-FPGA (*U9*). The FPGA accepts the data and processes

[4] Tektronix Inc.

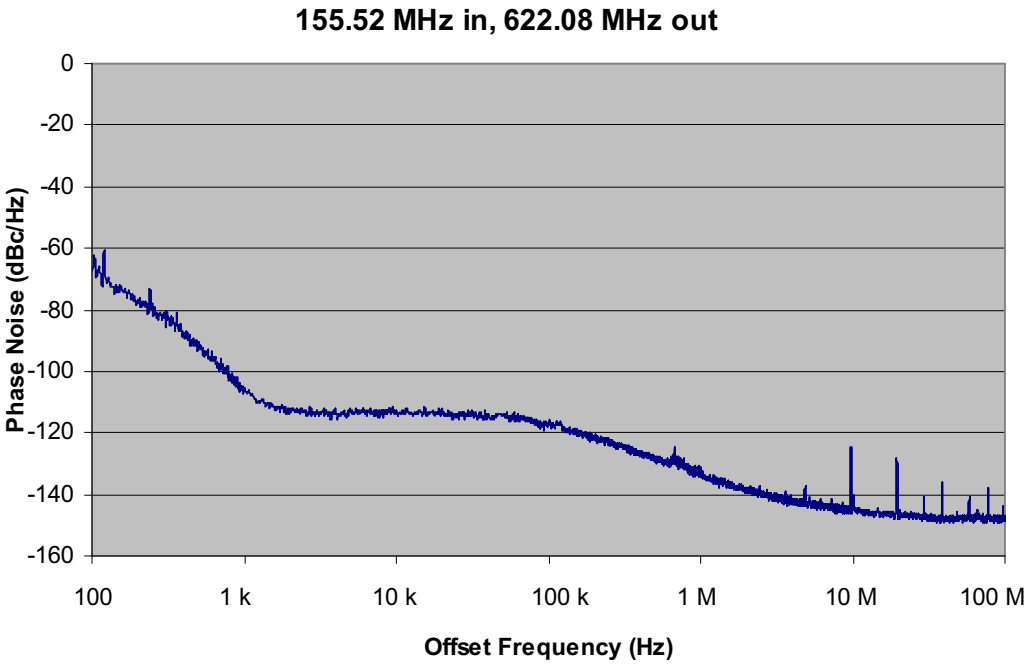


Figure 5.19: Phase noise plot to determine the jitter of the output clock of the *SI*5326 clock manager [98]. The measurement was performed with an input frequency of 155.54 MHz and an output frequency of 622.08 MHz [98].

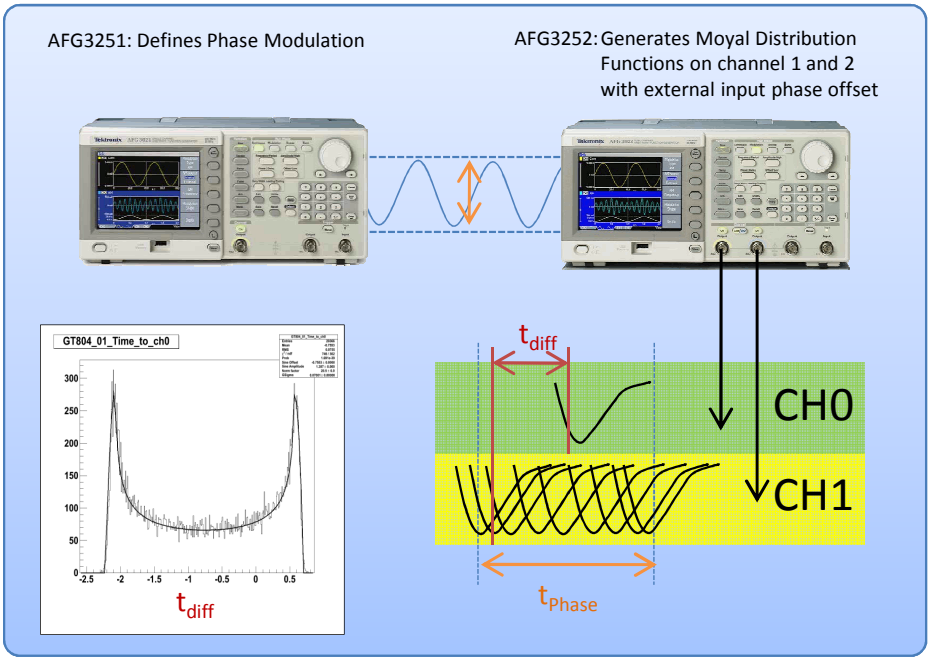


Figure 5.20: Schematic overview of the measurement setup for the convolution method.

it with the implemented digital Constant Fraction algorithm to detect the time information. The results are transferred to the data acquisition system and stored for the offline analysis of the data. During these measurements the GANDALF module is digitizing the data with a sampling rate of 1 GS/s.

To be able to rely on the measurement results and not to underlie digitization effects, the time between the two pulses $P1$ and $P2$ must sweep. Let t_i be the sampling times for the pulse given to channel $CH0$ and $CH1$ of the AMC respectively. The pulses from the two channels have an offset in time due to e.g. different cable lengths. This offset is expressed in c_{P1} and c_{P2}, respectively. If the time distance between the generated pulses is constant, the digitized values $f(t_i + c_{P1})$ and $f(t_i + c_{P2})$ will have a fixed relation:

$$f(t_i + c_{P1}) = f(t_i + c_{P2} + const.). \tag{5.11}$$

This can lead to systematic effects in case both pulses are digitized with the same correlated digitization scheme. To avoid this, a variable time offset between the two pulses is generated by the relation:

$$f(t_i + c_{P1}) = f(t_i + c_{P2} + sin(\omega_m t) \cdot \frac{t_{phase}}{2}), \tag{5.12}$$

where $\omega_m << 2\pi f_s$ is the sweep frequency which is an order of magnitude smaller than the sampling frequency f_s. The range wherein the sine functions are shifted to each other is $t_{phase} << t_s = 1/f_s$. This will guarantee that all digitization schemes for $t_i + \epsilon$ and $\epsilon \in [0, t_{i+1} - t_i]$ will occur for a set of measured events.

To implement this measurement configuration, a second function generator *AFG3251*[5] is used [95]. It generates a sine signal with a small frequency of $\omega_m = 193\,\text{mHz}$ compared to the sampling frequency of $f_s = 1\,\text{GHz}$. This signal can be fed to the external input of the *AFG3252* and defines the phase modulation and, therefore, the distance in time between the Moyal distribution pulses $P1$ and $P2$ (see Fig. 5.20).

Let assume an ideal measurement system; what one expects after filling the measured time differences into a histogram, is the sine density function:

$$p(t) = \frac{1}{\pi\sqrt{(B^2 - (t - T_{off})^2)}}\ , \tag{5.13}$$

where B is the time amplitude defined by the amplitude of the sine signal from the *AFG3251*, T_{off} the offset of the phase modulation sine function and t is the time difference of two signals.

In a real measurement system a finite time resolution is given and will smear the sine density. The convolution of the sine density function with a Gaussian distribution defined by the time resolution σ_t will be the expected measurement result. In Fig. 5.21 the sine density itself and some examples of Gaussian distributions of different widths convoluted with the sine density function are given. Here one can easily qualify the expected distributions shapes for an increasing time resolution σ_t.

As mentioned in 5.1.3, the time resolution of the algorithm directly depends on the amplitude of the input pulse. Therefore, measurements have been performed by screening the amplitudes of the pulses over the dynamic range of the digitization process. In Figs. 5.22 and 5.23 the result histograms are shown for pulses with $+2.3\,\text{V}$ (60% relative dynamic range) and $+90\,\text{mV}$ (2% relative dynamic range).
To obtain the time resolution of these measurements, a fit function $h(t)$ is defined which extracts the width σ_t of the Gaussian distribution used for the convolution:

$$h(t) = p(t) * g(t), \tag{5.14}$$

where

$$g(t) = \frac{1}{\sigma_t\sqrt{2\pi}} \exp\left(-\frac{1}{2}\left(\frac{t}{\sigma_t}\right)^2\right). \tag{5.15}$$

The results from the deconvolution method measurements are given in Fig. 5.24. The values obtained from the fit function for σ_t depending on the pulse amplitude are given. For a comparison the results from the simulations using random pulses (see section 5.1.3) are also plotted in this figure.

[5] Tektronix Inc.

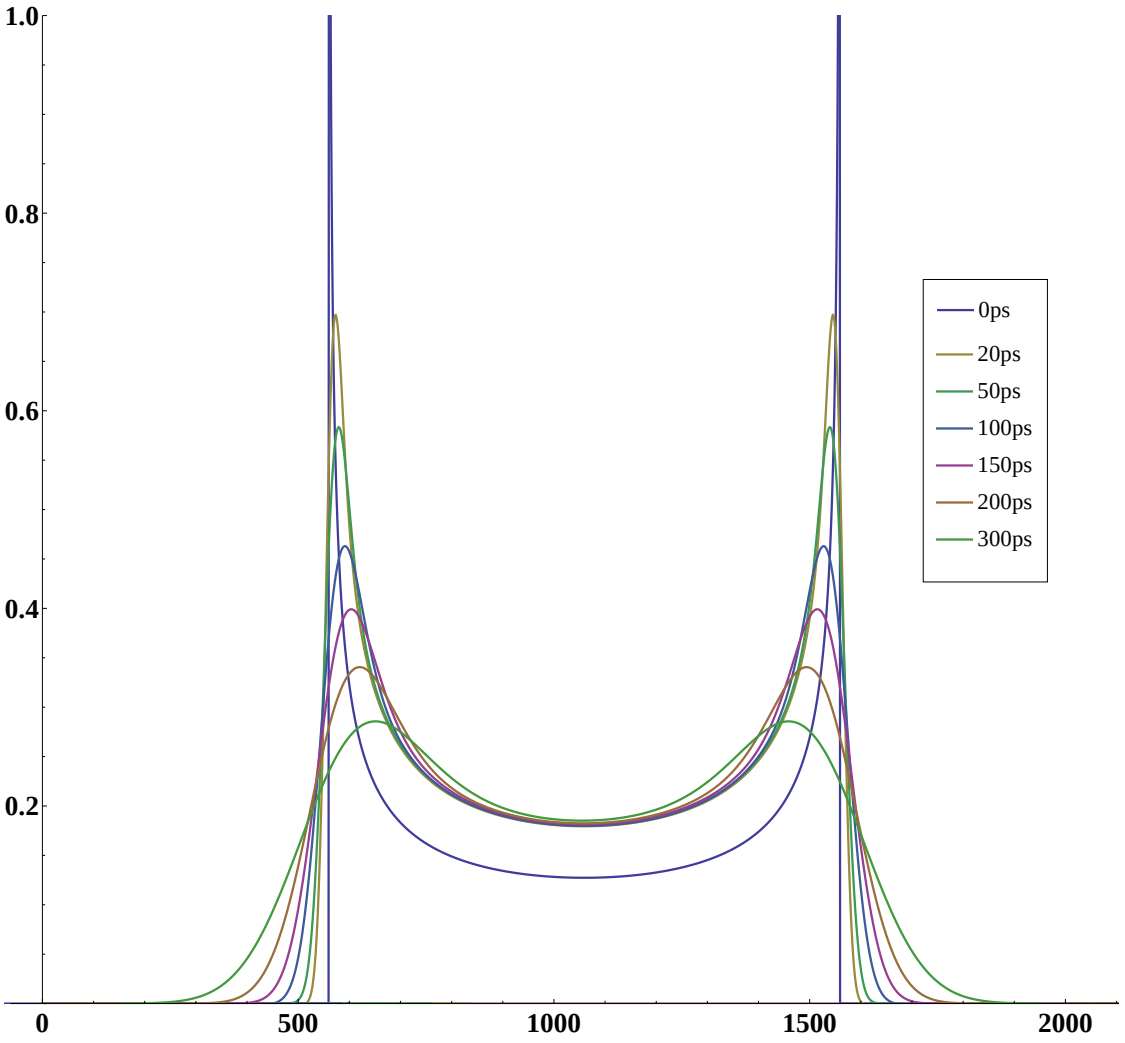


Figure 5.21: A normalized sine density function is plotted (blue) together with the sine density function convoluted with Gaussian functions of different widths: 20 ps, 50 ps, 100 ps, 150 ps, 200 ps, 300 ps.

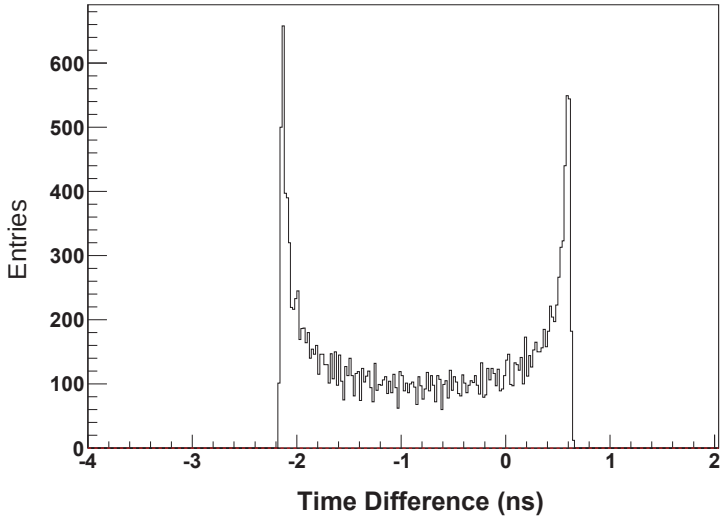


Figure 5.22: Result for the time differences using the deconvolution method measurement. The pulses used for these measurements have an amplitude of 2.3 V.

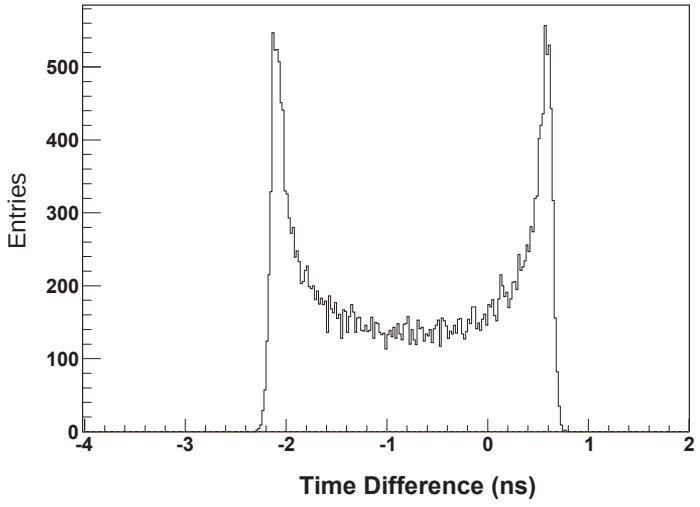


Figure 5.23: Result for the time differences using the deconvolution method measurement. The pulses used for these measurements have an amplitude of 90 mV.

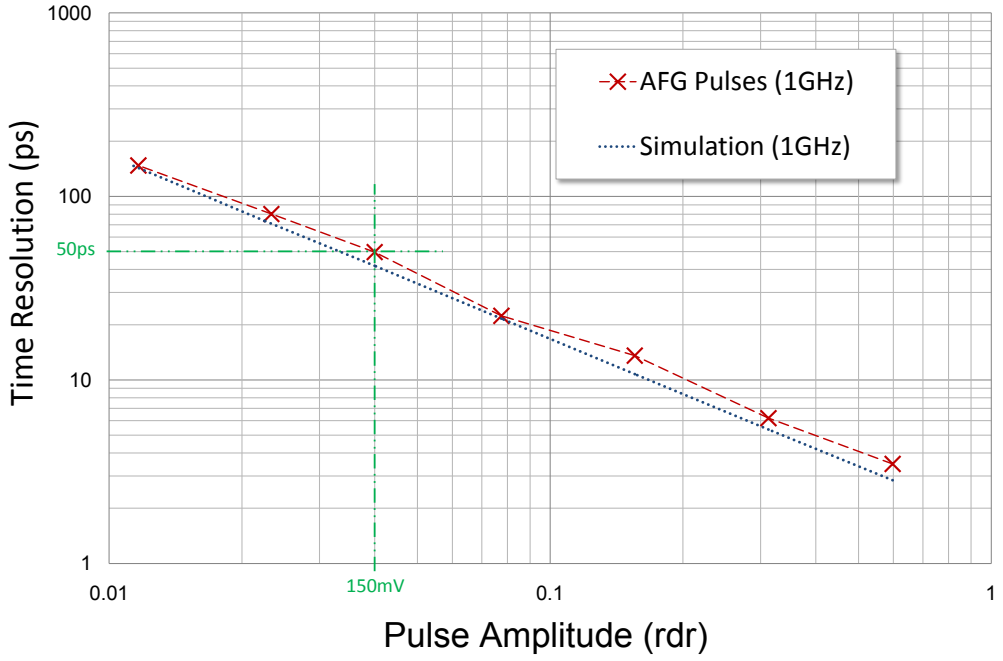


Figure 5.24: Measurement results for the time resolution performed with the deconvolution method. For different values of the relative dynamic range the width of the Gaussian distribution is plotted (red ×). The measurements were repeated until the statistical error has a negligible contribution. The error bars represent uncertainties obtained from the measurement of the amplitude and from the fit algorithm. The blue dotted line marks the simulation results obtained from random pulse generation (see section 5.1.3).

The same setup was used connecting the two signal inputs to two channels on two separated GANDALF modules. Here the TCS clock is transmitted to two modules via two separated optical fibers from the TCS system. The received clock signals are synchronous, but will obtain slight variations due to the separated clock signal transmission. The jitter on the clock input signal measured at the outputs of the optical receivers is of the order of $\sigma_{jitter} < 50\,\text{ps}$ but is improved with the $SI5326$ jitter attenuator chip located on each GANDALF module. As shown in Fig. 5.25 the time resolution for "board-to-board" measurements shows a worsening for pulses with amplitudes $A > 0.1\,\text{rdr}$ compared to the "same-board" measurements. The drop of the resolution in this region, where high time resolution can be achieved by the algorithm can be explained with a remaining jitter contribution from the TCS clock.

5.2.3 Comparison to the F1-TDC

To detect potential systematic effects in the time measurements with the GANDALF module operated as *transient analyzer* measurements with an independent unit were accomplished. To be able to quantify the high time resolution performance of the GANALF

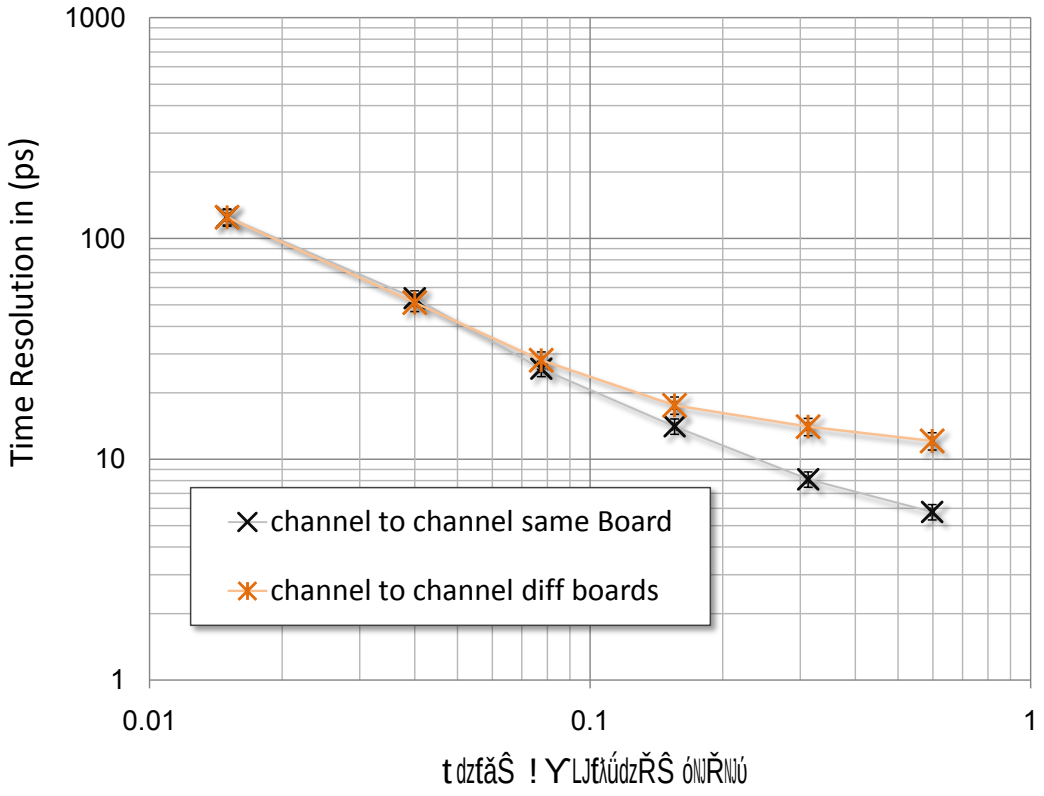


Figure 5.25: Measurement of the "board-to-board" time resolution. The black line gives the time resolution measured between two channels located on the same GANDALF module. The orange line represents the time resolution measured between two channels located on two different GANDALF modules. The pulses given to the analog input have a risetime of 3 ns and are sampled with 500 MS/s. The difference in the region of pulse amplitudes > 0.1 rdr can be explained by the remaining jitter contributions from the clock distribution with the TCS system.

module, a system has to be chosen which permits measurements in the sub nanosecond-range and also uses the same data acquisition environment for the comparison between measured times event by event.

The $\mathcal{F}$ 1-TDC used on a CATCH module was selected to perform a comparison measurement in the time resolution [101]. To be able to determine the time resolution of both measurement systems, the $\mathcal{F}$ 1-TDC and the GANDALF module, the measured times represented in two different data formats have to be transformed for a comparison (see section F.1.1, [73]). This transformation is possible as both digitization units use the same synchronous base clock (the experimental clock) to perform the time measurements.

The time-to-digital conversion used with the $\mathcal{F}$ 1-TDC is based on a subsection of the period of a clock signal with a frequency f_{PLL}. This clock signal is generated from the common base clock signal with frequency f_{base} (in the COMPASS environment $f_{base} =$

38.88 MHz) by selecting the multiplier M and the divisor N. The frequency f_{PLL} can be calculated with [102]:

$$f_{PLL} = \frac{2^{M_{LSB}} \times M}{2^N} \times k_{mode} \times f_{base}. \tag{5.16}$$

Due to the design of the $\mathcal{F}$1-TDC, the two least significant bits are not configurable. The multiplication factor, therefore, is $2^{M_{LSB}} \times M = 4 \times M$. The division factor is generated by a N bit counter; the division factor for the frequency f_{PLL} is 2^N. The factor k_{mode} is either 1 or 2 depending on the $\mathcal{F}$1-TDC is operated in normal or high resolution mode. In high resolution mode 2 TDC channels are combined to half the width of t_{bin} at a cost of reducing the number of signal inputs by a factor of 2.

For time measurements in the subrange of the period $t_{PLL} = \frac{1}{f_{PLL}}$ of the clock signal a subsection is done by generating a copy of n_{tap} clock signals delayed by delay taps as shown in Fig. 5.26. These clock signals are then transferred to the clock inputs of n_{tap} flip-flops. These flip-flops are now clocked with a time delay of t_{del} to each other. By connecting the data signal input to the inputs of the flip-flops, digital time information of a level change on the data signal input can be read from the group of all flip-flop outputs.

By calculating the time t_{del} generated by a single delay tap, the time bin t_{bin} of this digitization process can be determined. As both edges of the PLL clock are used to latch the flip-flops, the t_{del} is a fraction of T_{PLL} by two times the number of tabs n_{tap}:

$$t_{del} = t_{bin} = \frac{T_{PLL}}{2 \times n_{tap}} = \frac{1}{f_{PLL} \times 2 \times n_{tap}}, \tag{5.17}$$

$$t_{bin} = \frac{2^N}{f_{base} \times k_{mode} \times M \times 4 \times 2 \times n_{tap}}. \tag{5.18}$$

The data format of the $\mathcal{F}$1-TDC permits to transfer time data in 16 bit words. To guarantee the synchronization of the tap time information with an integer number $N_{T_{base}}$ of the base clock period T_{base}, different over-roll values $n_{roll,\mathcal{F}1} < 2^{16}$ have to be calculated in dependency on the time bin size t_{bin}:

$$n_{roll} = N_{T_{base}} \frac{k_{mode} \times M \times 4 \times 2 \times n_{tap}}{2^N}. \tag{5.19}$$

An example with typical values used with the $\mathcal{F}$1-TDC for a time binning of $t_{bin} = 112$ ps with $M = 96$, $N = 6$ is:

$$t_{bin} = \frac{2^6}{38.88\,\text{MHz} \times 96 \times 4 \times 2 \times 19} = 112.807\,\text{ps}, \tag{5.20}$$

$$\tag{5.21}$$

$$n_{roll} = 283\ \frac{96 \times 152}{2^6} = 64524. \tag{5.22}$$

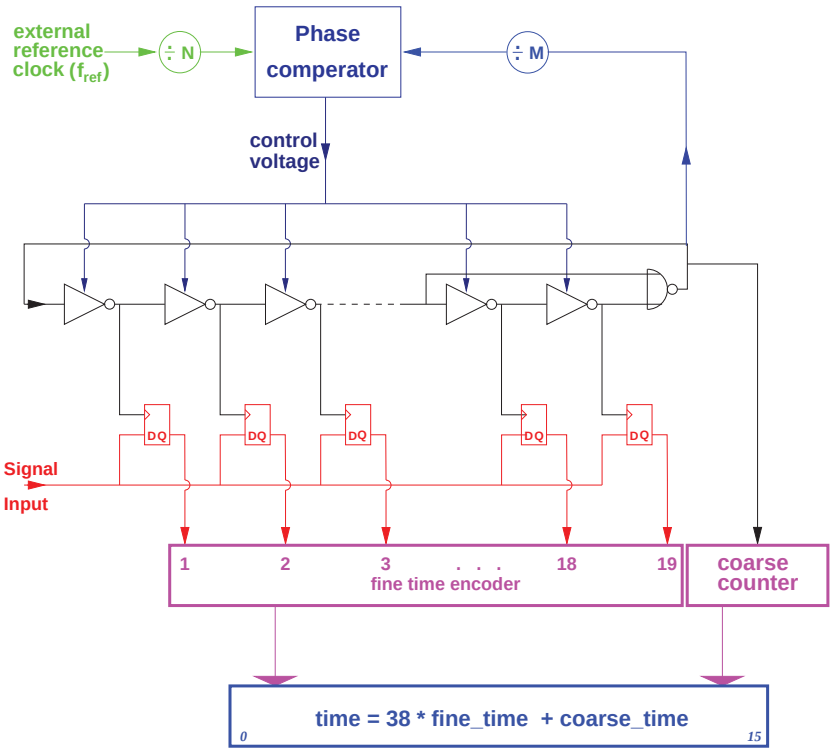


Figure 5.26: The base functionality of the $\mathcal{F}1$-TDC. By delaying the clock signal with the programmable frequency f_{PLL} by 19 taps, the flip-flops will give the time information in which of the $\frac{1}{19}$th time bin the input signal occurred [101].

The over-roll time due to the data format of the $\mathcal{F}1$-TDC, for this example is about $t_{roll,\mathcal{F}1} \approx 7.2\,\mu$s. As the data Format of the GANDALF module enables over-roll times of up to $t_{roll,G} \approx 550.0\,s$ (see section F.1.1), comparisons between the data can be performed by calculating the time information t_G given by the GANDALF module into a time information $t_{G\to\mathcal{F}1}$ in the $\mathcal{F}1$-TDC data format.

$$t_{G\to\mathcal{F}1} = \left(\frac{t_G}{k_G} \times \frac{k_{mode} \times M \times 152}{2^N}\right) \mod n_{roll,\mathcal{F}1}, \tag{5.23}$$

where t_G is the time given by the GANDALF module and k_G the factor defining the sampling frequency f_s of the ADCs:

$$f_s = k_G \times f_{base}. \tag{5.24}$$

The resolution $\sigma_{t,diff}$ of the measured time differences

$$t_{diff} = \left(t_{G\to\mathcal{F}1} - t_{\mathcal{F}1}\right), \tag{5.25}$$

permits a comparison of the two time measurement systems. Where $t_{G\to\mathcal{F}1}$ is the time of the pulse measured by the GANDALF in $\mathcal{F}$1data format and $t_{\mathcal{F}1}$ the time of the pulse from the discriminator measured by the $\mathcal{F}$1-TDC.

In Fig. 5.27 an overview of the measurement for the comparison with the $\mathcal{F}$1-TDC to the GANDALF module is given. The pulse shape for the comparison measurement is generated by an AFG3251 [95] and split with a power splitter [103] to provide one copy of the signal to an analog input channel of the GANDALF module and the second copy to the input of a LeCroy 623b discriminator [104]. The discriminator threshold was set to 50 mV and maximum amplitude of the Moyal function is set constantly to 70% rdr to avoid "time walk effects" caused by the discriminator. The logic pulse is then given to a digital input channel of the $\mathcal{F}$1-TDC via another GANDALF module equipped with a DMC. This permits a logic signal transformation from NIM to the LVDS standard with a minimum of additional jitter.

The base clock for both digitization processes is provided by an optical fiber TCS system (green lines in Fig. 5.27). The GANDALF module receives the clock signal via the GIMLI card (see section 4.1.3) and the $\mathcal{F}$1-TDC located on a CATCH module [105] via a TCS receiver transition card. A common acquisition system collects the data from the CATCH and the GANDALF module via the S-LINK interface [46].

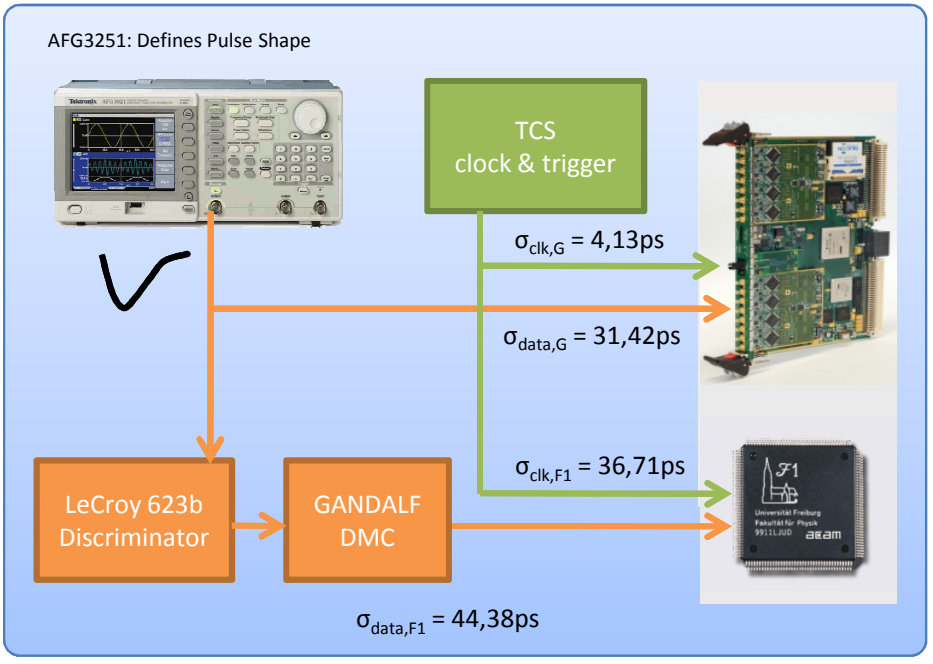


Figure 5.27: Schematic overview of the measurement setup for the comparison with the $\mathcal{F}$1-TDC.

To obtain the time resolution of the comparable time measurement units the time resolutions of the different clock and signal paths have to be determined. The total inaccuracy of the measurement can be summarized with:

$$\sigma_{t,diff} = \sigma_{data,G} \oplus \sigma_{clk,G} \oplus \sigma_{t,G} \oplus \sigma_{data,\mathcal{F}1} \oplus \sigma_{clk,\mathcal{F}1} \oplus \sigma_{t,\mathcal{F}1} \oplus \sigma_{system}, \tag{5.26}$$

where σ_{data} and σ_{clk} describe the uncertainties on the clock and data path for the GANDALF and the $\mathcal{F}$1-TDC setup. σ_t gives the uncertainties of the time measurements for the GANDALF module and the $\mathcal{F}$1-TDC itself. σ_{system} is the contribution caused by all remaining distortion effects which occur in the measurement system. This can be caused e.g. by power noise or ground differences between the electronic environments of the crates which house the GANDALF module and the CATCH module.

The uncertainties for the clock and data path were determined by using a *TDS6154C* oscilloscope, with a time resolution below 3 ps [106]. The contribution of $\sigma_{t,G}$ and $\sigma_{t,\mathcal{F}1}$ to the absolute time resolution $\sigma_{t,diff}$ measured with this setup can be determined by an additional measurement. Here the time difference between two channels connected to the GANDALF module and to the $\mathcal{F}$1-TDC is calculated each. The width of this distribution divided by $\sqrt{2}$ gives the resolution of a single ADC or TDC channel, assuming that the unique channels have the same resolution. In Tab. 5.3 the measurement results are concluded. With these values and equation (5.26), the contribution of the measurement setup can be estimated to be $\sigma_{system} < 29.4$ ps.

Table 5.3: Measured resolutions on clock, data paths and calculated resolutions for GANDALF module and $\mathcal{F}$1-TDC time measurements.

Contribution	Jitter (ps)	measured with
clk,$\mathcal{F}$1	36.71	TDS6154C
clk,G	4.13	TDS6154C
data,$\mathcal{F}$1	44.38	TDS6154C
data,G	31.42	TDS6154C
t,$\mathcal{F}$1	51.40	$\mathcal{F}$1-TDC
t,G	22.36	GANDALF

5.2.4 Pile Up Pulse Separation

The digital Constant Fraction algorithm described in section 5.1 was implemented in VHDL to perform the time extractions on the pulse shapes given to the GANDALF transient analyzer analog signal inputs. The algorithm implemented inside the FPGA also extends the capabilities to extract times from near following piled-up pulses. To verify this implementation and to permit a comparison to the simulations performed in section 5.1.4, a dedicated measurement setup was generated. An *AFG3251* and an *AFG3252* arbitrary function generator were used to artificially generate piled-up pulses [95, 100]. The variable mathematical description of pulse with (5.1) was programmed

with the *NI Signal Express* and loaded into the function generators using the *TekVisa* interface [107, 108]. In Fig. 5.28 an overview of the measurement setup is shown. The generated piled-up pulses with programmable amplitudes and time distances are given to an analog input signal of the GANDALF module. As a reference a copy of the first pulse is used and connected to another analog input of the GANDALF module.

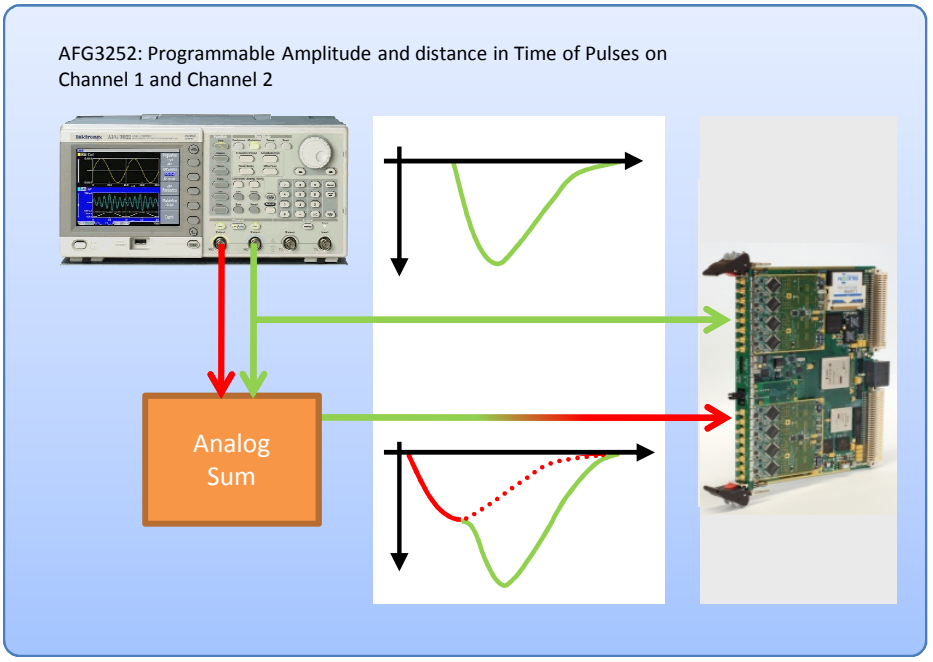


Figure 5.28: Schematic overview of the setup for the pile-up pulse measurement. The Moyal distribution pulse shape function (5.1) was generated on the outputs 1 and 2 of the *AFG3252* with a programmable delay between the outputs (green and red line). The pulses are combined using an analog sum [103].The therewith generated pile-up pulses are given to an analog input of the GANDALF module. As a reference a copy of one single pulse signal (green line) is given to another analog input of the GANDALF module.

The measurement result is plotted in Fig. 5.29. The measurement results show a comparable behavior for the pulse separation capability of the algorithm. The shortest time distances between two consecutive pulses t_{res} can be resolved for $A_{rel} \approx 1.5$. Also the slope of t_{res} for $A_{rel} < 1.5$ and $A_{rel} > 1.5$ is comparable to the simulation results given in section 5.13.

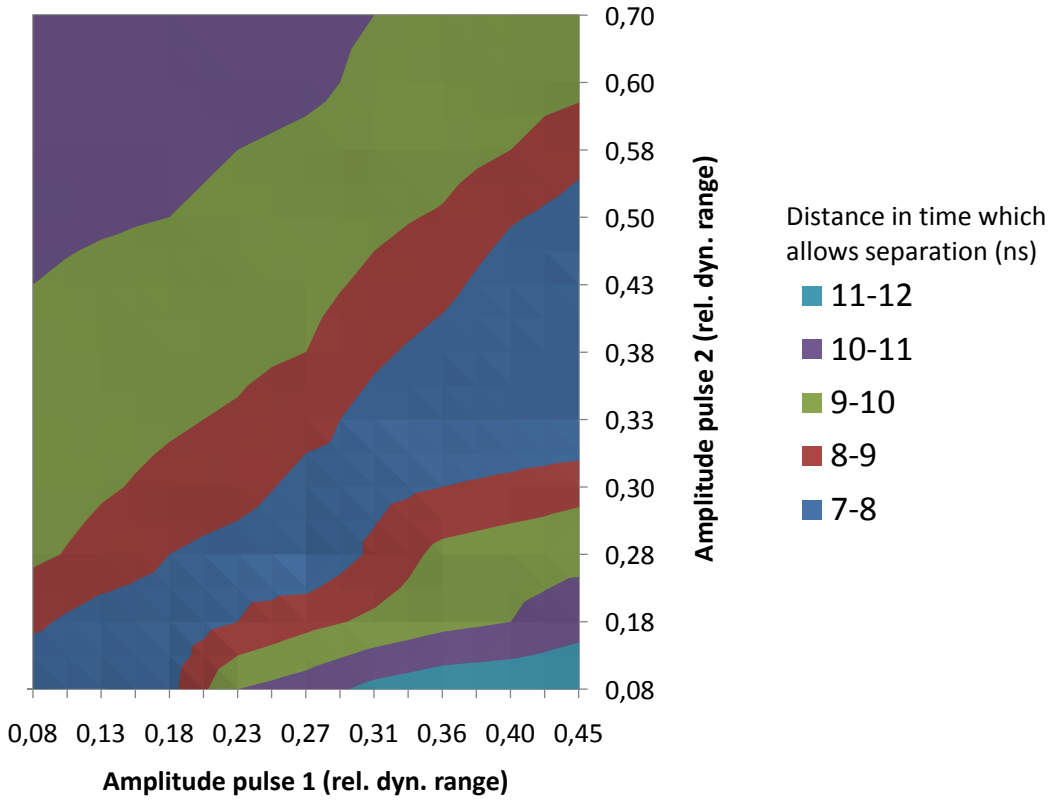


Figure 5.29: Measurement results for the resolution of two consecutive pulses. The x axis gives the amplitude of the first pulse, the y axis the amplitude of the second pulse. The values are given in relative dynamic range. Due to the power limitation of the outputs of the *AFG3252* the measurements were performed to amplitude ranges up to 45% and 70% for pulse 1 and 2, respectively. The z axis gives the minimum distance in time between the two pulses, if the algorithm is able to separate them. The pulses have a risetime of 3 ns and are sampled with 500 MS/s.

5.2.5 Measurements with a Laser pulsed PMT

To verify that the GANDALF module, used as a transient analyzer, reaches comparable precisions for the time resolution when connected to photomultipliers instead to the arbitrary function generator, another measurement described in Fig. 5.30 was set up. Here the signal source is a *R1450* PMT which was selected due to its fast rise time [109]. The spectral range of this PMT is 350 nm to 650 nm and the rise time is specified to $t_{rise} = 1.9$ ns. Such fast rise times could only be caught with a sampling frequency of $f_s > 1$ GHz (see section 4.1.3).

As a light source for the PMT a Laser, *PiL040* Optical Head, with a center wavelength of $\lambda_{center} = 408$ nm was chosen. The optical head is controlled by PiLas Digital Control Unit *EIG1000D* [110]. This unit generates short pulses with a width of < 45 ps. The

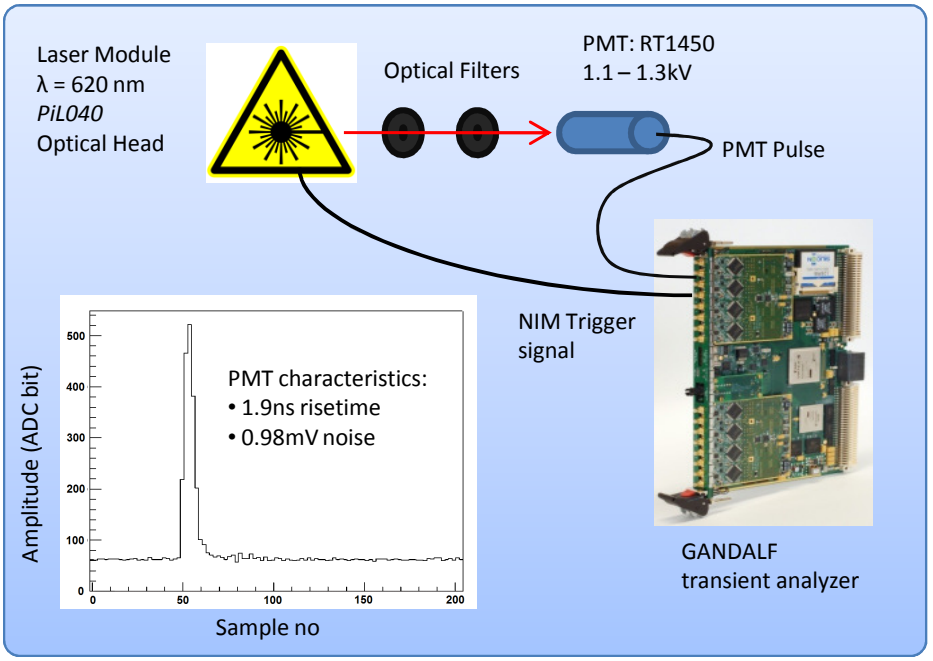


Figure 5.30: Schematic overview of the setup for the laser pulsed PMT measurement. The pulse from the PMT and the trigger of the *PiLas Digital Control Unit* are given to the analog inputs of the GANDALF module. In the lower left of this schematic an example pulse recorded with 1 GS/s by the GANDALF module is plotted.

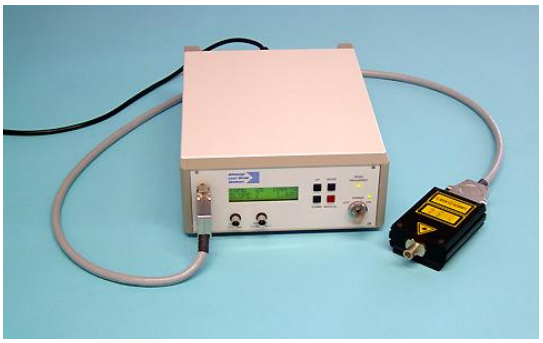


Figure 5.31: Picture of the *EIG1000D* Digital Control Unit with a *PiL040* Optical Head [110].

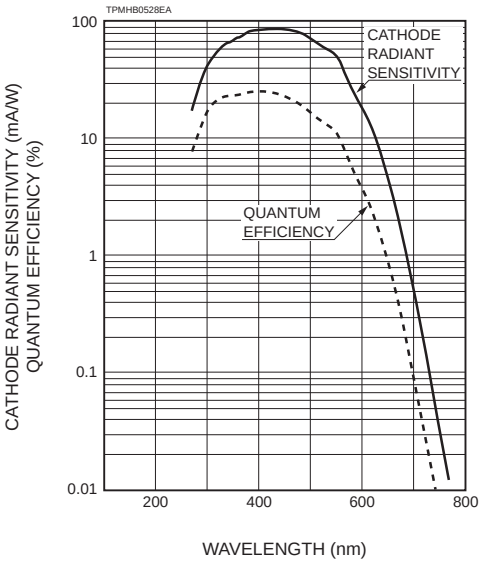


Figure 5.32: Quantum efficiency of the *R1450* photo multiplier tube [109].

repetition rate can be selected in steps from 1 kHz up to 1 MHz. The intensity of the light pulses can be set to a relative value of the maximum pulse energy. This can be used to define the maximum amplitude value for the pulses generated at the PMT output.

The PiLas Digital Control Unit *EIG1000D* has an external electrical output (TTL) signalizing a trigger relative to the emitted light pulse. The time jitter between the emitted light pulse and the TTL trigger is specified to < 3 ps. This signal is used as time reference for the measurement.

A schematic overview of the measurement is given in Fig. 5.30. The optical head was mounted to an optical bank together with optical filters ($R = 0.5$) for signal attenuation and apertures to minimize reflections along the optical path. The filters and apertures were mechanically mounted into a metal tube which helped to shield the system from external light sources.

For a characterization of the total jitter of the system including the PiLas Digital Control Unit, the optical head and the photo multiplier, a high precision measurement with the *TDS6154C* oscilloscope, was performed at a sampling rate of 40 GS/s by comparing the PMT output signal with the TTL trigger signal [106]. The system jitter of this setup was determined to $\sigma_{sys} = 39.8$ ps.

For the measurement with the GANDALF module the PMT output and the TTL signal were connected to two analog input channels. To characterize the time resolution in dependency on the dynamic range of the digitization unit of the AMC, the light pulse intensity defined by the PiLas Digital Control Unit was varied. The measured times for the resulting PMT signal and the TTL trigger signal were recorded by the

data acquisition system. In Fig. 5.33 the results from the off line analysis for the time resolution are plotted. The relative dynamic range is here defined from the voltage range of $-4.0\,\mathrm{V}$ to $0.0\,\mathrm{V}$. The red crosses show the measured time resolution for the given relative amplitude. The green dashed line shows the system jitter $\sigma_{sys} = 39.8\,\mathrm{ps}$ and the blue dashed line gives the simulation results for pulses with a rise time of $t_{rise} = 1.9\,\mathrm{ns}$ (see section 5.1.3). The red dashed line is corresponding to the squared sum of the system jitter with the simulated contribution.

To conclude the measurements performed with the GANDALF *transient analyzer*, the following results can be summarized:
As learned from section 5.1.1 the bandwidth of the pulses expected from the CAMERA detector with a rise time of 3 ns is $f_{BW} < 200\,\mathrm{MHz}$. With the measurements described in section 5.2.1 it is verified, that the signal-to-noise ratio of the analog input circuit is better than 62 dB for this frequency band.
The time resolution of the algorithms predicted in section 5.1.3 could be approved by the measurement results in section 5.2.2. The time resolution of the GANDALF *transient analyzer* is significantly better than the time resolution of the CAMERA detector ($\approx 200\,\mathrm{ps}$). The capability of the dCF algorithm to separate near following pulses was first simulated in section 5.1.4 and could be confirmed by measurements given in section 5.2.4.

For the exclusion of systematic effects on the time measurement setup the $\mathcal{F}$1-TDC was used as an independent reference system. As described in section 5.2.3 the predicted time resolutions of the GANDALF *transient analyzer* could be verified. To test the GANDALF module with PMTs a measurement setup consisting of a Laser pulser and a PMT generating pulses with fast risetimes was operated. The results of this measurement, given in section 5.2.5, are in conformance with the simulation results.

With the verification of the mentioned measurements the expectations on the GANDALF *transient analyzer* are complied. The production of 12 modules including the analog mezzanine cards is accomplished. The boards are commissioned and ready for operation as electronic readout system for the CAMERA detector.

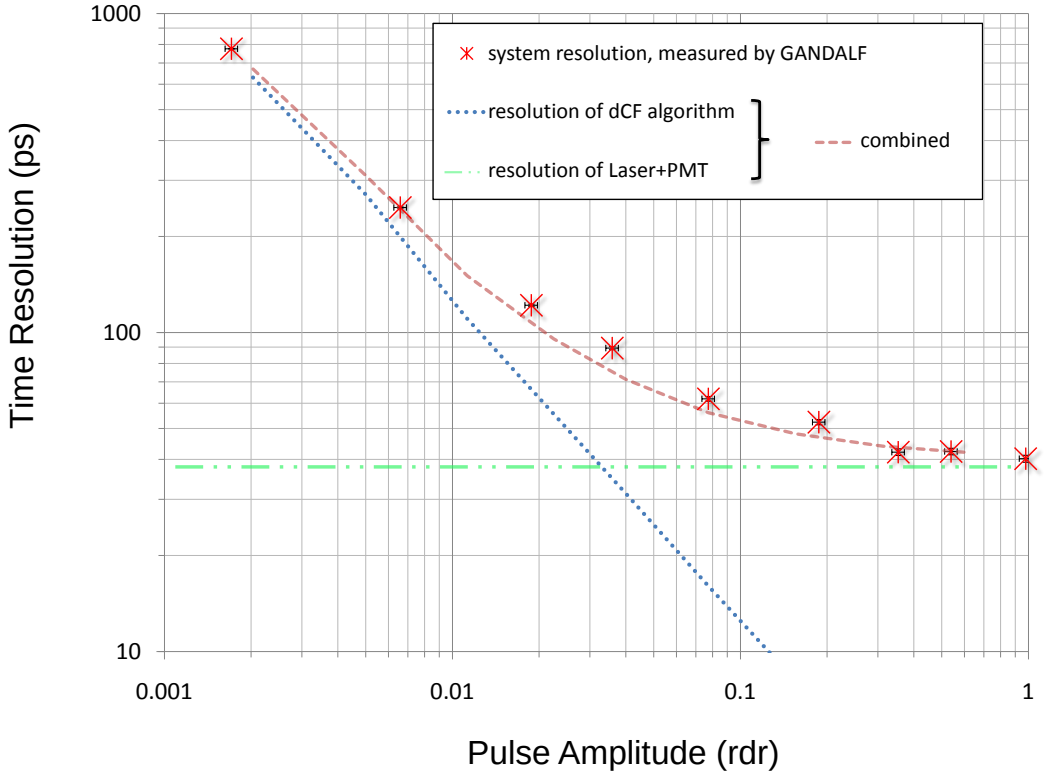


Figure 5.33: Measurement result for the time resolution using a *PiL040* Optical Head and a *R1450* PMT system as signal source. The red crosses give the measured time resolution for the time difference between the signal from the PMT and the TTL trigger of the PiLas Digital Control Unit (*EIG1000D*) for the given relative amplitude. The green dashed line shows the system jitter $\sigma_{sys} = 39.8\,\text{ps}$ measured with a *TDS6154C* oscilloscope and the blue dashed line gives the simulation results for pulses with a rise time of $t_{rise} = 1.9\,\text{ns}$ (see section 5.1.3), [106]. The red dashed line is corresponding to the squared sum of the system jitter with the simulated contribution.

6. Summary

Since the approval of the COMPASS-II proposal by the SPSC in May 2010, the work towards the investigation of the nucleon spin structure has been proceeding. In order to determine the contribution of the angular momentum distribution of quarks to the total spin of the nucleon, measurements to constrain GPD are foreseen. An upgrade of the spectrometer and the target region of the COMPASS experiment comes along with these measurements.

The collaboration plans to have a test period for the DVCS measurements in 2012 and two years of data taking during the following years. For the measurement of exclusive DVCS events with the COMPASS-II spectrometer, efforts are focused on the extension of the existing electromagnetic calorimeters and the construction of the CAMERA detector. The detection of final states from scattering processes in the COMPASS-II spectrometer has to reach a time resolution of 200 ps to reconstruct the exclusive Deeply Virtual Compton Scattering process: $\mu p \rightarrow \mu p \gamma$. With the aim of improving the efficiency in measuring DVCS processes, it will be an advantage to gain detailed information about the recoiled protons detected inside the CAMERA detector. This detector can provide information about the energy deposition and time-of-flight of particles passing trough and, therefore, can be used for particle identification.

In order to increase the efficiency of this separation, near following pulses have to be resolved due to the expected background of the detector from δ-electrons and beam halo. In addition, to generate a trigger signal on the recoiled protons the combination of all detector channel information is required. With the time information of the incoming beam muon and the time of the recoiled proton at the scattering vertex a trigger on time coincidence is possible.

With the intention to cover these different challenging readout tasks, the GANDALF framework has been designed and developed. Used as a *transient analyzer* module it accomplishes all challenges to operate as an electronic readout system and is part of a first level trigger for the CAMERA detector based on the recoil particle:

- The analog input circuits of the implemented AMCs cover the bandwidth of the expected pulse shapes (≈ 200 MHz). The low noise behavior of the input circuit was shown, as the signal-to-noise ratio is better than 62 dB.
- The resolution of 50 ps for the measured times of the expected detector pulse shapes are significantly better than the time resolution of the detector. This statement holds for pulses with rise times of 2.0 ns and signal amplitudes in the range of 5% to 100% of the relative dynamic range of the ADC.

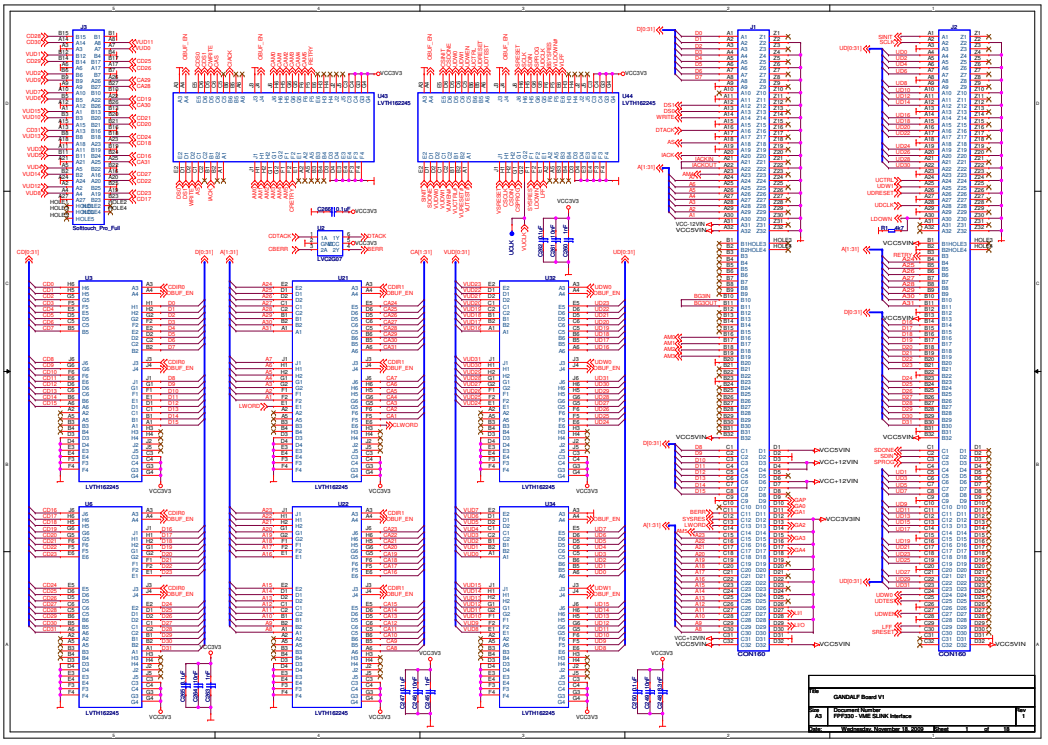
- The calculation of these times can be performed online, without introducing any dead time, using the *digital Constant Fraction* algorithm implemented in the DSP-FPGA. This algorithm is capable of separating pile-up pulses.
- The capability of the GANDALF module to communicate with the TIGER module is given by including the interface to the VITA41.0/VXS backplane bus. Hence, the data collected by the entire CAMERA detector equipped with GANDALF modules, can be used to generate a trigger signal on geometric, energy deposition and time information. The development of the first level trigger module is ongoing.

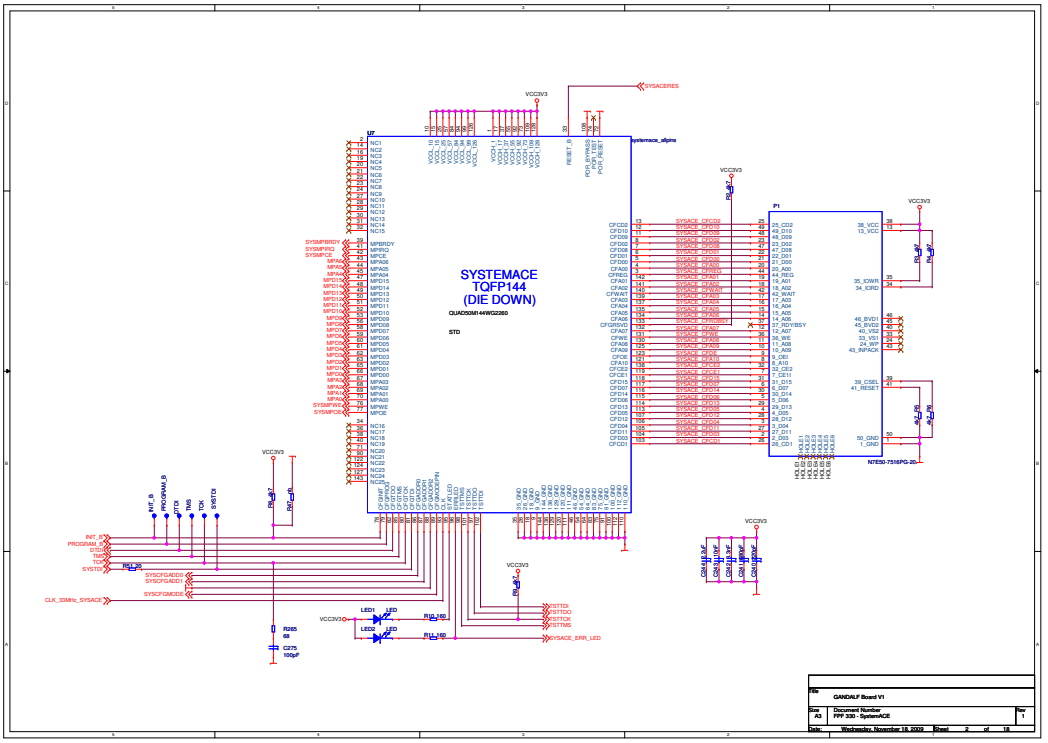
The research done within the frame of this thesis has shown that the GANDALF framework is able to perform the electronic read-out of the CAMERA detector with the defined specifications and required precision. The development of this read-out module was started from scratch and has reached its finalized state. Together with the central TIGER module, the possibility to combine precise information from the CAMERA detector will improve the separation of recoiled protons from background and, therefore, the detection of DVCS events. As the beam period of a full year is needed to obtain some hundreds of exclusive $\mu p \rightarrow \mu p \gamma$ events, an increase of the CAMERA detector efficiency and purity will optimize the statistics uncertainty of the measurement to constraint GPD.
In other words: With *GANDALF linked to the Rings* of the CAMERA detector, the next step towards the solution of the *spin puzzle* will become possible.

During the development on the GANDALF framework, a variety of additional applications in nuclear and particle physics became obvious due to its modularity. With the free programmability of the FPGAs and by replacing the analog mezzanine card by a digital mezzanine card the functionality of the module can be changed completely. Different readout tasks such as for example a 128 channel TDC with 160 ps digitization steps, 128 channel meantimer functionality and logic matrices for hodoscope triggers decisions have already been implemented successfully into the GANDALF module [42, 71]. This variety of potential fields of application including the given performance as a *transient analyzer*, distinguishes the GANDALF module a high performance electronic readout framework for high energy physics.

A. Appendix: PCB Design

A.1 GANDALF Schematics

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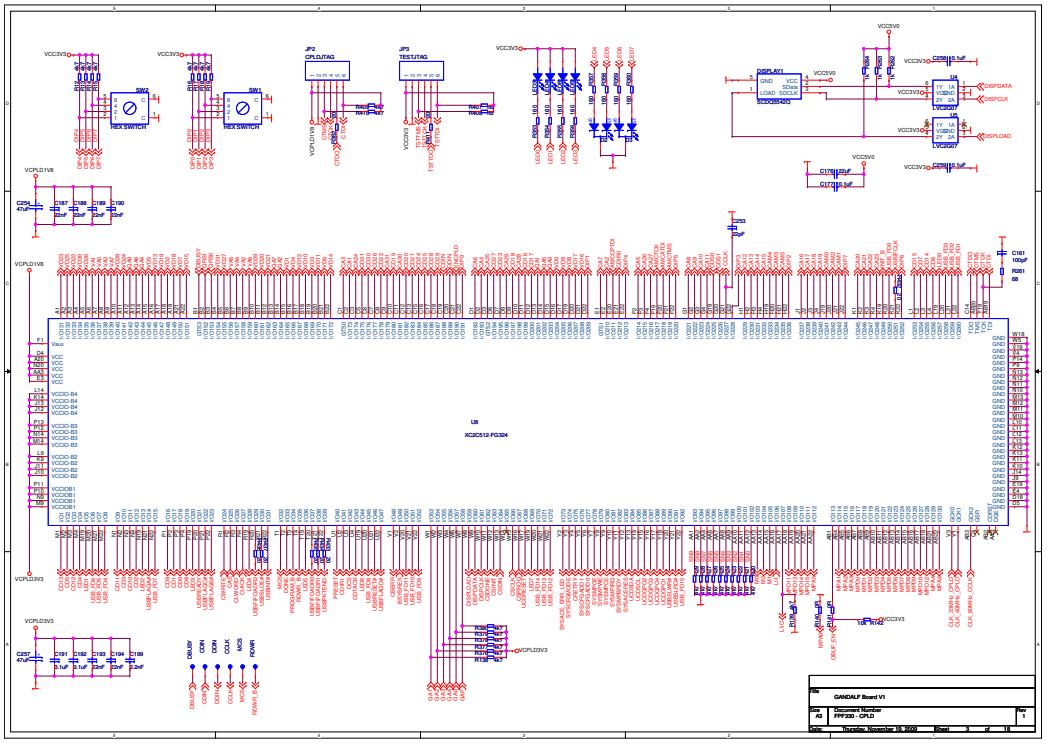
STD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TEST/JTAG
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GANDALF Board V1
Document Number
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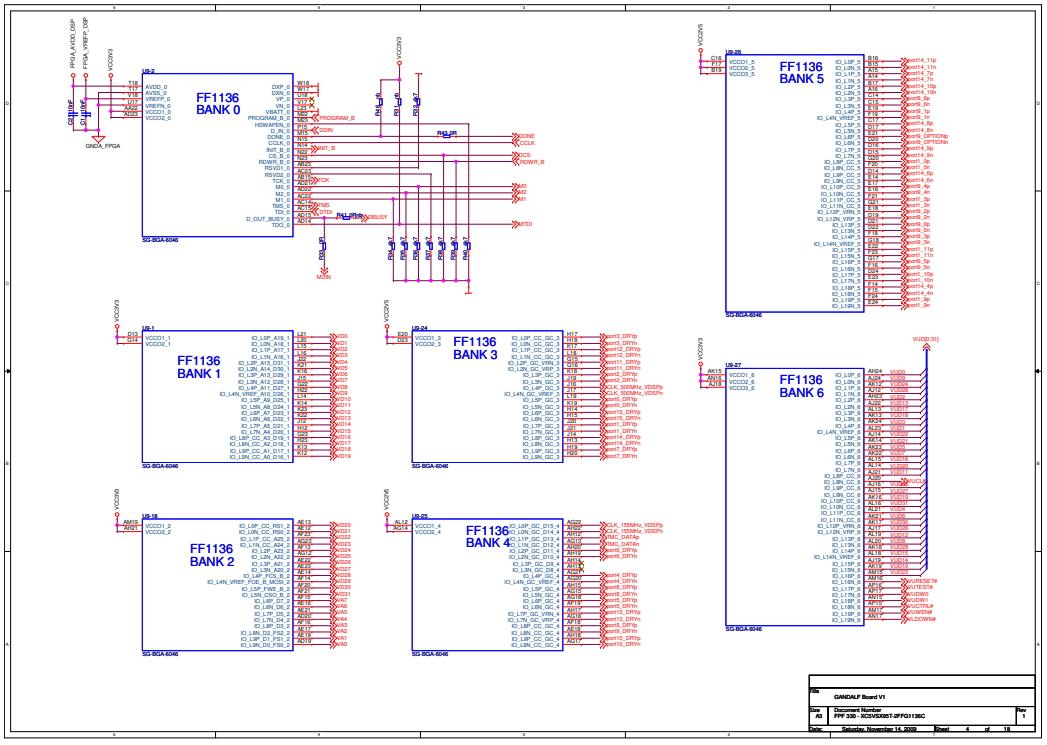
Thursday, November 19, 2009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BANK 5
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BANK 6
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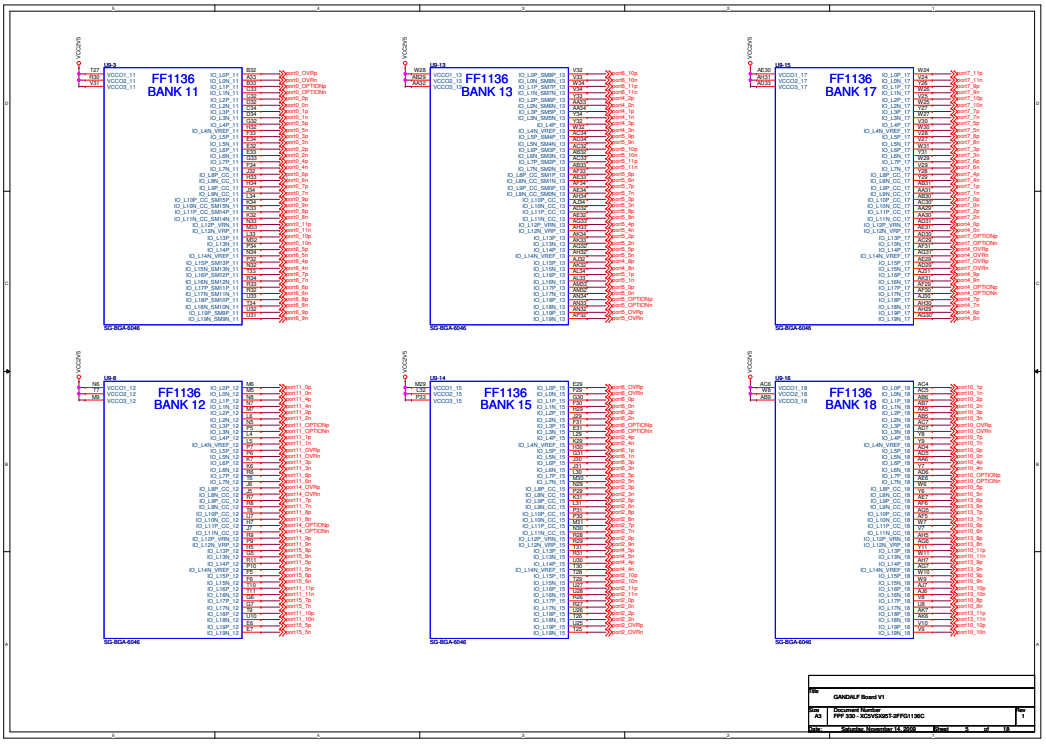
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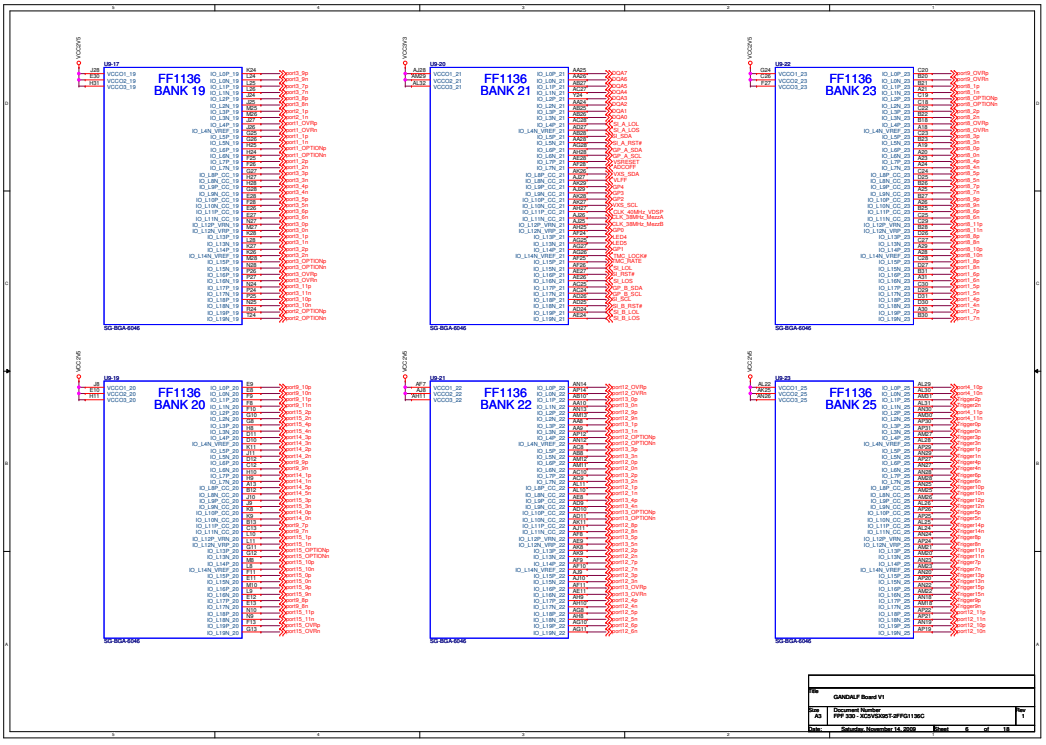
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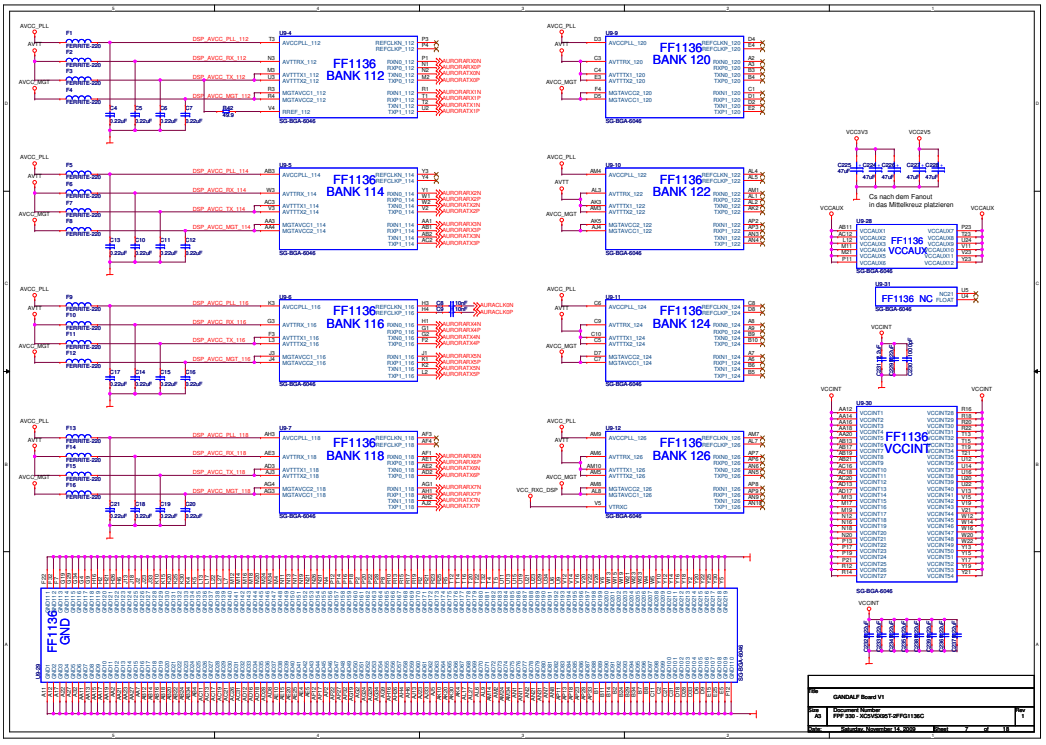
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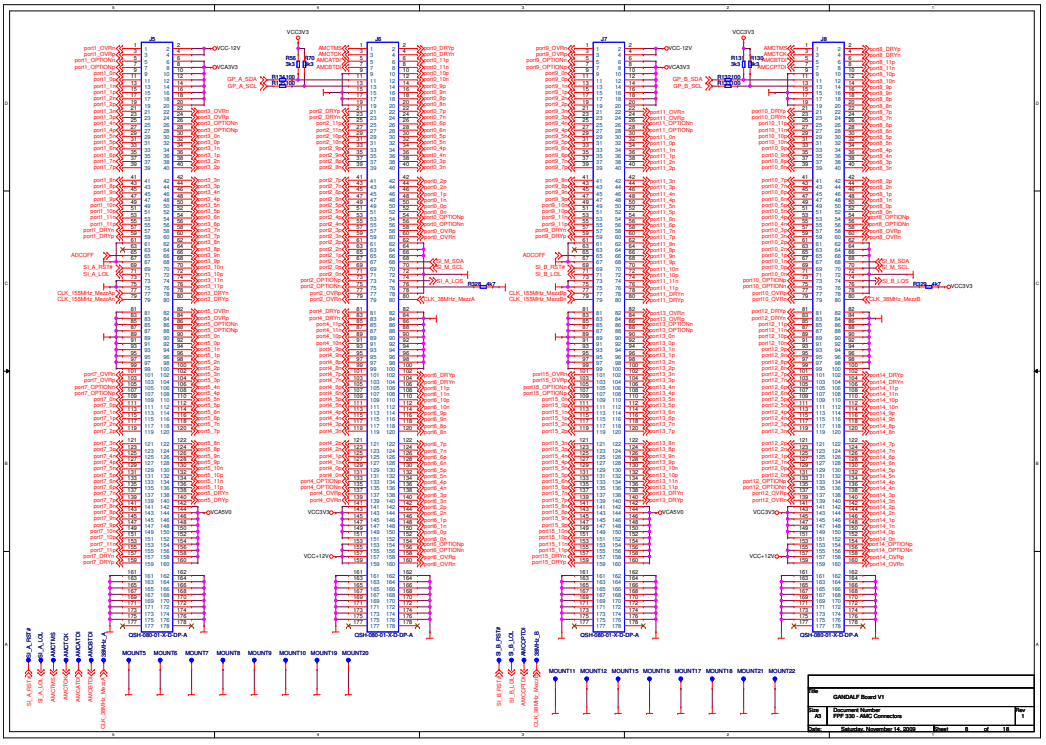
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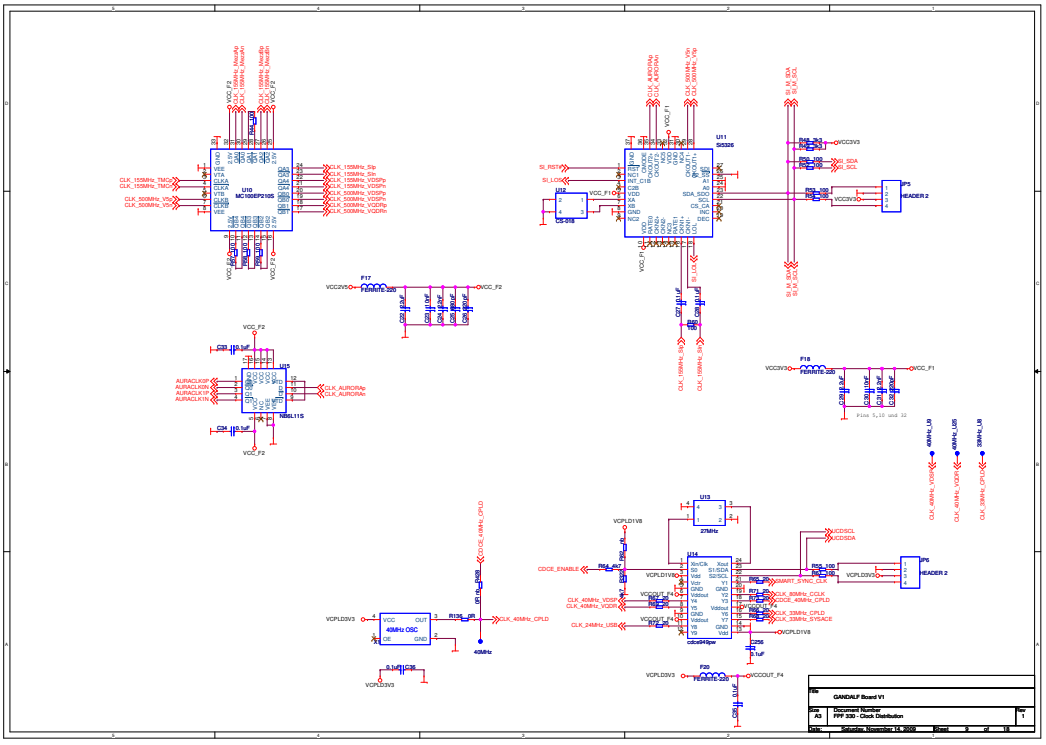

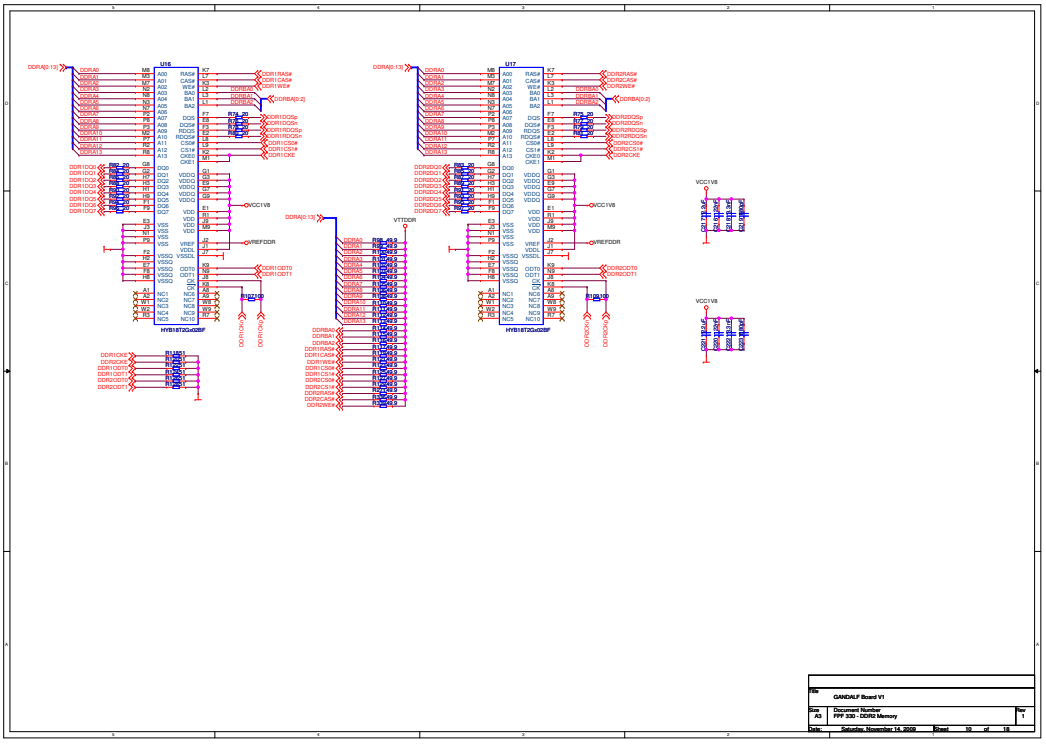

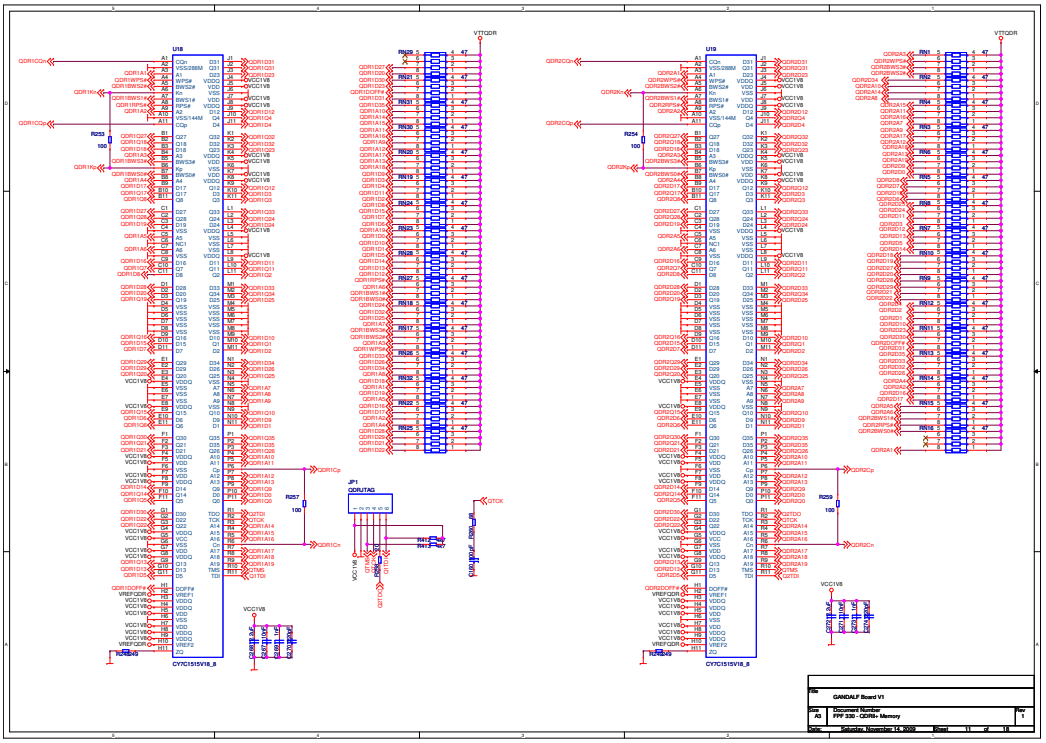

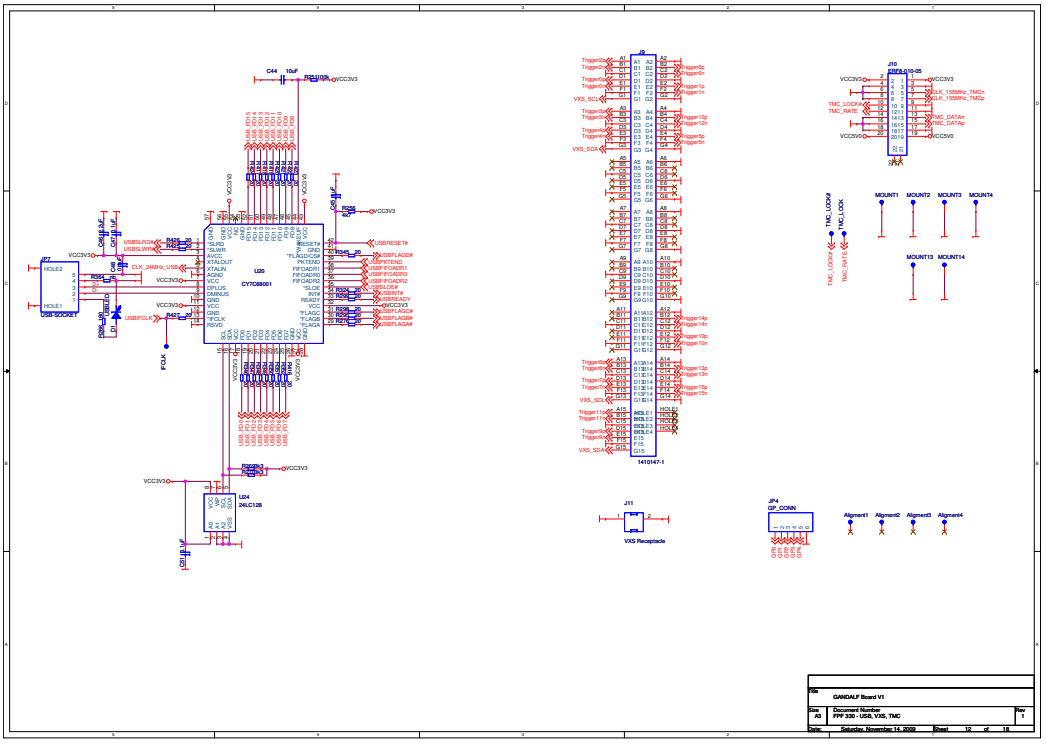

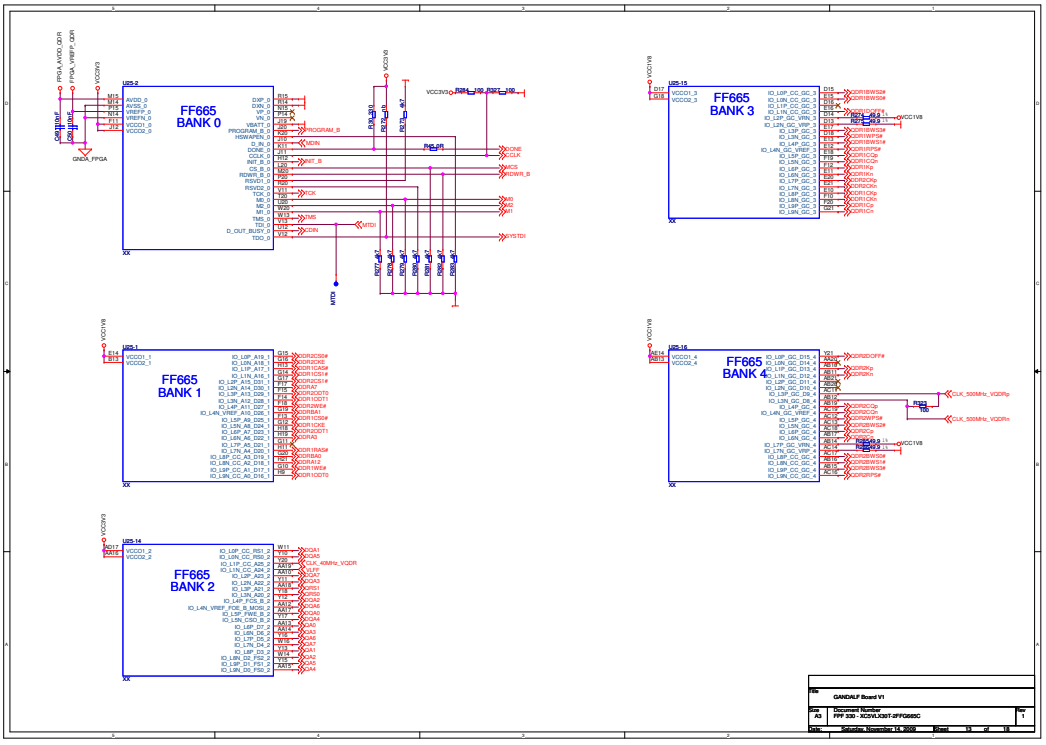
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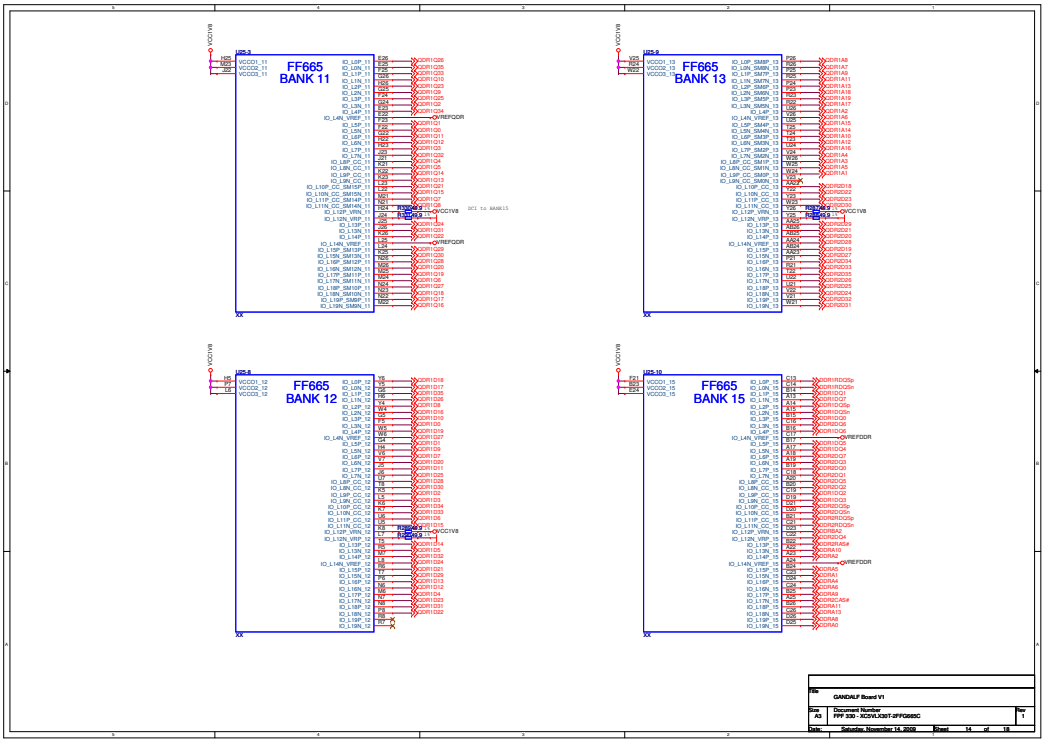
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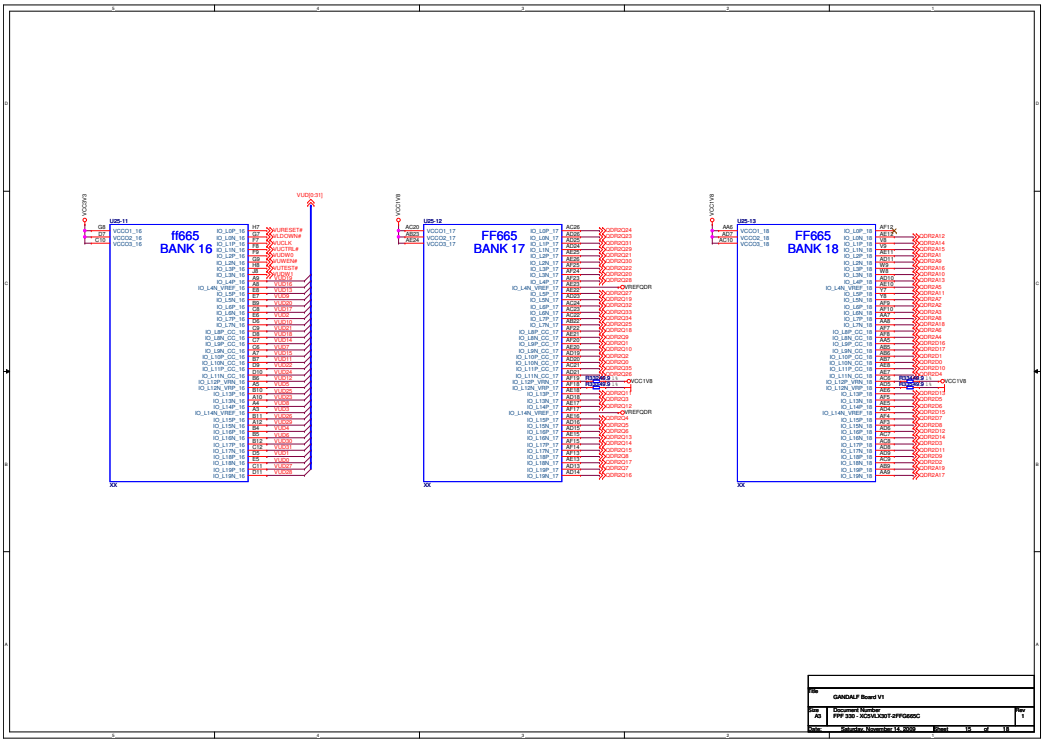
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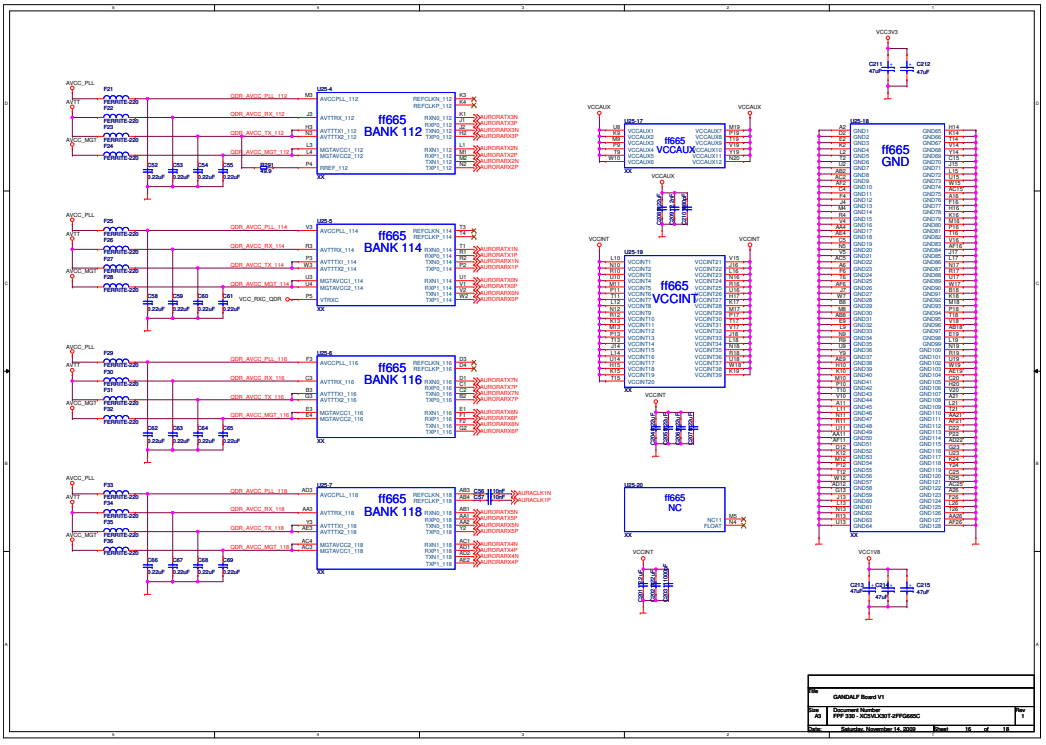
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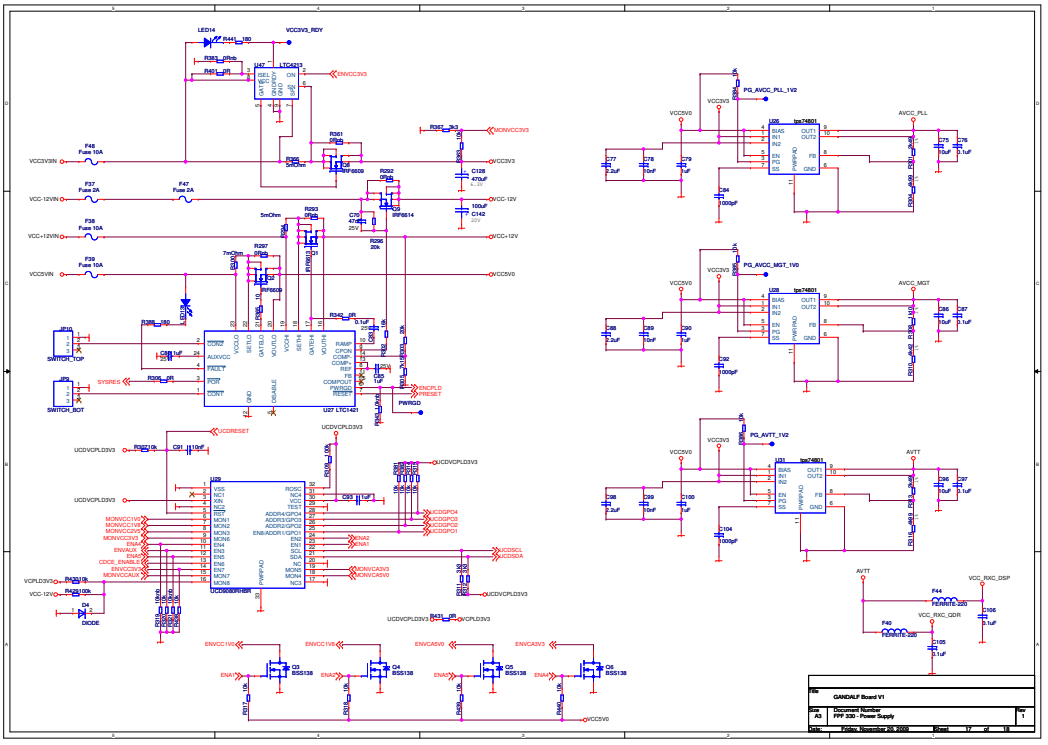

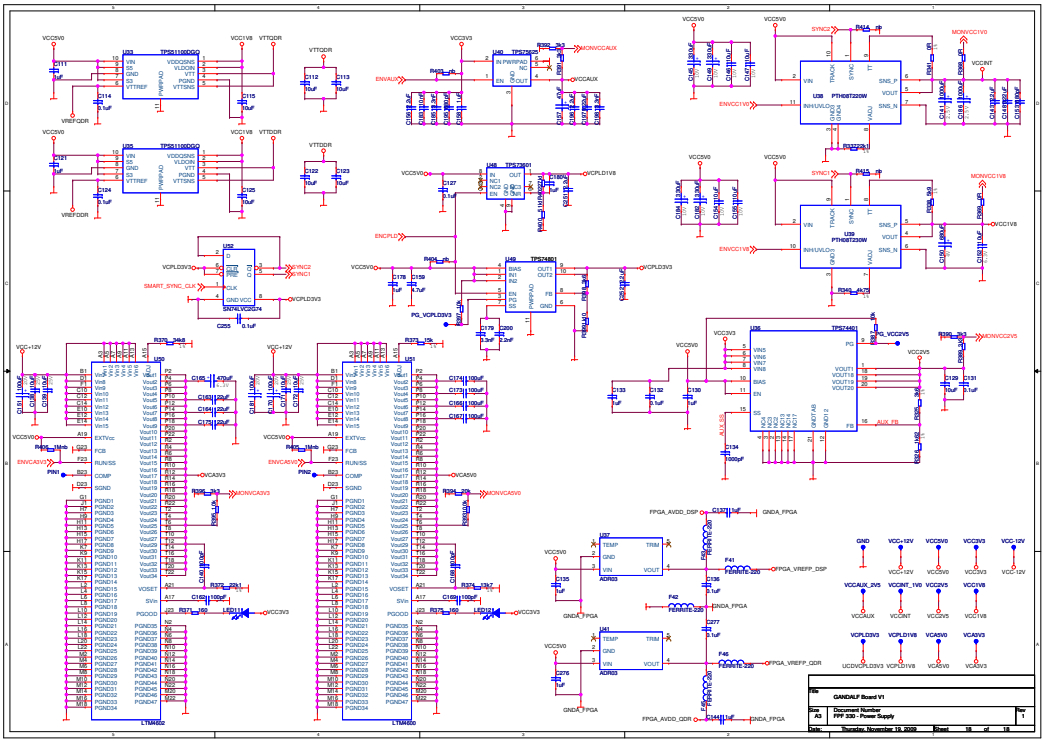

A.2 GANDALF PCB Stackup

Table A.1: Stack-up of the 14 layer GANDALF PCB. Total thickness ≈ 1.8 mm.

Layer	Type	Material	Thickness (μm)
SLDMSK	dielectric	polymer	40
TOP	conductor	copper	42
	dielectric	FR-4	60
GND1	plane	copper	17
	dielectric	FR-4	100
SIG2	conductor	copper	17
	dielectric	FR-4	160
SIG3	conductor	copper	17
	dielectric	FR-4	100
VCC1	plane	copper	17
	dielectric	FR-4	50
GND2	plane	copper	17
	dielectric	FR-4	100
SIG4	plane	copper	17
	dielectric	FR-4	160
SIG5	plane	copper	17
	dielectric	FR-4	100
GND3	conductor	copper	17
	dielectric	FR-4	50
VCC2	conductor	copper	17
	dielectric	FR-4	100
SIG6	plane	copper	17
	dielectric	FR-4	160
SIG7	conductor	copper	17
	dielectric	FR-4	100
GND4	plane	copper	17
	dielectric	FR-4	60
BOT	conductor	copper	42
SLDMSK	dielectric	polymer	40

Table A.2: Width and distance for differential pair signals for impedance defined conductors on the GANDALF module.

	Impedance	Width (μm)	Distance (μm)
differential (normal)	100 Ω	100	200
differential (neck mode)	97 Ω	95	120
single ended	50 Ω	100	

A.3 GANDALF PCB Layers

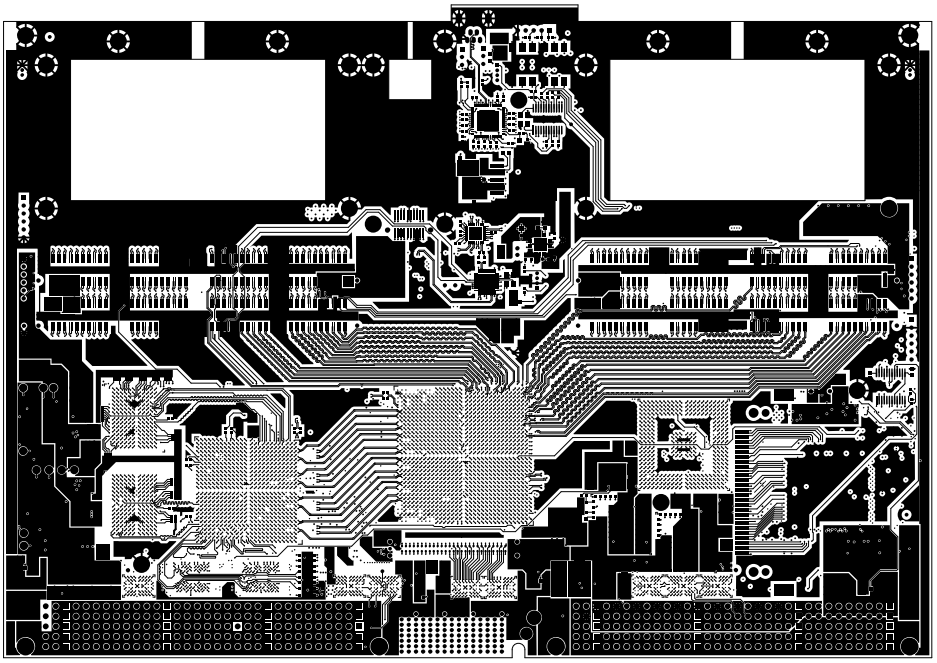

Figure A.1: Layer TOP of the GANDALF PCB.

Figure A.2: Layer GND1 of the GANDALF PCB.

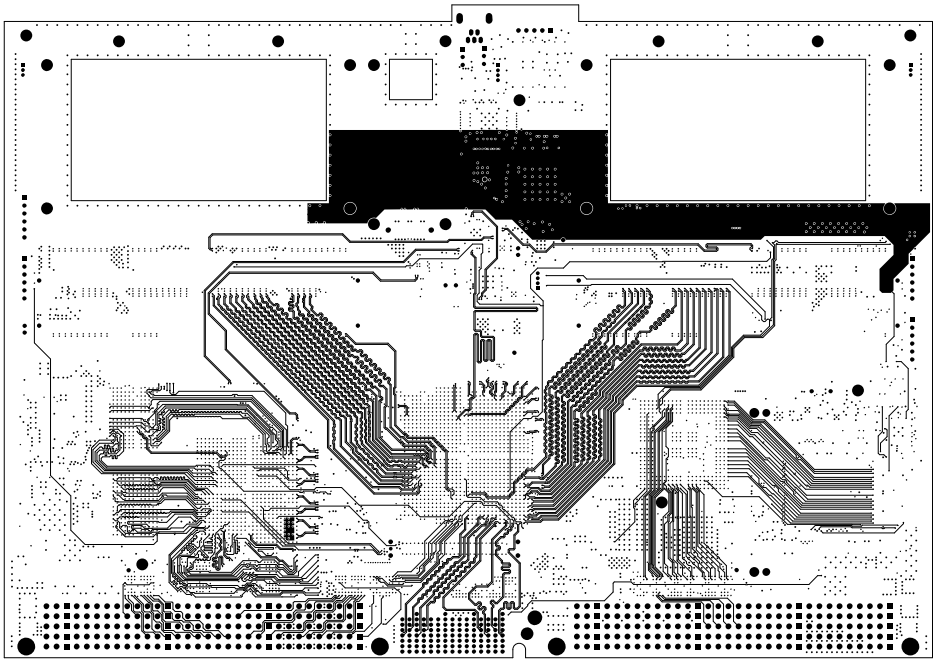

Figure A.3: Layer SIG2 of the GANDALF PCB.

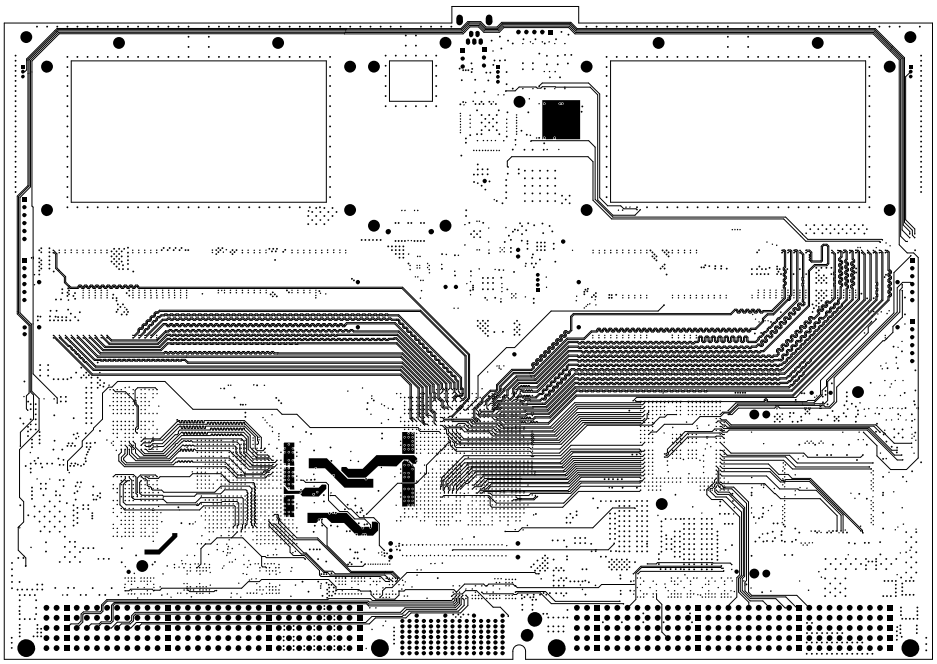

Figure A.4: Layer SIG3 of the GANDALF PCB.

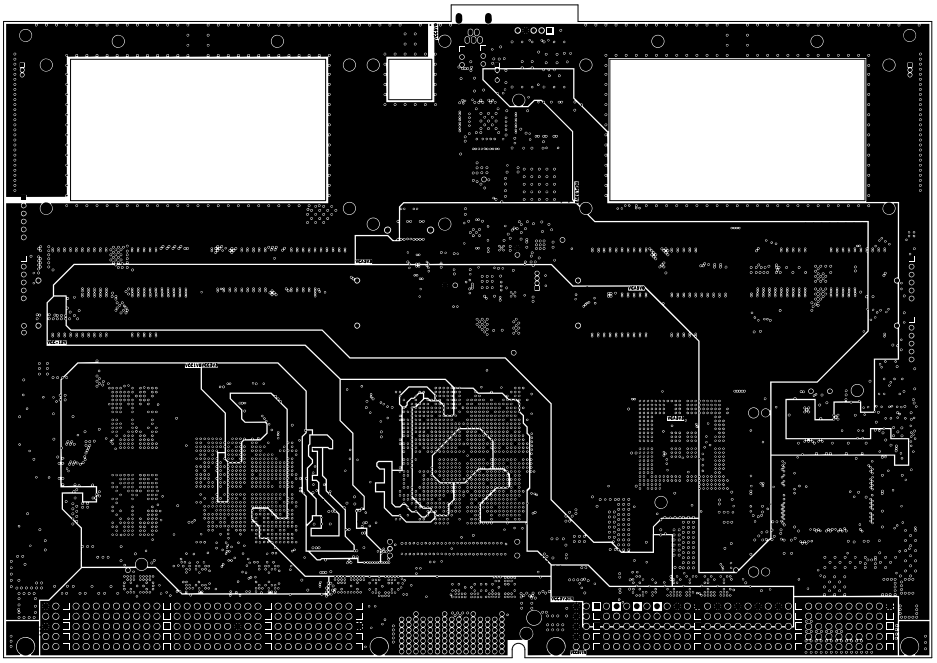

Figure A.5: Layer VCC1 of the GANDALF PCB.

Figure A.6: Layer GND2 of the GANDALF PCB.

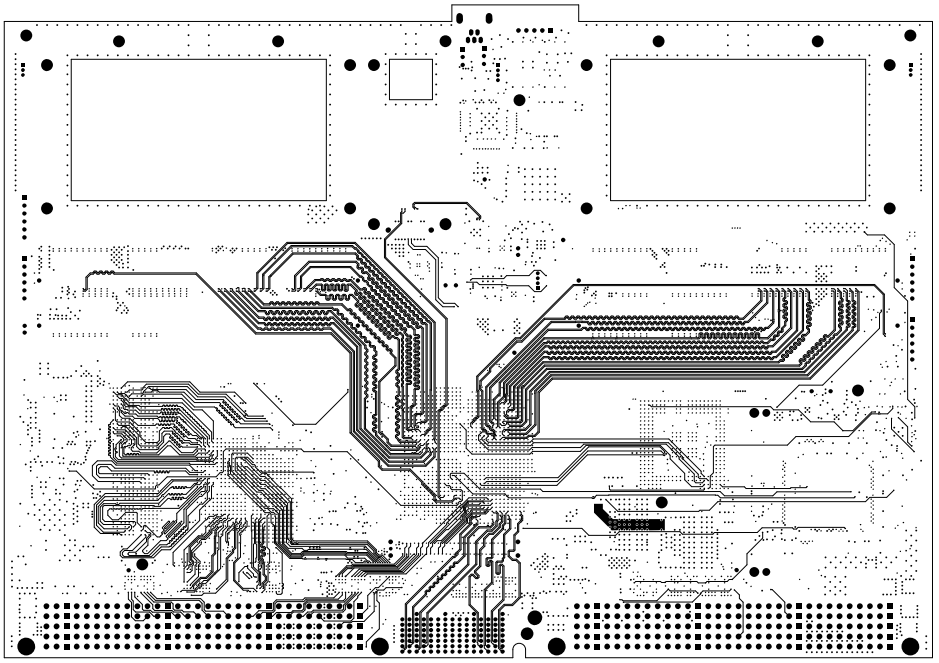

Figure A.7: Layer SIG4 of the GANDALF PCB.

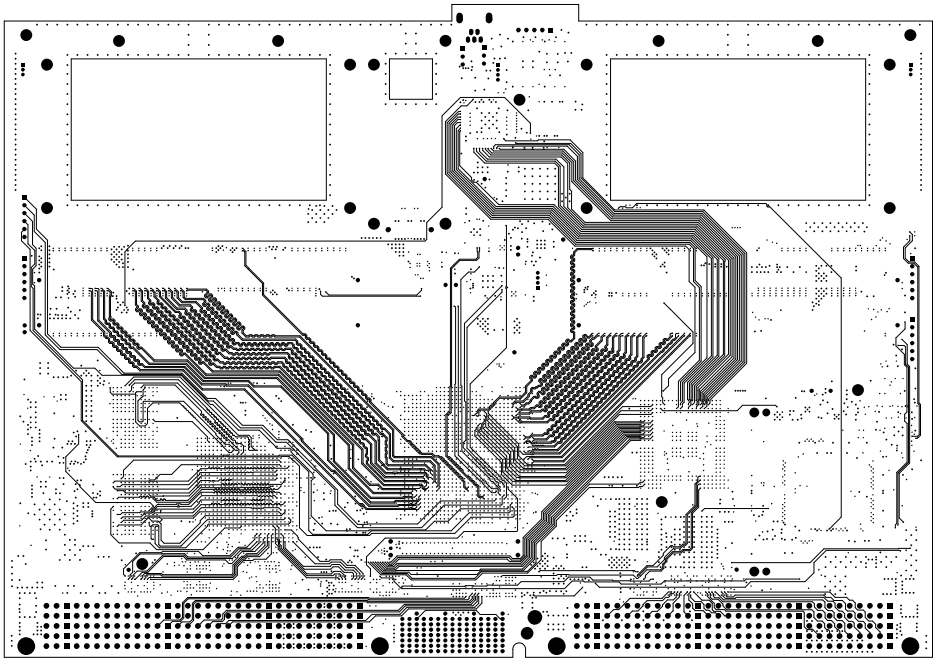

Figure A.8: Layer SIG5 of the GANDALF PCB.

Figure A.9: Layer GND3 of the GANDALF PCB.

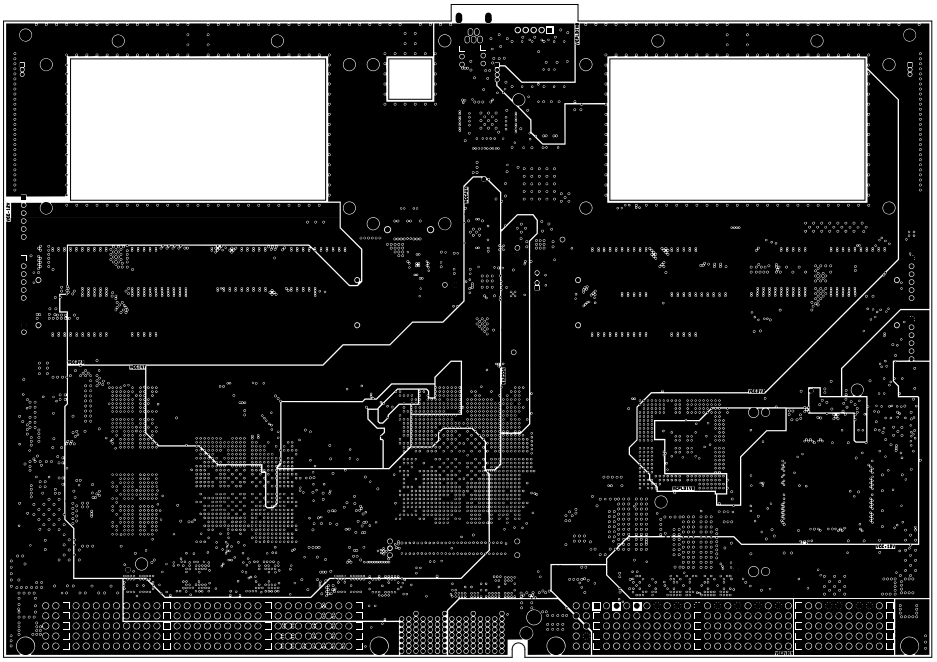

Figure A.10: Layer VCC2 of the GANDALF PCB.

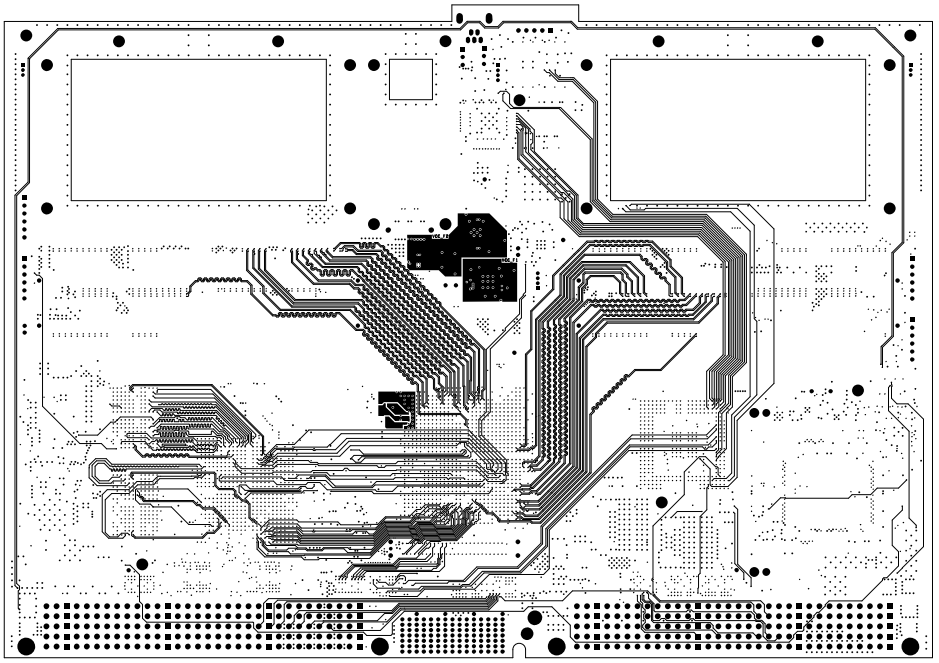

Figure A.11: Layer SIG6 of the GANDALF PCB.

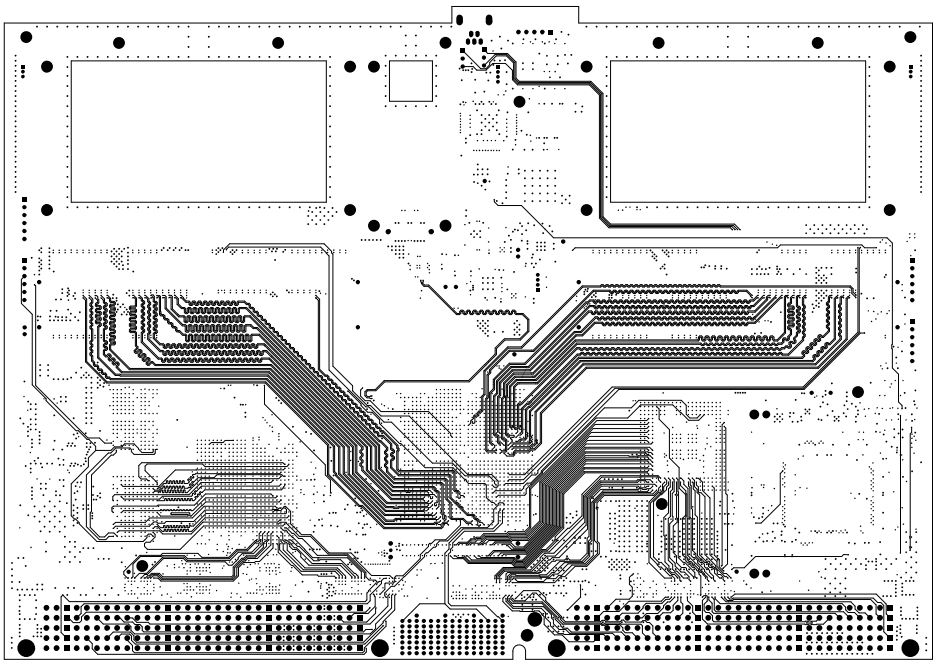

Figure A.12: Layer SIG7 of the GANDALF PCB.

Figure A.13: Layer GND4 of the GANDALF PCB.

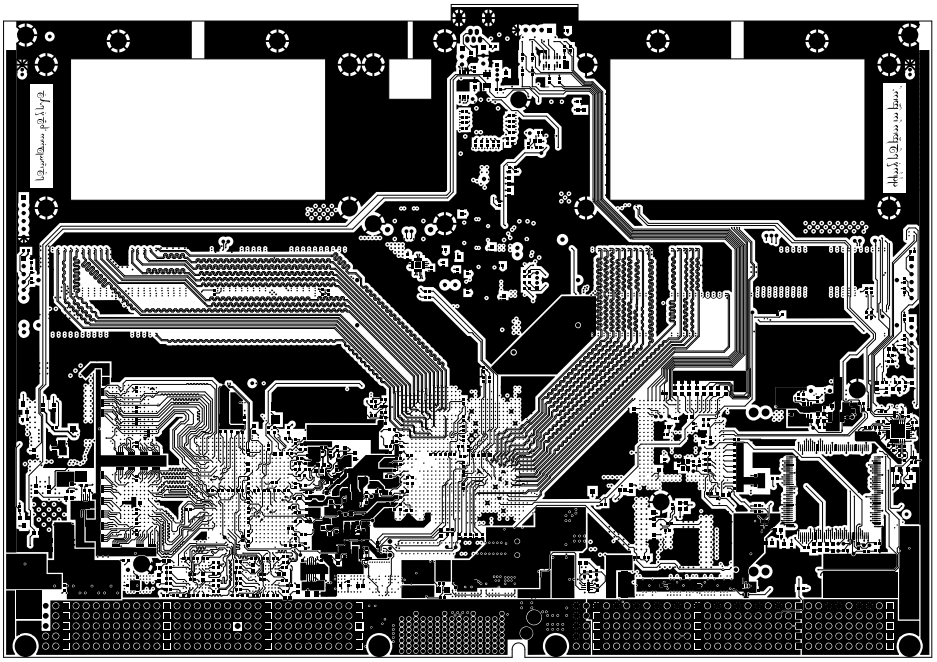

Figure A.14: Layer BOT of the GANDALF PCB.

A.4 GANDALF Module Device Overview

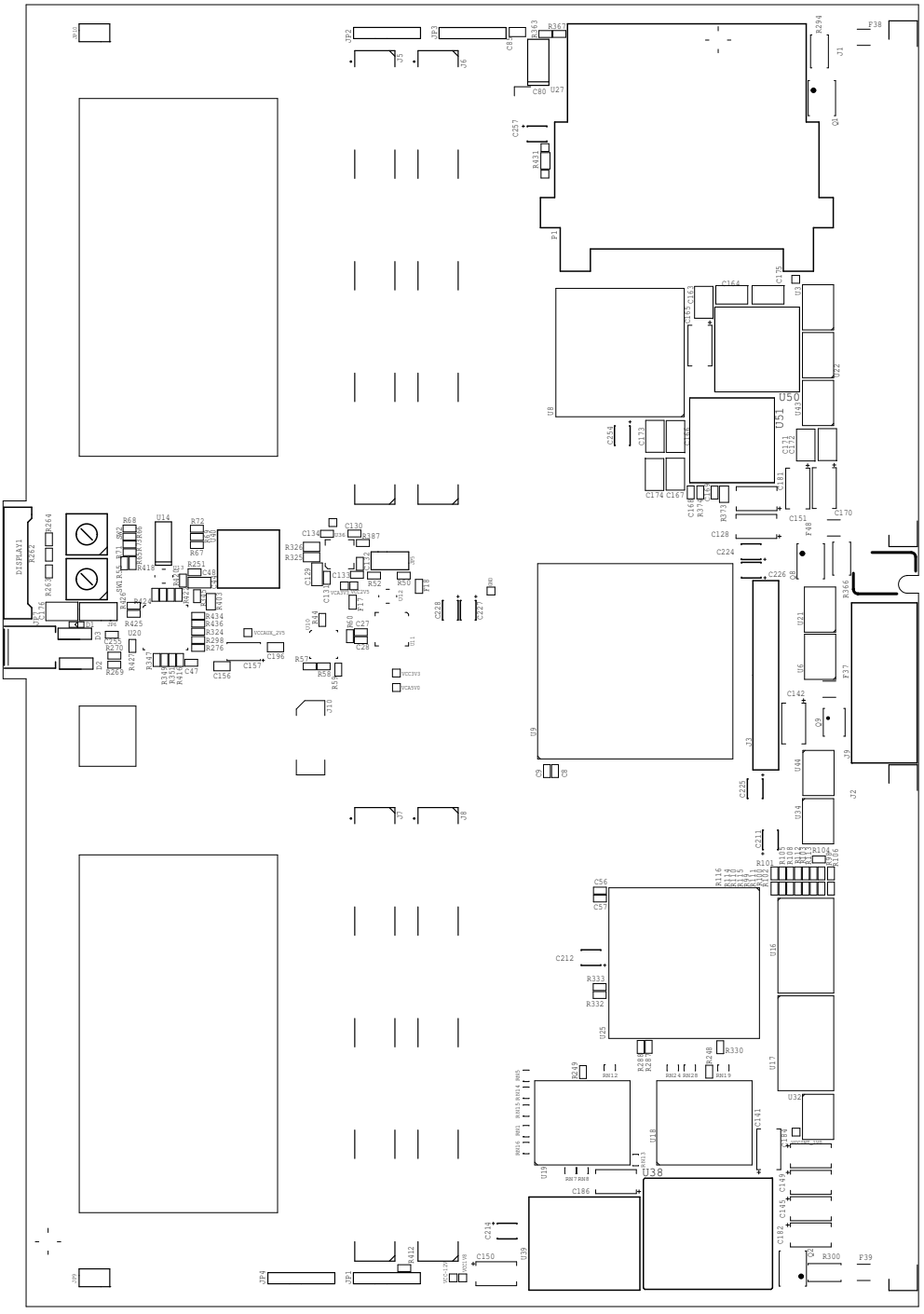

Figure A.15: Overview of the placed devices including Reference Designators on the top side of the PCB.

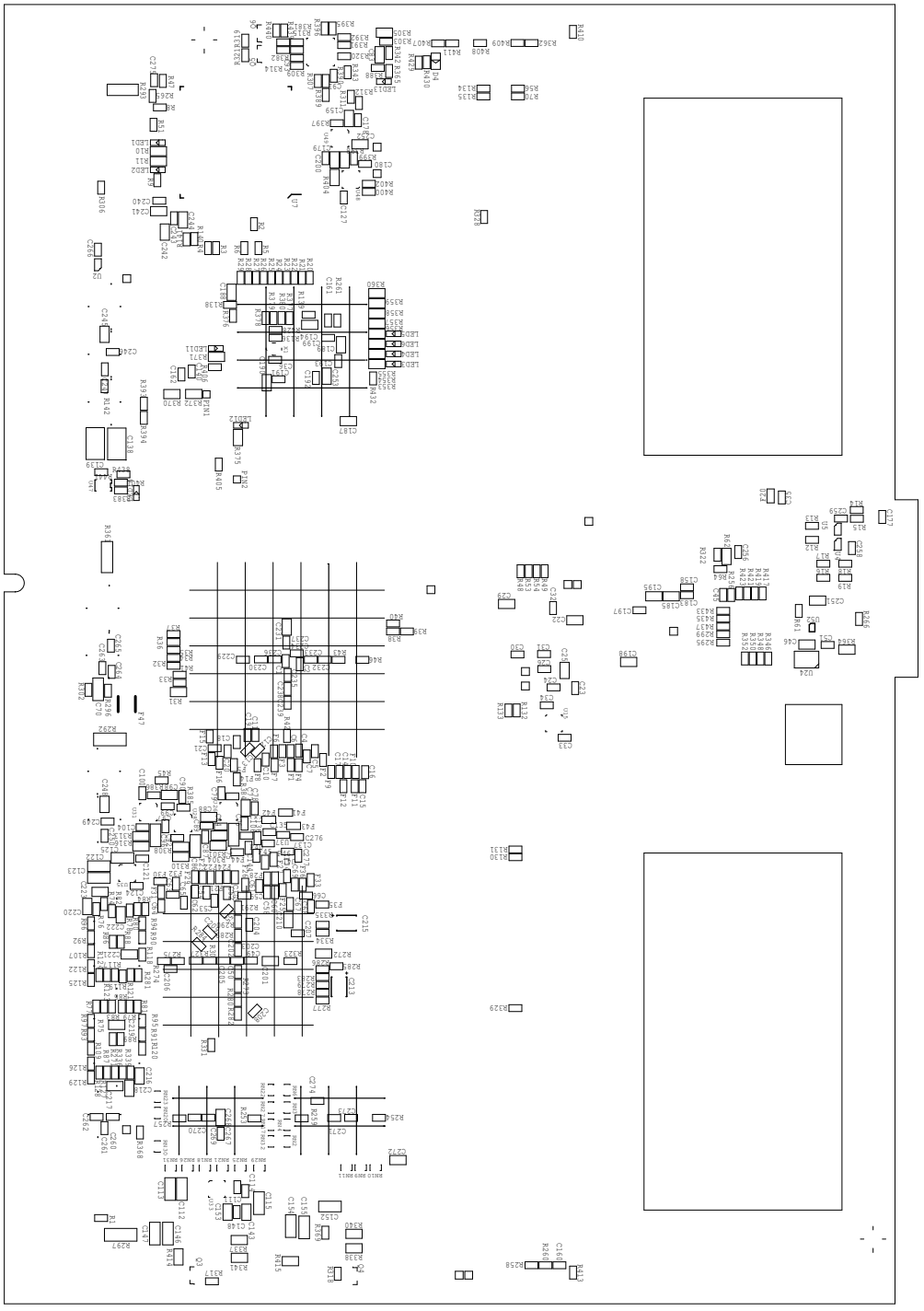

Figure A.16: Overview of the placed devices including Reference Designators on the bottom site of the PCB.

B. Appendix: Connectivity Tables

B.1 GANDALF Backplane Connectors

Table B.1: VME connector (*J1*) pinout.

	Z	A	B	C	D
1	-	D(0)	-	D(8)	+5V
2	GND	D(1)	-	D(9)	GND
3	-	D(2)	-	D(10)	+12V
4	GND	D(3)	-	D(11)	+12V
5	-	D(4)	-	D(12)	-
6	GND	D(5)	-	D(13)	+12V
7	-	D(6)	-	D(14)	+12V
8	GND	D(7)	-	D(15)	-
9	-	GND	-	GND	GAP
10	GND	-	BG3IN	-	GA0
11	-	GND	BG3OUT	BERR	GA1
12	GND	DS1	-	SYSRES	+3.3V
13	-	DS0	-	LWORD	GA2
14	GND	WRITE	-	AM5	+3.3V
15	-	GND	-	A(23)	GA3
16	GND	DTACK	AM0	A(22)	+3.3V
17	-	GND	AM1	A(21)	GA4
18	GND	AS	AM2	A(20)	+3.3V
19	-	GND	AM3	A(19)	-
20	GND	IACK	GND	A(18)	+3.3V
21	-	IACKIN	-	A(17)	-
22	GND	IACKOUT	-	A(16)	+3.3V
23	-	AM4	GND	A(15)	-
24	GND	A(7)	-	A(14)	+3.3V
25	-	A(6)	-	A(13)	-
26	GND	A(5)	-	A(12)	+3.3V
27	-	A(4)	-	A(11)	LI/I
28	GND	A(3)	-	A(10)	+3.3V
29	-	A(2)	-	A(9)	LI/O
30	GND	A(1)	-	A(8)	+3.3V
31	-	-12V	-	+12V	GND
32	GND	+5V	+5V	+5V	+5V

Table B.2: VME connector (*J2*) pinout. The UD bus in row A and C are used for the S-LINK interface.

	Z	A	B	C	D
1	-	SINIT	+5V	SDONE	-
2	GND	SCLK	GND	SDIN	-
3	-	GND	-	SPROG	-
4	GND	UD(0)	A(24)	GND	-
5	-	UD(2)	A(25)	UD(1)	-
6	GND	UD(4)	A(26)	UD(3)	-
7	-	UD(6)	A(27)	UD(5)	-
8	GND	GND	A(28)	UD(7)	-
9	-	UD(8)	A(29)	GND	-
10	GND	UD(10)	A(30)	UD(9)	-
11	-	UD(12)	A(31)	UD(11)	-
12	GND	UD(14)	GND	UD(13)	-
13	-	GND	+5V	UD(15)	-
14	GND	UD(16)	D(16)	UD(17)	-
15	-	UD(18)	D(17)	GND	-
16	GND	UD(20)	D(18)	UD(19)	-
17	-	UD(22)	D(19)	UD(21)	-
18	GND	GND	D(20)	UD(23)	-
19	-	UD(24)	D(21)	UD(25)	-
20	GND	UD(26)	D(22)	GND	-
21	-	UD(28)	D(23)	UD(27)	-
22	GND	UD(30)	GND	UD(29)	-
23	-	GND	D(24)	UD(31)	-
24	GND	UCTRL	D(25)	UDW0	-
25	-	UDW1	D(26)	UDTEST	-
26	GND	UDRESET	D(27)	GND	-
27	-	GND	D(28)	UDWEN	-
28	GND	UDCLK	D(29)	GND	-
29	-	GND	D(30)	LFF	-
30	GND	LDOWN	D(31)	SRESET	-
31	-	-	GND	-	GND
32	GND	-	+5V	-	+5V

Table B.3: VXS connector (*J9*) pinout.

	A	B	C	D	E	F	G
1	TRG_2P	TRG_2N	GND	TRG_0P	TRG_0N	GND	VXS_SCL
2	GND	TRG_6P	TRG_6N	GND	TRG_1P	TRG_1N	GND
3	TRG_3P	TRG_3N	GND	TRG_4P	TRG_4N	GND	VXS_SDA
4	GND	TRG_12P	TRG_12N	GND	TRG_5P	TRG_5N	GND
5	-	-	GND	-	-	GND	-
6	GND	-	-	GND	-	-	GND
7	-	-	GND	-	-	GND	-
8	GND	-	-	GND	-	-	GND
9	-	-	GND	-	-	GND	-
10	GND	-	-	GND	-	-	GND
11	-	-	GND	-	-	GND	-
12	GND	TRG_14P	TRG_14N	GND	TRG_10P	TRG_10N	GND
13	TRG_8P	TRG_8N	GND	TRG_7P	TRG_7N	GND	-
14	GND	TRG_13P	TRG_13N	GND	TRG_15P	TRG_15N	GND
15	TRG_11P	TRG_11N	GND	TRG_9P	TRG_9N	GND	-

B.2 Mezzanine Card Socket Up/Down Connectors

Table B.4: Mezzanine Card Socket Up connector pinout (*J5*).

1	PORT1_0N	VCC-12V	2
3	PORT1_0P	VCC-12V	4
5	PORT1_1N	VCA3V3	6
7	PORT1_1P	VCA3V3	8
9	PORT1_2N	VCA3V3	10
11	PORT1_2P	VCA3V3	12
13	PORT1_3N	VCA3V3	14
15	PORT1_3P	VCA3V3	16
17	PORT1_4N	VCA3V3	18
19	PORT1_4P	VCA3V3	20
21	PORT1_5N	PORT3_0N	22
23	PORT1_5P	PORT3_0P	24
25	PORT1_6N	PORT3_1N	26
27	PORT1_6P	PORT3_1P	28
29	PORT1_7N	PORT3_2N	30
31	PORT1_7P	PORT3_2P	32
33	PORT1_8N	PORT3_3N	34
35	PORT1_8P	PORT3_3P	36
37	PORT1_9N	PORT3_4N	38
39	PORT1_9P	PORT3_4P	40
41	PORT1_10N	PORT3_5N	42
43	PORT1_10P	PORT3_5P	44
45	PORT1_11N	PORT3_6N	46
47	PORT1_11P	PORT3_6P	48
49	PORT1_12N	PORT3_7N	50
51	PORT1_12P	PORT3_7P	52
53	PORT1_13N	PORT3_8N	54
55	PORT1_13P	PORT3_8P	56
57	PORT1_DRYN	PORT3_9N	58
59	PORT1_DRYP	PORT3_9P	60
61	GND	PORT3_10N	62
63	ADC_NC	PORT3_10P	64
65	ADCOFF	PORT3_11N	66
67	GND	PORT3_11P	68
69	SI_RST#	PORT3_12N	70
71	SI_LOL	PORT3_12P	72
73	GND	PORT3_13N	74
75	GND	PORT3_13P	76
77	CLK_155MHZ_P	PORT3_DRYN	78
79	CLK_155MHZ_N	PORT3_DRYP	80
81	GND	PORT5_0N	82

83	GND	PORT5_0P	84
85	GND	PORT5_1N	86
87	GND	PORT5_1P	88
89	GND	PORT5_2N	90
91	GND	PORT5_2P	92
93	GND	PORT5_3N	94
95	GND	PORT5_3P	96
97	GND	PORT5_4N	98
99	GND	PORT5_4P	100
101	PORT7_0N	PORT5_5N	102
103	PORT7_0P	PORT5_5P	104
105	PORT7_1N	PORT5_6N	106
107	PORT7_1P	PORT5_6P	108
109	PORT7_2N	PORT5_7N	110
111	PORT7_2P	PORT5_7P	112
113	PORT7_3N	PORT5_8N	114
115	PORT7_3P	PORT5_8P	116
117	PORT7_4N	PORT5_9N	118
119	PORT7_4P	PORT5_9P	120
121	PORT7_5N	PORT5_10N	122
123	PORT7_5P	PORT5_10P	124
125	PORT7_6N	PORT5_11N	126
127	PORT7_6P	PORT5_11P	128
129	PORT7_7N	PORT5_12N	130
131	PORT7_7P	PORT5_12P	132
133	PORT7_8N	PORT5_13N	134
135	PORT7_8P	PORT5_13P	136
137	PORT7_9N	PORT5_DRYN	138
139	PORT7_9P	PORT5_DRYP	140
141	PORT7_10N	VCA5V0	142
143	PORT7_10P	VCA5V0	144
145	PORT7_11N	VCA5V0	146
147	PORT7_11P	VCA5V0	148
149	PORT7_12N	VCA5V0	150
151	PORT7_12P	VCA5V0	152
153	PORT7_13N	VCA5V0	154
155	PORT7_13P	VCA5V0	156
157	PORT7_DRYN	VCA5V0	158
159	PORT7_DRYP	VCA5V0	160

Table B.5: Mezzanine Card Socket Up connector pinout (*J6*).

1	AMCTMS	PORT0_DRYP	2
3	AMCTCK	PORT0_DRYN	4
5	AMCTDI	PORT0_13P	6
7	AMCTDO	PORT0_13N	8
9	GND	PORT0_12P	10
11	GP_SDA	PORT0_12N	12
13	GP_SCL	PORT0_11P	14
15	GND	PORT0_11N	16
17	GND	PORT0_10P	18
19	GND	PORT0_10N	20
21	PORT2_DRYP	PORT0_9P	22
23	PORT2_DRYN	PORT0_9N	24
25	PORT2_13P	PORT0_8P	26
27	PORT2_13N	PORT0_8N	28
29	PORT2_12P	PORT0_7P	30
31	PORT2_12N	PORT0_7N	32
33	PORT2_11P	PORT0_6P	34
35	PORT2_11N	PORT0_6N	36
37	PORT2_10P	PORT0_5P	38
39	PORT2_10N	PORT0_5N	40
41	PORT2_9P	PORT0_4P	42
43	PORT2_9N	PORT0_4N	44
45	PORT2_8P	PORT0_3P	46
47	PORT2_8N	PORT0_3N	48
49	PORT2_7P	PORT0_2P	50
51	PORT2_7N	PORT0_2N	52
53	PORT2_6P	PORT0_1P	54
55	PORT2_6N	PORT0_1N	56
57	PORT2_5P	PORT0_0P	58
59	PORT2_5N	PORT0_0N	60
61	PORT2_4P	GND	62
63	PORT2_4N	GND	64
65	PORT2_3P	GND	66
67	PORT2_3N	SI_SDA	68
69	PORT2_2P	SI_SCL	70
71	PORT2_2N	GND	72
73	PORT2_1P	SI_LOS	74
75	PORT2_1N	MEZZ_ADDR	76
77	PORT2_0P	GND	78
79	PORT2_0N	CLK_38MHZ	80
81	PORT4_DRYP	GND	82
83	PORT4_DRYN	GND	84
85	PORT4_13P	GND	86

87	PORT4_13N	GND	88
89	PORT4_12P	GND	90
91	PORT4_12N	GND	92
93	PORT4_11P	GND	94
95	PORT4_11N	GND	96
97	PORT4_10P	GND	98
99	PORT4_10N	GND	100
101	PORT4_9P	PORT6_DRYP	102
103	PORT4_9N	PORT6_DRYN	104
105	PORT4_8P	PORT6_13P	106
107	PORT4_8N	PORT6_13N	108
109	PORT4_7P	PORT6_12P	110
111	PORT4_7N	PORT6_12N	112
113	PORT4_6P	PORT6_11P	114
115	PORT4_6N	PORT6_11N	116
117	PORT4_5P	PORT6_10P	118
119	PORT4_5N	PORT6_10N	120
121	PORT4_4P	PORT6_9P	122
123	PORT4_4N	PORT6_9N	124
125	PORT4_3P	PORT6_8P	126
127	PORT4_3N	PORT6_8N	128
129	PORT4_2P	PORT6_7P	130
131	PORT4_2N	PORT6_7N	132
133	PORT4_1P	PORT6_6P	134
135	PORT4_1N	PORT6_6N	136
137	PORT4_0P	PORT6_5P	138
139	PORT4_0N	PORT6_5N	140
141	VCC3V3	PORT6_4P	142
143	VCC3V3	PORT6_4N	144
145	VCC3V3	PORT6_3P	146
147	VCC3V3	PORT6_3N	148
149	VCC3V3	PORT6_2P	150
151	VCC3V3	PORT6_2N	152
153	VCC+12V	PORT6_1P	154
155	VCC+12V	PORT6_1N	156
157	VCC+12V	PORT6_0P	158
159	VCC+12V	PORT6_0N	160

Table B.6: Mezzanine Card Socket Down connector pinout (*J7*).

1	PORT9_0N	VCC-12V	2
3	PORT9_0P	VCC-12V	4
5	PORT9_1N	VCA3V3	6
7	PORT9_1P	VCA3V3	8
9	PORT9_2N	VCA3V3	10
11	PORT9_2P	VCA3V3	12
13	PORT9_3N	VCA3V3	14
15	PORT9_3P	VCA3V3	16
17	PORT9_4N	VCA3V3	18
19	PORT9_4P	VCA3V3	20
21	PORT9_5N	PORT11_0N	22
23	PORT9_5P	PORT11_0P	24
25	PORT9_6N	PORT11_1N	26
27	PORT9_6P	PORT11_1P	28
29	PORT9_7N	PORT11_2N	30
31	PORT9_7P	PORT11_2P	32
33	PORT9_8N	PORT11_3N	34
35	PORT9_8P	PORT11_3P	36
37	PORT9_9N	PORT11_4N	38
39	PORT9_9P	PORT11_4P	40
41	PORT9_10N	PORT11_5N	42
43	PORT9_10P	PORT11_5P	44
45	PORT9_11N	PORT11_6N	46
47	PORT9_11P	PORT11_6P	48
49	PORT9_12N	PORT11_7N	50
51	PORT9_12P	PORT11_7P	52
53	PORT9_13N	PORT11_8N	54
55	PORT9_13P	PORT11_8P	56
57	PORT9_DRYN	PORT11_9N	58
59	PORT9_DRYP	PORT11_9P	60
61	GND	PORT11_10N	62
63	ADC_NC	PORT11_10P	64
65	ADCOFF	PORT11_11N	66
67	GND	PORT11_11P	68
69	SI_RST#	PORT11_12N	70
71	SI_LOL	PORT11_12P	72
73	GND	PORT11_13N	74
75	GND	PORT11_13P	76
77	CLK_155MHZ_P	PORT11_DRYN	78
79	CLK_155MHZ_N	PORT11_DRYP	80
81	GND	PORT13_0N	82
83	GND	PORT13_0P	84
85	GND	PORT13_1N	86

87	GND	PORT13_1P	88
89	GND	PORT13_2N	90
91	GND	PORT13_2P	92
93	GND	PORT13_3N	94
95	GND	PORT13_3P	96
97	GND	PORT13_4N	98
99	GND	PORT13_4P	100
101	PORT15_0N	PORT13_5N	102
103	PORT15_0P	PORT13_5P	104
105	PORT15_1N	PORT13_6N	106
107	PORT15_1P	PORT13_6P	108
109	PORT15_2N	PORT13_7N	110
111	PORT15_2P	PORT13_7P	112
113	PORT15_3N	PORT13_8N	114
115	PORT15_3P	PORT13_8P	116
117	PORT15_4N	PORT13_9N	118
119	PORT15_4P	PORT13_9P	120
121	PORT15_5N	PORT13_10N	122
123	PORT15_5P	PORT13_10P	124
125	PORT15_6N	PORT13_11N	126
127	PORT15_6P	PORT13_11P	128
129	PORT15_7N	PORT13_12N	130
131	PORT15_7P	PORT13_12P	132
133	PORT15_8N	PORT13_13N	134
135	PORT15_8P	PORT13_13P	136
137	PORT15_9N	PORT13_DRYN	138
139	PORT15_9P	PORT13_DRYP	140
141	PORT15_10N	VCA5V0	142
143	PORT15_10P	VCA5V0	144
145	PORT15_11N	VCA5V0	146
147	PORT15_11P	VCA5V0	148
149	PORT15_12N	VCA5V0	150
151	PORT15_12P	VCA5V0	152
153	PORT15_13N	VCA5V0	154
155	PORT15_13P	VCA5V0	156
157	PORT15_DRYN	VCA5V0	158
159	PORT15_DRYP	VCA5V0	160

Table B.7: Mezzanine Card Socket Down connector pinout (*J8*).

1	AMCTMS	PORT8_DRYP	2
3	AMCTCK	PORT8_DRYN	4
5	AMCTDI	PORT8_13P	6
7	AMCTDO	PORT8_13N	8
9	GND	PORT8_12P	10
11	GP_SDA	PORT8_12N	12
13	GP_SCL	PORT8_11P	14
15	GND	PORT8_11N	16
17	GND	PORT8_10P	18
19	GND	PORT8_10N	20
21	PORT10_DRYP	PORT8_9P	22
23	PORT10_DRYN	PORT8_9N	24
25	PORT10_13P	PORT8_8P	26
27	PORT10_13N	PORT8_8N	28
29	PORT10_12P	PORT8_7P	30
31	PORT10_12N	PORT8_7N	32
33	PORT10_11P	PORT8_6P	34
35	PORT10_11N	PORT8_6N	36
37	PORT10_10P	PORT8_5P	38
39	PORT10_10N	PORT8_5N	40
41	PORT10_9P	PORT8_4P	42
43	PORT10_9N	PORT8_4N	44
45	PORT10_8P	PORT8_3P	46
47	PORT10_8N	PORT8_3N	48
49	PORT10_7P	PORT8_2P	50
51	PORT10_7N	PORT8_2N	52
53	PORT10_6P	PORT8_1P	54
55	PORT10_6N	PORT8_1N	56
57	PORT10_5P	PORT8_0P	58
59	PORT10_5N	PORT8_0N	60
61	PORT10_4P	GND	62
63	PORT10_4N	GND	64
65	PORT10_3P	GND	66
67	PORT10_3N	SI_SDA	68
69	PORT10_2P	SI_SCL	70
71	PORT10_2N	GND	72
73	PORT10_1P	SI_LOS	74
75	PORT10_1N	MEZZ_ADDR	76
77	PORT10_0P	GND	78
79	PORT10_0N	CLK_38MHZ	80
81	PORT12_DRYP	GND	82
83	PORT12_DRYN	GND	84
85	PORT12_13P	GND	86

87	PORT12_13N	GND	88
89	PORT12_12P	GND	90
91	PORT12_12N	GND	92
93	PORT12_11P	GND	94
95	PORT12_11N	GND	96
97	PORT12_10P	GND	98
99	PORT12_10N	GND	100
101	PORT12_9P	PORT14_DRYP	102
103	PORT12_9N	PORT14_DRYN	104
105	PORT12_8P	PORT14_13P	106
107	PORT12_8N	PORT14_13N	108
109	PORT12_7P	PORT14_12P	110
111	PORT12_7N	PORT14_12N	112
113	PORT12_6P	PORT14_11P	114
115	PORT12_6N	PORT14_11N	116
117	PORT12_5P	PORT14_10P	118
119	PORT12_5N	PORT14_10N	120
121	PORT12_4P	PORT14_9P	122
123	PORT12_4N	PORT14_9N	124
125	PORT12_3P	PORT14_8P	126
127	PORT12_3N	PORT14_8N	128
129	PORT12_2P	PORT14_7P	130
131	PORT12_2N	PORT14_7N	132
133	PORT12_1P	PORT14_6P	134
135	PORT12_1N	PORT14_6N	136
137	PORT12_0P	PORT14_5P	138
139	PORT12_0N	PORT14_5N	140
141	VCC3V3	PORT14_4P	142
143	VCC3V3	PORT14_4N	144
145	VCC3V3	PORT14_3P	146
147	VCC3V3	PORT14_3N	148
149	VCC3V3	PORT14_2P	150
151	VCC3V3	PORT14_2N	152
153	VCC+12V	PORT14_1P	154
155	VCC+12V	PORT14_1N	156
157	VCC+12V	PORT14_0P	158
159	VCC+12V	PORT14_0N	160

B.3 Mezzanine Card Socket Central Connector

Table B.8: Mezzanine Card Socket Central connector pinout (*J10*).

1	+3.3V	+3.3V	2
3	GND	GND	4
5	CLK_N	GND	6
7	CLK_P	GND	8
9	GND	LOCK	10
11	GND	RATE	12
13	DATA_N	GND	14
15	DATA_P	GND	16
17	GND	GND	18
19	+5V	+5V	20

C. Appendix: VXS Crate Power Supply Specification

Table C.1: Selection of power supply modules for the VXS crate. The total maximum power of a VXS crate with this power supply configuration 2760W. The crate including the power supply was manufactured by Wiener Inc. [92].

Voltage	# modules	Current
+12.0V	3	138A
+ 5.0V	1	115A
+ 3.3V	1	115A
-12.0V	1	46A

D. Appendix: ADC, DAC and Input Voltage Correlation

In Figs. D.1 to D.3 measurement results which express the correlation between input circuit baseline, the DAC values and the corresponding ADC values are given. In Fig. D.1 the voltage applied to the analog circuit was screened from $-2.0\,\mathrm{V}$ to $+2.0\,\mathrm{V}$ (x axis) for two channels. The resulting ADC values are plotted on the y axis. This is done for a constant DAC value of $0x0000$. In Fig. D.2 the same measurement was performed with a screening from $-4.0\,\mathrm{V}$ to $0.0\,\mathrm{V}$ and a DAC value of $0x6400$. In Fig. D.3 a screening of DAC values is performed (x axis) and the resulting ADC values are plotted on the y axis for a constant voltage of $0.0\,\mathrm{V}$ at the analog inputs.

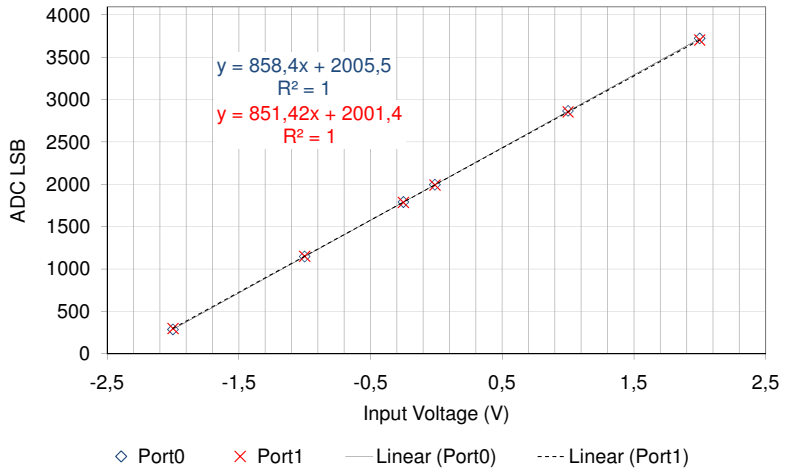

Figure D.1: Voltage to ADC LSB screening with constant DAC value $0x0000$. This is the DAC setting to image bipolar input signals from $-2.0\,\mathrm{V}$ to $+2\,\mathrm{V}$ to the full dynamic range of the ADC. For comparison the measurements of two channels are plotted.

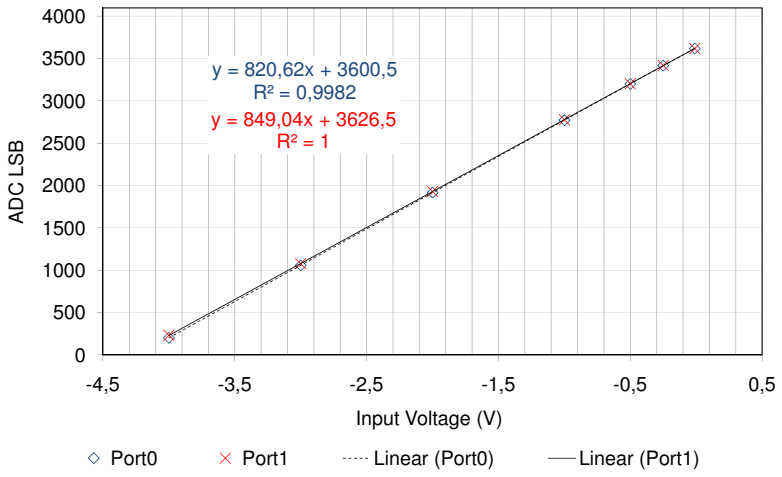

Figure D.2: Voltage to ADC LSB screening with constant DAC value $0x6400$. This is a DAC setting to image unipolar input signals from $-4.0\,\mathrm{V}$ to $0.0\,\mathrm{V}$ to the full dynamic range of the ADC. For comparison the measurements of two channels are plotted.

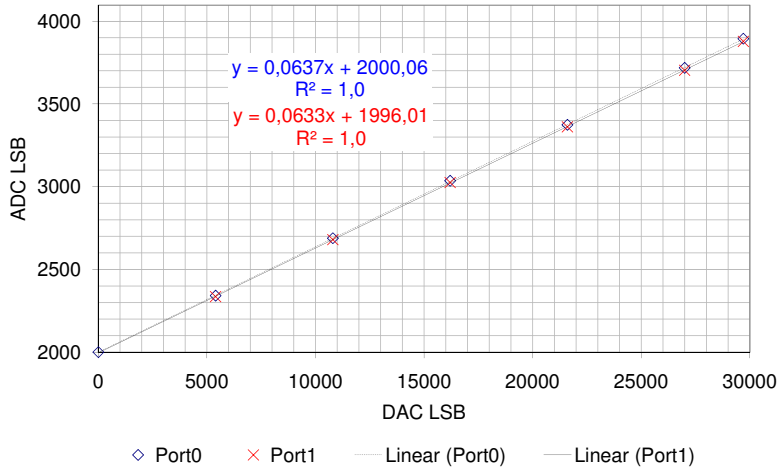

Figure D.3: DAC LSB to ADC LSB screening with a constant input voltage of $0.0\,\mathrm{V}$. This images the DAC range to the full dynamic range of the ADC. For comparison the measurements of two channels are plotted.

E. Appendix: GANDALF Firmware Registers

E.1 VME Interface Registers

Table E.1: VME address for communication with the GANDALF CPLD. The [HEXID(8)] to address the GANDALF modules located in a VME crate can be selected by DIP switches (*SW1*, *SW2*) (see Fig. 4.3). Please refer to http://hadron.physik.uni-freiburg.de/gandalf for updates.

VME address	**Name**	**Description**
0xE0[HEXID(8)]00FC	BOARDSTATUS	Returns 0x[CONF(4)][HEXID(8)]'00'[GeoAdd(6)]'00'[SN(10)] of module with [HEXID(8)].
0xE0[HEXID(8)]3000	R_VISION_FIFO	Reads the valid data word from the output of the *Spy FIFO*.
0xE0[HEXID(8)]0010	ARMBROADCAST	Resets module with [HEXID(8)] to accept broadcasting data.
0xE0[HEXID(8)]8000	BC_FPGA_CFG	VME address to write the broadcast configuration data for the DSP (*U9*) or the MEM-FPGA (*U25*) to the VME backplane (the DSP-FPGA has to be configured first). The rightmost GANDALF module located in the VME crate must be addressed.
0xE0[HEXID(8)]0014	BC_SWITCH	VME address to switch from DSP-FPGA (*U9*) configuration to MEM-FPGA (*U25*) configuration. The rightmost GANDALF module located in the VME crate must be addressed.

E.2 Fast Registers

Table E.2: Table of Fast Register Commands. To set a Fast Register use the command
$\# > ./vme\_write\ E0[HEXID(8)][CMD\_SEL(4)][FR\_ADDR(12)]\ \ [PULSE\_TYPE(4)]$,
where $[CMD\_SEL(4)]$ is 0x7, $[FR\_ADDR(12)]$ is the addressed Fast Register and $[PULSE\_TYPE(4)]$ defines the pulse type. In the VHDL firmware the Fast Registers are represented in a 256 bit bus. $VHDL\_SIG$ gives the corresponding number of the bus member (see section 4.2.2). Please refer to http://hadron.physik.uni-freiburg.de/gandalf for updates.

FR Name	**FR_ADDR**	**VHDL_SIG**	**PULSE_TYPE**	**Description**
DAC_CALIB	0x00C	3	const (TYPE = 0x0/1)	Disables/Enables DAC calibration.
TRG_TEMP_RDOUT	0x010	4	pulse (TYPE = 0x2)	Triggers readout of all temperature values (AMC, FPGA temp sensors).
TRG_VOLT_RDOUT	0x014	5	pulse (TYPE = 0x2)	Triggers readout of all voltage values (FPGA voltage sensors).
RD_EEPROM_UP	0x018	6	pulse (TYPE = 0x2)	Triggers readout of EEPROM data to configuration memory of mezzanine in card slot up.
WR_EEPROM_UP	0x01C	7	pulse (TYPE = 0x2)	Triggers storage of configuration memory data to EEPROM of mezzanine in card slot up.
RD_EEPROM_DN	0x020	8	pulse (TYPE = 0x2)	Triggers readout of EEPROM data to configuration memory of mezzanine in card slot down.
WR_EEPROM_DN	0x024	9	pulse (TYPE = 0x2)	Triggers storage of configuration memory data to EEPROM of mezzanine in card slot dn.

Table E.2: Table of Fast Register Commands (continued).

FR Name	FR_ADDR	VHDL_SIG	PULSE_TYPE	Description
LOAD_SI	0x028	10	pulse (TYPE = 0x2)	Triggers configuration of the *SI*5326 clock synthesizer located on the GANDALF module and all SI5326 on the mounted AMCs. The configuration data is stored in the configuration memory registers *SI_CONF_DATA*0 - *SI_CONF_DATA*11 (see Tab. E.3, [77]).
LOAD_DACs	0x02C	11	pulse (TYPE = 0x2)	Triggers configuration of the *AD*5665*R* DACs located on the AMCs. The DAC values are stored in the configuration memory registers *DAC_VAL*0 - *DAC_VAL*3 (see Tab. E.3, [66]).
TRG_DAC_CALIB	0x030	12	pulse (TYPE = 0x2)	Triggers the automatic DAC calibration. New DAC values are written to the *DAC_VAL*0 - *DAC_VAL*3 registers.
LOAD_G_CONF_VAL	0x034	13	pulse (TYPE = 0x2)	Updates all configuration values written into the configuration memory to the active FPGA logic.
*VME_RESET*0	0x038	14	pulse (TYPE = 0x2)	Performs a reset on reset level 0 (see section 4.2.2).
*VME_RESET*1	0x03c	15	pulse (TYPE = 0x2)	Performs a reset on reset level 1 (see section 4.2.2).
*VME_RESET*2	0x040	16	pulse (TYPE = 0x2)	Performs a reset on reset level 2 (see section 4.2.2).

Table E.2: Table of Fast Register Commands (continued).

FR Name	FR_ADDR	VHDL_SIG	PULSE_TYPE	Description
EXT_BOS	0x044	17	pulse (TYPE = 0x2)	Used to generate an artificial BOS[1] signal. Can be used if no TCS[2] is adapted (see section 4.1.3, [54]).
EXT_EOS	0x048	18	pulse (TYPE = 0x2)	Used to generate an artificial EOS[3] signal. Can be used if no TCS is adapted.
ART_TRG	0x04c	19	pulse (TYPE = 0x2)	Used to generate an artificial trigger signal. Can be used if no TCS is adapted.
SLINK_RESET	0x050	20	pulse (TYPE = 0x2)	Triggers the S-LINK reset procedure as explained in the S-LINK specification [46].
SMUX_RESET	0x054	21	pulse (TYPE = 0x2)	Triggers a reset signal on the *SRESET* pin C30 (P2, [49], see Tab. B.2) to perform a common reset on up to four SMUX transition cards.
SELF_TRG	0x060 - 0x09C	24 - 39	const (TYPE = 0x1)	Specifies the analog channel which is allowed to generate a "self trigger", if the analog signal reaches a value above the constant defined in the configuration registers $THRES\_VAL0$ - $THRES\_VAL3$.

[1] Begin Of Spill
[2] Trigger Control System
[3] End Of Spill

E.3 Configuration Memory Registers

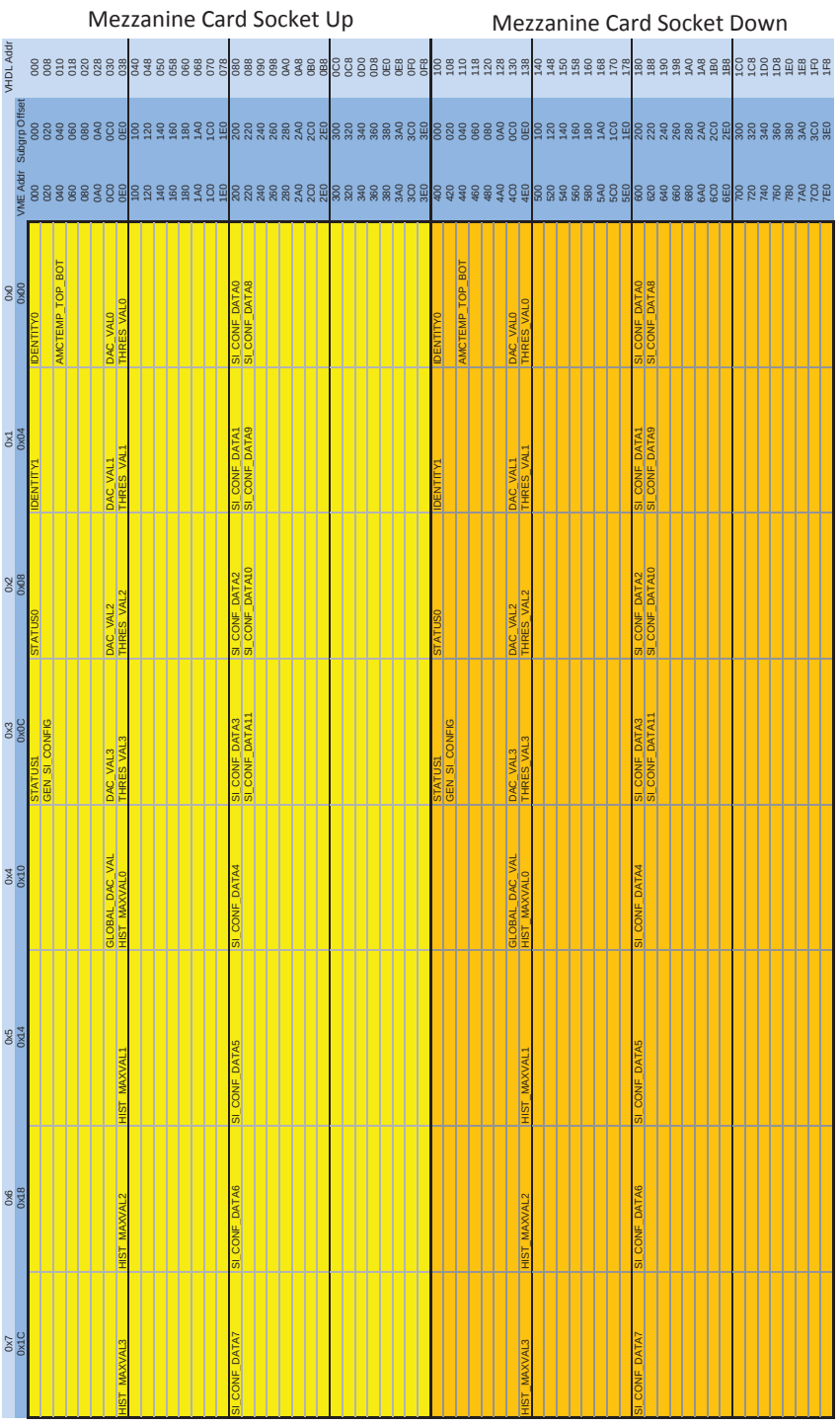

Figure E.1: Overview of the Configuration Memory Registers for the mounted Mezzanine Cards on Mezzanine Card Socket Up and Down. A detailed description of the registers can be found in Tab. E.3. Please refer to http://hadron.physik.uni-freiburg.de/gandalf for updates.

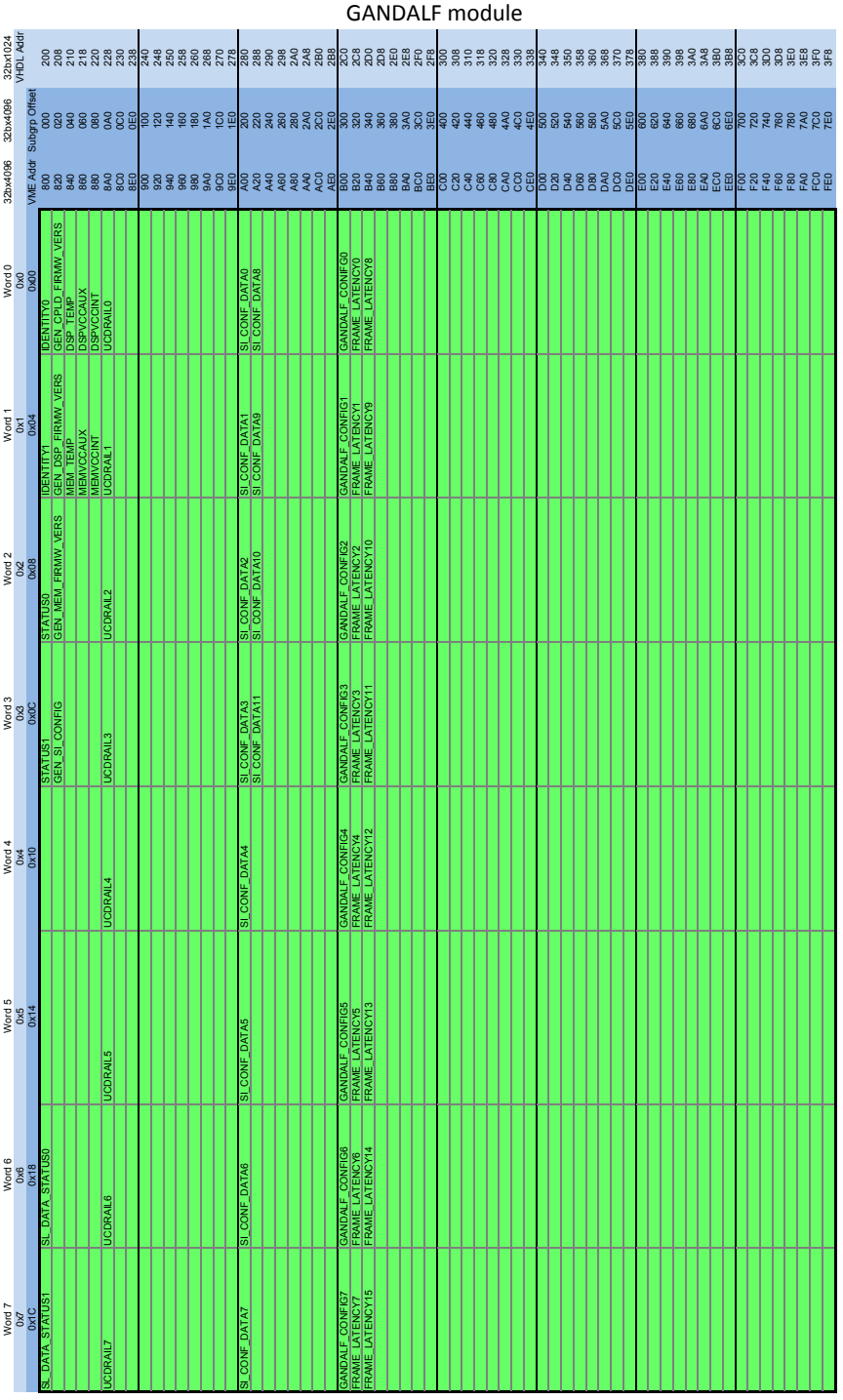

Figure E.2: Overview of the Configuration Memory Registers for the GANDALF module. A detailed description of the registers can be found in Tab. E.3. Please refer to http://hadron.physik.uni-freiburg.de/gandalf for updates.

Table E.3: Table of Configuration Memory Registers. *CM_REG* gives the name of the configuration memory register and *VME_CMR_ADDR* the corresponding VME address. The colours orange and yellow declare that the register is used for mezzanine cards installed in mezzanine card slot up and down. Green coloured VME addresses declare that the register is used for the GANDALF module. See also Figs. E.1, E.2. The corresponding VHDL address for the configuration memory can also be found in this Figures. *CMR_DETAIL* gives the names and in brackets the size of the detail of a register. Please refer to http://hadron.physik.uni-freiburg.de/gandalf for updates.

CM_REG	VME_CMR_ADDR	CMR_DETAIL	Description
*IDENTITY*0 (11 dnto 0)	0x000 0x400	*SERIAL_NO* (12)	Defines the Serial Number of the installed mezzanine card in mezzanine card slot up and down.
*IDENTITY*0 (15 dnto 12)	0x000 0x400	*CARD_TYPE* (4)	Defines the mezzanine card type: **0x0** AMC, **0x1** DMC, **0x2** OMC
*IDENTITY*0 (17 dnto 16)	0x000 0x400	*ADC_RES* (2)	Defines the resolution of the used ADCs, if AMC is installed: **0x0** 12bit, **0x1** 14 bit
*IDENTITY*0 (19 dnto 18)	0x000 0x400	*ADC_CONFIG* (2)	Defines the configuration of the input circuit of the used AMC: **0x0** normal, **0x1** interleaved
*IDENTITY*0 (21 dnto 20)	0x000 0x400	*DMC_CONFIG* (2)	Defines the differential buffer orientation used with the DMC: **0x0** input, **0x1** output
*IDENTITY*0 (6 dnto 0)	0x800	*STAT_MON* (10)	Defines the status of the System Monitoring (TBD).
*IDENTITY*0 (11 dnto 7)	0x800	*GEO_ADDR* (10)	Defines the geographic address (slot number in Crate) where the GANDALF module is installed to.
*IDENTITY*0 (21 dnto 12)	0x800	*GEO_ID* (10)	Defines the COMPASS experiment geographic ID.
*IDENTITY*0 (31 dnto 22)	0x800	*SERIAL_NO* (10)	Defines the Serial Number of the GANDALF module.

Table E.3: Table of Configuration Memory Registers (continued).

CM_REG	**VME_CMR_ADDR**	**CMR_DETAIL**	**Description**
*IDENTITY*1 (31 dnto 0)	0x004 0x404	*TBD* (32)	TBD
*IDENTITY*1 (9 dnto 0)	0x804	*SOURCE_ID* (32)	Defines the COMPASS experiment source ID.
*STATUS*0 (31 dnto 30)	0x008 0x408	*EEPROM_CONF* (2)	Defines if the EEPROM is configured: **0x0**,**0x3** not configured, **0x1** configured
*STATUS*0 (31 dnto 30)	0x008 0x408	*MEZZ_INST* (2)	Defines if a mezzanine card is installed (is defined physically when no EEPROM is attached to the I2C bus): **0x1** not installed, **0x0**,**0x3** installed
*STATUS*0 (27 dnto 20)	0x808	*DESIGN_TYPE* (8)	Defines which firmware is loaded into the GANDALF module: **0x00** GANDALF base design, **0x04** GANDALF transient analyzer, **0x08** GANDALF TDC, **0x09** GANDALF scaler, **0x10** GANDALF meantimer, **0x14** GANDALF Arwen readout, **0xF0** GANDALF pattern generator, **0xF1** GANDALF module test
*STATUS*1 (31 dnto 0)	0x00C 0x40C 0x80C	*TBD* (32)	TBD
PROD_DATE (31 dnto 0)	0x010 0x410 0x810	*PROD_DATE* (32)	Defines the production date of the mezzanine card and the module. Date format is 0xDDMMYYYY.

Table E.3: Table of Configuration Memory Registers (continued).

CM_REG	VME_CMR_ADDR	CMR_DETAIL	Description
PROD_DATE (31 dnto 0)	0x010 0x410 0x810	*PROD_DATE* (32)	Defines the production date of the mezzanine card and the module.
CPLD_FIRM (31 dnto 0)	0x820	*CPLD_FIRM* (32)	Defines the firmware version of the CPLD (*U8*). Format is for firmware is 0xVVVVYYYY, where VVVV gives the firmware revision number and YYYY the year of release.
DSP_FIRM (31 dnto 0)	0x824	*DSP_FIRM* (32)	Defines the firmware version of the DSP-FPGA (*U9*).
MEM_FIRM (31 dnto 0)	0x828	*MEM_FIRM* (32)	Defines the firmware version of the MEM-FPGA (*U25*).
SI_FIRM (31 dnto 0)	0x02C 0x42C 0x82C	*SI_FIRM* (32)	Defines the firmware version of the SI (*U11*).
*TEMP*0 (9 dnto 0)	0x040 0x440	*AMC_TMP_TOP* (10)	Temperature measured by the *TMP*175 placed on the top layer of the AMC (see section 4.1.3). All temperature and voltage values are updated after toggling Fast Register *TRG_TEMP_RDOUT* (Tab. E.2).
*TEMP*0 (25 dnto 16)	0x040 0x440	*AMC_TMP_BOT* (10)	Temperature measured by the *TMP*175 placed on the bottom layer of the AMC.
*TEMP*0 (9 dnto 0)	0x840	*DSP_TMP* (10)	Temperature measured by the SystemMonitor (inside the DSP-FPGA (*U9*)).
*TEMP*0 (19 dnto 10)	0x840	*DSP_TMP_MAX* (10)	Maximum temperature measured by the SystemMonitor since configuration.

Table E.3: Table of Configuration Memory Registers (continued).

CM_REG	VME_CMR_ADDR	CMR_DETAIL	Description
$TEMP0$ (29 dnto 20)	0x840	DSP_TMP_MIN (10)	Minimum temperature measured by the SystemMonitor since configuration.
$TEMP1$ (9 dnto 0)	0x844	MEM_TMP (10)	Temperature measured by the SystemMonitor (inside the MEM-FPGA ($U25$)).
$TEMP1$ (19 dnto 10)	0x844	MEM_TMP_MAX (10)	Maximum temperature measured by the SystemMonitor since configuration.
$TEMP1$ (29 dnto 20)	0x844	MEM_TMP_MIN (10)	Minimum temperature measured by the SystemMonitor since configuration.
$VCCAUX0$ (9 dnto 0)	0x860	DSP_AUX (10)	Auxiliary voltage ($U_{AUX} = 2.5\,\mathrm{V}$) measured by the SystemMonitor (inside the DSP-FPGA ($U9$)).
$VCCAUX0$ (19 dnto 10)	0x860	DSP_AUX_MAX (10)	Maximum auxiliary voltage measured by the SystemMonitor since configuration.
$VCCAUX0$ (29 dnto 20)	0x860	DSP_AUX_MIN (10)	Minimum auxiliary voltage measured by the SystemMonitor since configuration.
$VCCAUX1$ (9 dnto 0)	0x864	MEM_AUX (10)	Auxiliary voltage ($U_{AUX} = 2.5\,\mathrm{V}$) measured by the SystemMonitor (inside the MEM-FPGA ($U25$)).
$VCCAUX1$ (19 dnto 10)	0x864	MEM_AUX_MAX (10)	Maximum auxiliary voltage measured by the SystemMonitor since configuration.
$VCCAUX1$ (29 dnto 20)	0x864	MEM_AUX_MIN (10)	Minimum auxiliary voltage measured by the SystemMonitor since configuration.
$VCCINT0$ (9 dnto 0)	0x880	DSP_INT (10)	Internal voltage ($U_{INT} = 1.0\,\mathrm{V}$) measured by the SystemMonitor (inside the DSP-FPGA ($U9$)).
$VCCINT0$ (19 dnto 10)	0x880	DSP_INT_MAX (10)	Maximum internal voltage measured by the SystemMonitor since configuration.

Table E.3: Table of Configuration Memory Registers (continued).

CM_REG	VME_CMR_ADDR	CMR_DETAIL	Description
*VCCINT*0 (29 dnto 20)	0x880	*DSP_INT_MIN* (10)	Minimum internal voltage measured by the SystemMonitor since configuration.
*VCCINT*1 (9 dnto 0)	0x884	*MEM_INT* (10)	Temperature measured by the SystemMonitor (inside the MEM-FPGA (*U25*)).
*VCCINT*1 (19 dnto 10)	0x884	*MEM_INT_MAX* (10)	Maximum internal voltage measured by the SystemMonitor since configuration.
*VCCINT*1 (29 dnto 20)	0x884	*MEM_INT_MIN* (10)	Minimum internal voltage measured by the SystemMonitor since configuration.
UCD_RL0-7 (31 dnto 0)	0x8A0 - 0x81C	TBD	Voltage information measured from the UCD9081 can be stored here. TBD.
DAC_VAL0-3 (15 dnto 0)	0x0C0-0x0C3 0x4C0-0x4C3	*DAC_VAL0-3* (16)	DAC values for the first four ADCs (CH0 - CH3) located on a AMC.
DAC_VAL0-3 (31 dnto 16)	0x0C0-0x0C3 0x4C0-0x4C3	*DAC_VAL4-7* (16)	DAC values for the second four ADCs (CH4 - CH7) located on a AMC.
THR_VAL0-3 (15 dnto 0)	0x0C0-0x0C3 0x4C0-0x4C3	*THR_VAL0-3* (16)	Threshold values (in ADC LSB) to generate a self trigger for the first four ADCs (CH0 - CH3) located on a AMC.
THR_VAL0-3 (31 dnto 16)	0x0C0-0x0C3 0x4C0-0x4C3	*THR_VAL4-7* (16)	Threshold values (in ADC LSB) to generate a self trigger for the second four ADCs (CH4 - CH7) located on a AMC.
SI_CONF0-11 (31 dnto 0)	0x200-0x22C 0x600-0x62C 0xA00-0xA2C	*SI_CONF0-1* (32)	Configuration register for the programming of the SI5326. The registers are arranged as defined in the text format output of the software utility, *DSPLLsim*, provided by Silicon Labs.

Table E.3: Table of Configuration Memory Registers (continued).

CM_REG	VME_CMR_ADDR	CMR_DETAIL	Description
G_CONF0 (15 dnto 0)	0xB00	*GEN_LAT* (16)	Generic latency value for the time window wherein occuring signals were processed. This register is used in transient analyzer and TDC mode.
G_CONF0 (31 dnto 16)	0xB00	*GEN_FRA* (16)	Generic window size value for the time window wherein occuring signals were processed. This register is used in transient analyzer and TDC mode.
G_CONF1 (15 dnto 0)	0xB04	*GEN_THR* (16)	Generic threshold value to generate a self trigger.
G_CONF1 (31 dnto 16)	0xB04	*GEN_FT* (16)	Generic threshold value to generate a fast trigger send to the TIGER module.
G_CONF2 (13 dnto 0)	0xB08	*GEN_BASE* (14)	Baseline Level to where the input circuit are set to.
G_CONF2 (16)	0xB08	*GEN_CLK_SRC* (1)	Defines type of mounted GIMLI card. **0** fiber, **1** OCXO
G_CONF3 (7 dnto 0)	0xB0C	*DAC_SET_TRL* (8)	Defines number of failed DAC calibrations until error occurs.
G_CONF3 (31 dnto 16)	0xB0C	*DAC_INIT* (16)	Defines initial DAC value.
G_CONF4 (5 dnto 0)	0xB10	*CAL_TRG* (6)	Defines TCS calibration trigger type accepted by GANDALF.
G_CONF4 (8)	0xB10	*CTRG_EN* (1)	**1** Enables or **0** disables calibration trigger
G_CONF4 (13 dnto 10)	0xB10	*RDM* (4)	Defines readout mode parameter (see section F.1).
G_CONF5 (23 dnto 16)	0xB14	*PRESCALE* (16)	Defines Prescaler Value to determine trigger sequence for debug mode readout.
G_CONF6 (31 dnto 0)	0xB18	TBD	TBD

Table E.3: Table of Configuration Memory Registers (continued).

CM_REG	**VME_CMR_ADDR**	**CMR_DETAIL**	**Description**
G_CONF7 (31 dnto 0)	0xB1C	TBD	TBD
FRA_LAT0-15 (15 dnto 0)	0xB20-0xB4C	*LATENCY0-15* (16)	Latency value for the time window wherein occuring signals were processed (CH0-CH16). This register is used in transient analyzer and TDC mode.
FRA_LAT0-15 (31 dnto 16)	0xB20-0xB4C	*FRAMEW0-15* (16)	Window size/Framewidth value for the time window wherein occurring signals were processed (CH0-CH16). This register is used in transient analyzer and TDC mode.

F. Appendix: GANDALF Data Format Definitions

F.1 GANDALF Data Format

The data format chosen for the GANDALF module is compatible with the S-LINK protocol as defined in the S-LINK specification [46]. The structure of the S-LINK header is given in the first three words in Tab. F.2. The *format(8)* byte, written in the third word of the header, covers extended information about the configuration of the GANDALF modules (see Tab. F.1). There is a separation between the first event in a run (FER) and a first event in a spill (FES). A detailed description of the COMPASS online data format can be found in [73].

F.1.1 GANDALF Transient Analyzer Data

A GANDALF module equipped with two AMCs can operate as a *transient analyzer*. The AMC can be used in *normal* or *time-interleaved* digitization mode. Therefore, the number of effective digitization channels changes respectively. In *normal mode* 8 ADCs of one AMC build eight effective channels. In the *time-interleaved mode* the 8 ADCs build 4 effective channels. This enumeration of effective channels is used to declare the corresponding channels in the data format.
When the GANDALF module is used as transient analyzer, the following information is given in the FER and FES:

- The serial numbers and configuration status (e.g. *normal* or *time-interleaved mode*) of the used modules and mezzanine cards.
- The sourceID of the GANDALF module and its location in the VME crate (crate slot number).
- The version number of the firmware for the FPGAs.
- Temperatures and voltages measured by the monitoring system.
- DAC and threshold values for the different analog input channels.

The detailed data format structure of the FER and the FES is given in Tabs. F.2 and F.3 respectively. Some of the values mentioned above can be set by writing them into the *Configuration Memory* and are printed in bold letters (see section 4.2.3 and App. E.3).
For events generated by a physics trigger, from two kinds of data modes can be selected:

- **Normal Data Mode**

  In this mode, the GANDALF module outputs the processed data in data blocks per hit, if the algorithm has detected one or more pulses inside the given window with the corresponding latency. In *Normal Data Mode* the dataset for one physical event consists of n data blocks and includes the following information:

  – Integral of all sampling values measured in the frame. A frame is a defined number of sampling words.
  – The maximum amplitude of the corresponding hit.
  – The calculated time information of the corresponding hit. It is separated in 28 bit coarse time information (number of sampling units) and 10 bit high resolution time information (subdividing the sampling unit by 1024).

  The detailed structure of an event in *Normal Data Mode* is given in Tab. F.4.

- **Debug Data Mode**

  In this mode, the GANDALF module outputs both, the during the defined time window recorded frame and the processed data. The length of the frames depends on the selected window length (see section 4.2.3). The structure of the GANDALF *Debug Data Mode* consists of an event header, data blocks and an event trailer, containing the following information:

  – System monitoring information: FPGA configured, Si locked, TCS status, voltages and temperatures.
  – Readout mode (RDM): Normal or Debug Data Mode.
  – The window size and the digitized frame data.
  – Processed data, as mentioned above, for each hit inside the frame.
  – A pulse detection flag which signalizes that the algorithm has detected hits inside the frame.

  The detailed structure of an event in *Debug Data Mode* is given in Tab. F.5.
  With the register *PRESCALE* (see Tab. E.3), the occurrence of events in Debug Data format can be selected. By setting the integer value n in the *PRESCALE* register, every n-th event is transferred in Debug Data format and all remaining events are in *Normal Data Mode*. For $n = 0x0$, any event is processed in *Debug Data Mode*.

F.1.2 GANDALF TDC Data

A GANDALF module equipped with two DMCs can operate as a 128 channel TDC. In this mode, the GANDALF module generates the same data structure as the CATCH module with 16 installed $\mathcal{F}$1-TDCs [73]. A GANDALF module generates TDC data in the same format as a CATCH module to comply with existing offline analysis software [91]. The window and latency values for the TDC functionality can be set by choosing the corresponding registers in the *Configuration Memory* (see Tab. E.3).

Table F.1: Format definition

7	6	5	4	3	2	1	0
1 = first event of a run (else 0)	1 = HOTL. CMC 0 = TDC-CMC/ G-TDC	1 = l & t edge 0 = l or t edge	1 = high res 0 = norm res	1 = latch mode 0 = no latch mode		1 = sparsi-fied mode 0 = debug mode	1=TDC readout
1 = first event of a run (else 0)	0 = GeSiCA (APV) 1 = GANDALF-ADC 2 = GANDALF-Scaler 3 = Scaler-CMC 4 = FI-ADC HOTLink 5 = RICH HOTFiber 6 = 7 = Scaler HOTLink			0 = nml mode, processed data 1 = nml mode, frame data 2 = nml mode, debug data 3 = 4 = ilm mode, processed data 5 = ilm mode, frame data 6 = ilm mode, debug data 7 =			0=ADC or scaler readout

Table F.2: First Event of Run Header from GANDALF.

31 0

S-Link Header

err	ev. type (5)	source ID (10)			event size excl. CTRL (16)		
stat	spill no. (11)		event no. (20)				
format (8)			#errorwords (8)		tcs error (8)		status (8)

First Event of Run Header

GANDALF S/N (10)			GANDALF srcID (10)		CrateSlot (5)		#AMC(2)		SysMon (5)
DSP-FPGA usrID (16)					MEM-FPGA usrID(16)				
CPLD Firmware Version (32)									
DSP Firmware Version (32)									
MEM Firmware Version(32)									
TBD (24)								SI Conf. Type(8)	
TBD (16)					GANDALF status (16)				
TBD (6)	DSP-FPGA TEMP (10)				TBD (6)	MEM-FPGA TEMP (10)			
TBD (6)	DSP-FPGA VCC1V0 (10)				TBD (6)	MEM-FPGA VCC1V0 (10)			
TBD (6)	DSP-FPGA VCCAUX (10)				TBD (6)	MEM-FPGA VCCAUX (10)			

TBD (16)							AMC1 S/N (10)		AMC1 cfg (6)
TBD (16)							AMC2 S/N (10)		AMC2 cfg (6)
TBD (6)	LOLS (2)		AMC1 Ch. ON (8)				CALDONE (8)		CALERR (8)

Table F.2: Format of the First Event of Spill Header from GANDALF (continued).

31 0

TBD (6)	LOLS (2)	AMC2 Ch. ON (8)	CALDONE (8)	CALERR (8)
TBD (8)		AMC1 Temp. top&bot (24)		
TBD (8)		AMC2 Temp. top&bot (24)		

DAC 0 value (16)	DAC 8 value (16)
...	
DAC 7 value (16)	DAC 15 value (16)

Thrsld. 0 value (16)	Thrsld. 8 value (16)
...	
Thrsld. 7 value (16)	Thrsld. 15 value (16)

Data words

Table F.3: First Event of Spill Header from GANDALF.

31 0

S-Link Header

err	ev. type (5)	source ID (10)	event size excl. CTRL (16)	
stat	spill no. (11)	event no. (20)		
format (8)		#errorwords (8)	tcs error (8)	status (8)

First Event of Spill Header

GANDALF S/N (10)	GANDALF srcID (10)	CrateSlot (5)	#AMC(2)	SysMon (5)
GANDALF status (16)		TBD (16)		
TBD (6)	DSP-FPGA TEMP (10)	TBD (6)	MEM-FPGA TEMP (10)	
TBD (6)	DSP-FPGA VCC1V0 (10)	TBD (6)	MEM-FPGA VCC1V0 (10)	
TBD (6)	DSP-FPGA VCCAUX (10)	TBD (6)	MEM-FPGA VCCAUX (10)	

TBD (16)			AMC1 S/N (10)	AMC1 cfg (6)
TBD (16)			AMC2 S/N (10)	AMC2 cfg (6)
TBD (6)	LOLS (2)	AMC1 Ch. ON (8)	CALDONE (8)	CALERR (8)
TBD (6)	LOLS (2)	AMC2 Ch. ON (8)	CALDONE (8)	CALERR (8)
TBD (8)		AMC1 Temp. top&bot (24)		
TBD (8)		AMC2 Temp. top&bot (24)		

Table F.3: Format of the First Event of Spill Header from GANDALF (continued).

31 0

DAC 0 value (16)	DAC 8 value (16)
...	
DAC 7 value (16)	DAC 15 value (16)
Thrsld. 0 value (16)	Thrsld. 8 value (16)
...	
Thrsld. 7 value (16)	Thrsld. 15 value (16)
Data words	

Table F.4: Data format of the GANDALF Normal Data Mode.

31 0

0-16× (n× DATA Blocks)

1	ch (4)	TBD (Baseline) (11)	Integral (16)
1	Coarse Time DATA MSB (17)		max Amplitude (14)
1	Coarse Time DATA LSB (21)		High Res Time(10)

Table F.5: Data format of the GANDALF Debug Data Mode.

31 0

0-16× (Header, n× DATA words, Trailer)

0	0	event no. (6)	ch. ID (4)	SysMon (5)	Window Length (11)	RDM (4)

1	0	Data Word 0 (14)	0	0	Data Word 1 (14)
1	0	Data Word 2 (14)	0	0	Data Word 3 (14)
		...			
1	0	Data Word n-1 (14)	0	0	Data Word n (14)

1	0	0	PulseDet (1)	BaslErr (1)	”0 - 0” (13)	max Amplitude (14)
1	0	1	”0 - 0” (13)		Integral (16)	
1	1	0	Frame Time (12)		Coarse Time MSB (17)	
1	1	0	”0 - 0” (8)	Coarse Time LSB (21)		
1	1	1	”0 - 0” (19)		High Res Time (10)	

0	1	event no. (6)	ch. ID (4)	SysMon (5)	Window Length (11)	RDM (4)

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Danksagung

Diese Arbeit wäre nicht möglich gewesen ohne die Unterstützung vieler aus meinem Umfeld. Ich möchte mich bedanken bei:

- Prof. Dr. Horst Fischer für seine stets professionelle, offene und freundschaftliche Betreuung.
- Prof. Dr. Kay Königsmann dafür, dass ich diese Arbeit in seiner Arbeitsgruppe als Teil der COMPASS Kollaboration schreiben konnte.
- Sebastian Schopferer für die spannende und unterhaltsame Zeit, in der wir in perfekter Teamarbeit dieses Projekt in die Welt gesetzt haben.
- Dem Hardware Team unserer Abteilung für die Umsetzung aller gemeinsamen Ideen: Max Büchele, Louis Lauser, Christian Schill und Stefan Bartknecht.
- Sebastian Schopferer, Tillmann Guthörl, Johannes ter Wolbeek, Julia Vogel, Carolin Mecus und Christian Schill für das sorgfältige Korrekturlesen dieser Arbeit.
- Martin Kienzler für die Geduld, die nötig war die GANDALF Platine zu erstellen.
- Rainer Fastner für die sehr angenehmen Diskussionen über die technischen und alltäglichen Details.
- Bei allen Mitgliedern unserer Abteilung für die gute und positive Atmosphäre: Max Büchele, Sebastian Schopferer, Louis Lauser, Julia Vogel, Heiner Wollny, Johannes ter Wolbeek, Tillmann Guthörl, Christiane Imlintz, Rainer Fastner, Christian Schill, Donghee Kang, Donghwa Kang, Stefan Sirtl, Elisabeth Wursthorn, Andreas Mutter, Frank Nerling, Elisabeth Gruber, Katharina Schmidt, Tobias Baumann, Tobias Szameitat, Tobias Kunz, Phillip Jörg, Matthias Gotzelik, Khalil Rehmani und Susanne Rombach-Mikl.

- Meiner Familie und insbesondere meinen Eltern, für die liebevolle Unterstützung in den vergangenen Jahren.