First test of the COMPASS-GASSIPLEX chip

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Introduction

We have performed a first set of tests to study the performances of the new version of the GASSIPLEX chip, produced by IMEC and based on the project of J.C. Santiard (EP/MIC - CERN), the **COMPASS-GASSIPLEX:**

1) full functionality
2) noise level
3) linearity
4) dynamic performance
5) possible generation of parasitics with logic signals
6) measurement of out-put DC level (pedestal)
7) gain uniformity between different channels
8) check of peaking time variation
9) variation of DC level with temperature
10) behavior of GASSIPLEX with different supply voltages
11) power consumption
12) gain

The number of chips under tests was 20, prototypes produced in a multiproject run.

In order to do the test, J.C. Santiard has prepared a PC test board which hauses one COMPASS-GASSIPLEX, the 16 input and the two output connectors and all the logic and bias signals required to run the chip.
The COMPASS-GASSIPLEX design report from IMEC and the logical scheme of the test board are herewith enclosed .

The tests have been performed with a delta pulse input charge generated by a pulse generator through a 1.8 pF capacitor. Each output of the gassiplex was connected to a unity gain, wide band video Op-Amp (EL2170cn), in order to drive a 50 ohm cable.

For some tests, due to the their limit in the dynamic range (the same voltage supply has been used both for the gassiplex and for the output buffers) , the amplifiers have been removed and the output measured directly with a high impedance probe and an oscilloscope.
The effective gain of the preamplifier and the tail of the shaped signal, have to be measured with signals generated by a MWPC.

Results

1) full functionality:

All the 20 IC' s have been tested with different input signals channel by channel.

A complete test of all the parameters of the (16 x 20) channels has not yet been performed, but all the channels of all the chips have output signals, and no major difference between them have been reported.

2) noise level

An evaluation of the noise has been realized with a MCA. For this test, two different input charges (20 fC and 40 fC) have been amplified via the same GASSIPLEXchannel and the out-put read by the ADC of the MCA.
The measurement have been performed with a total input capacitance of 25 pF.
Using the formula:

$$N = [\Delta Q\ (C)\ /D] \times [FWHM/2.35] \times [1/1.6 \times 10^{-19}\ (C)]$$

we found a noise level, measured for two different values of the output multiplexer rate, of about (fig. 1):

820 e^- @ 1MHz

1300 e^- @ 20 MHz

The noise of the pulse generator have not been subtracted. Thus these measurements must be regarded as upper limits. At 20 MHz, the measurement has been done on the whole area of the output pulse instead of on the plateau, due to the minimum gate width accepted by the MCA. This gives fluctuations larger than the ones of the signal plateau: for this measurement the resulting value is certainly largely overestimated.

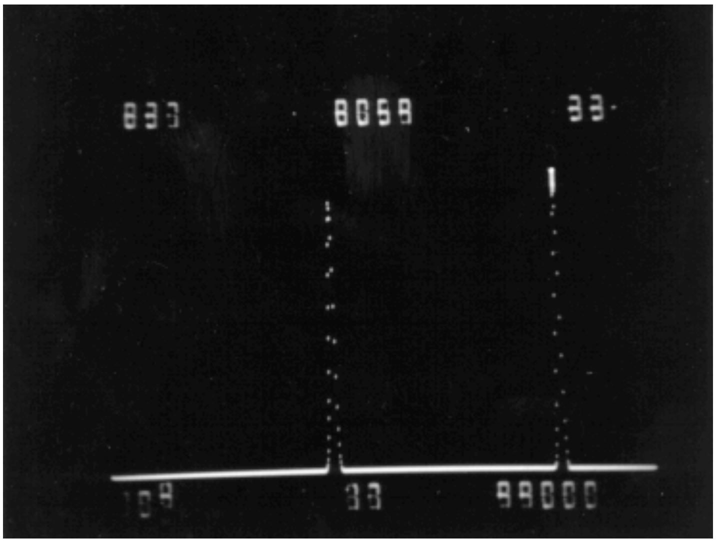
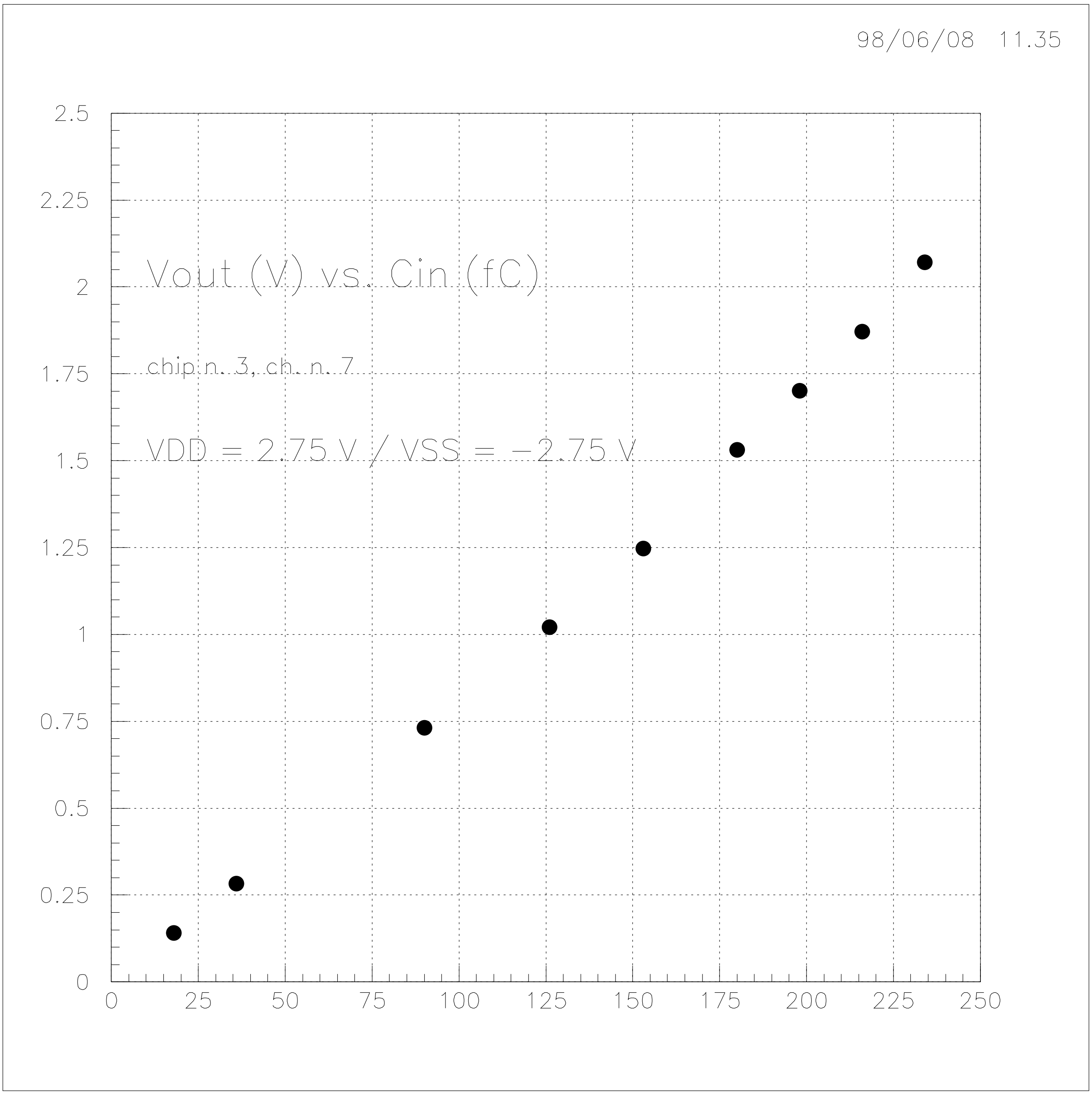


fig. 1

3) linearity

The linearity measurement is just a rough estimation of the complete test we foresee to do, as it has been measured via the scope. Obviously we need to have a complete and precise check of this important parameter via a set-up with an ADC, that was not available at the time of the test. There are several parameters that influence the measurement of the linearity for a single channel, and that afflict the difference between the channels: the scope sensitivity at different gain, the difference between the input resistance (with a tollerance of 5%) and capacitance (5%) and so on.

In the following picture (fig. 2) we see the Vout (V) vs. Qin (fC) at the voltage supply of +/- 2.75 V for one particular channel (chip n.3, ch n. 7):



(fig. 2)

For some comments about this plot, see also below, section (8), check of peaking time variation vs. applied resistance.

4) dynamic performances

We varied, at the maximum output value Vout = 2 V, three different parameters:

- the voltage supply Vcc,
- the bias current ISHAP via the R20 resistor
- the multiplexer frequency f

in order to see how Td (time delay), Tr (rise time) and Tf (fall time) are influenced by these parameters.

We found the following results (tab. I):

	f = 20 Mhz R20 = 20 k Vcc = +/- 2.75	f = 20 Mhz R20 = 20 k Vcc = +/- 2.5	f = 20 Mhz R20 = 36 k Vcc = +/- 2.75	f = 20 Mhz R20 = 36 k Vcc = +/- 2.5	f = 1 Mhz R20 = 20 k Vcc = +/- 2.75
Td (ns)	39	43	42.5	44	36.5
Tr (ns)	8	9	13	16	9
Tf (ns)	10.5	11	14.5	18	12

tab. I

These parameters are also illustrated by the following pictures (fig. 3) and in fig. 4. The first picture of fig. 3 shows the output signal for Vcc= +/- 2.75 V and R20 = 20 kohm; the 20 Mhz clock is also shown. The second picture of fig. 3 shows the output signal for Vcc= +/- 2.75 V and R20 = 36 kohm; the 20 Mhz clock is also shown.

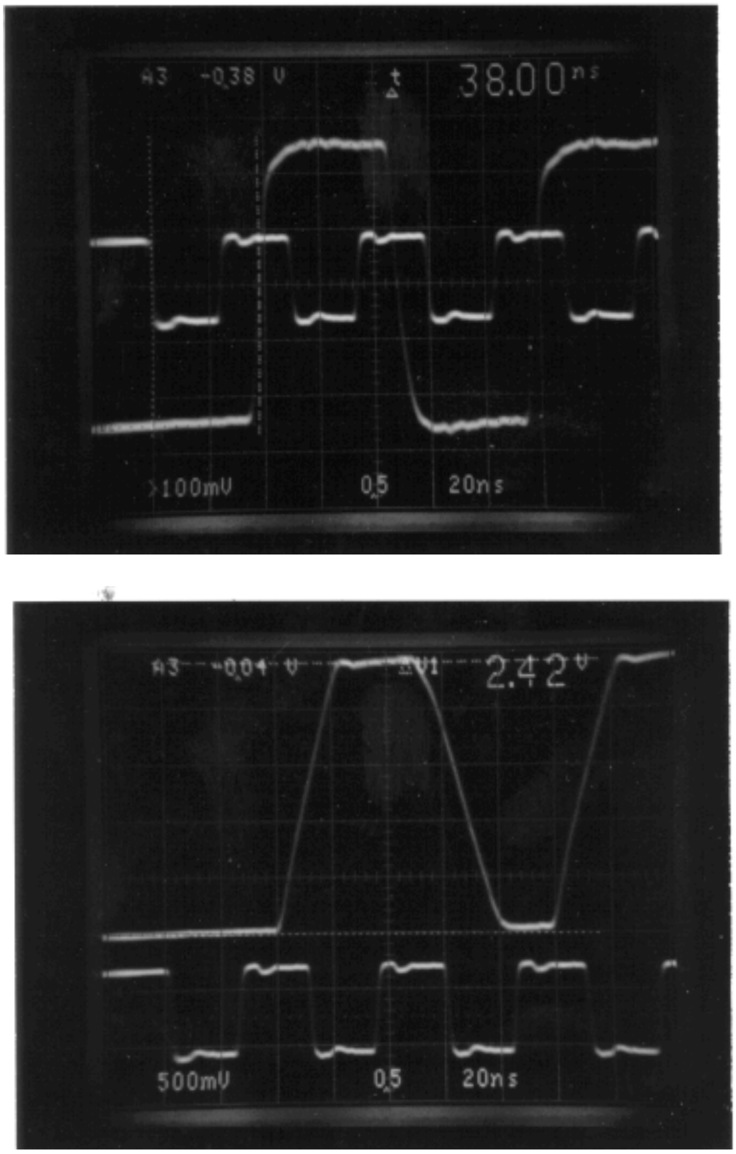
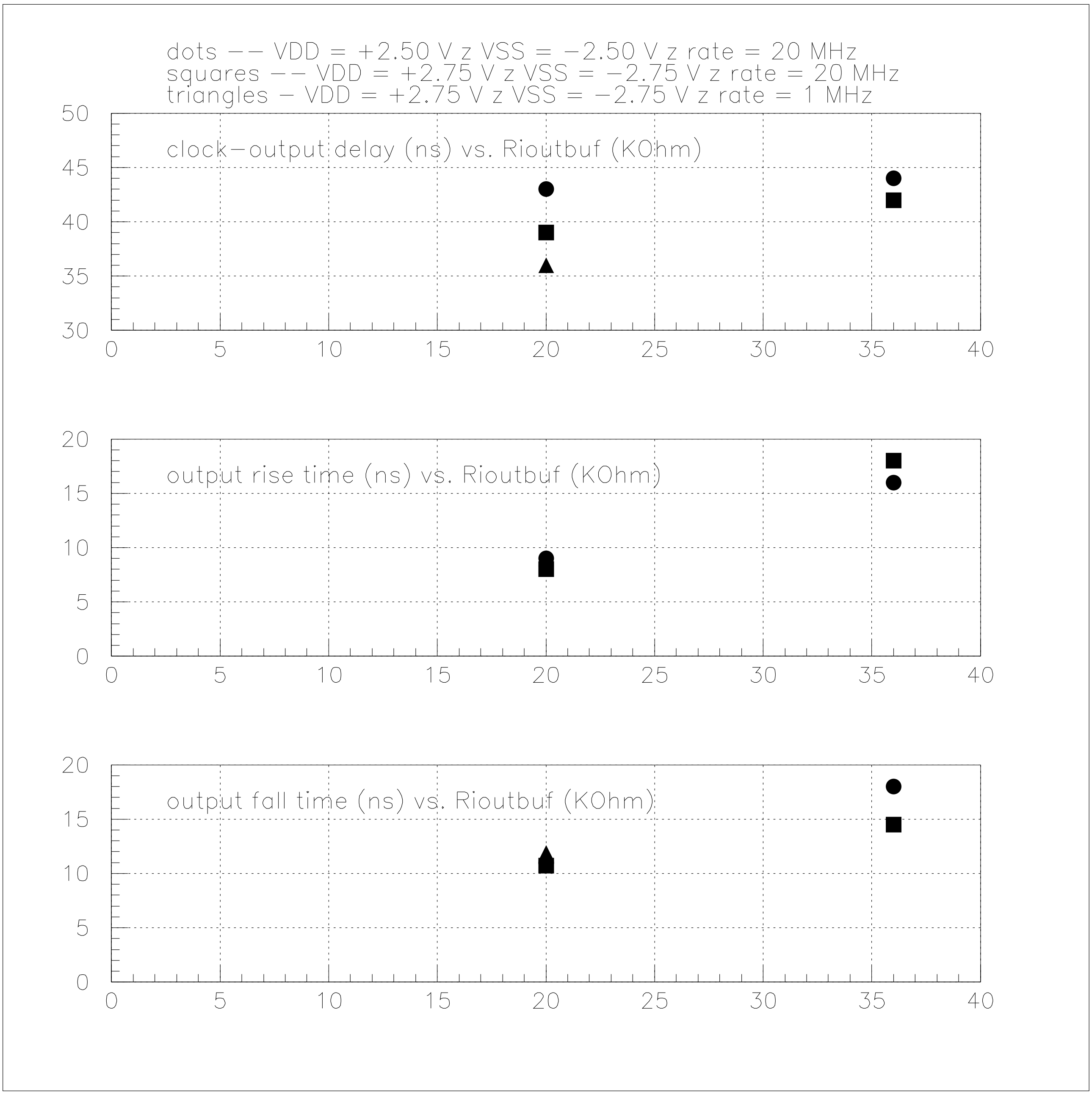


fig. 3



(fig. 4)

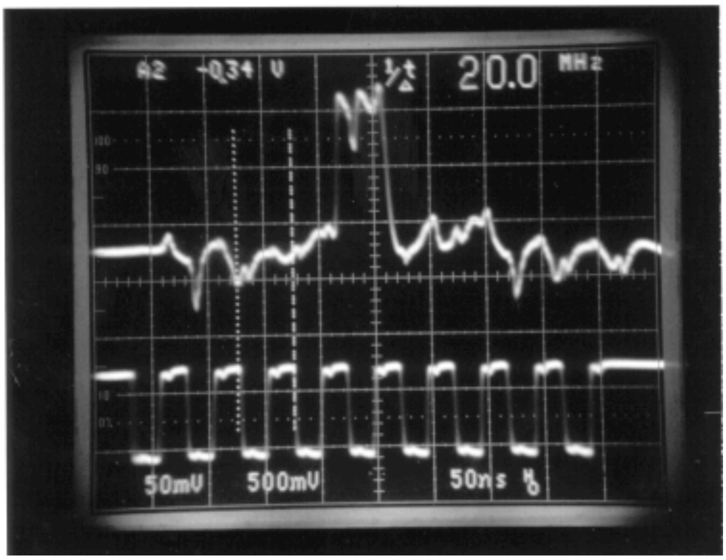
The **delay** of the first data, following the first clock cycle is, for the configuration f = 20 Mhz, R20 = 20 kohm and Vcc = +/- 2.75 V, about **39 ns**.

In conclusion, the multiplexer rate of 20 Mhz, that is one of the major difference with the old version of the GASSIPLEX, seems to be not a problem for the COMPASS-GASSIPLEX chips.

5) possible generation of parasitic with logic

The output 2 (wich correspond to the input channels 9 - 16) of the multiplexer, show some spikes in the output signal due to the clock signal.

In the following picture (fig. 5) it is possible to see these spikes on outbuf2; also shown the 20 MHz clock.:



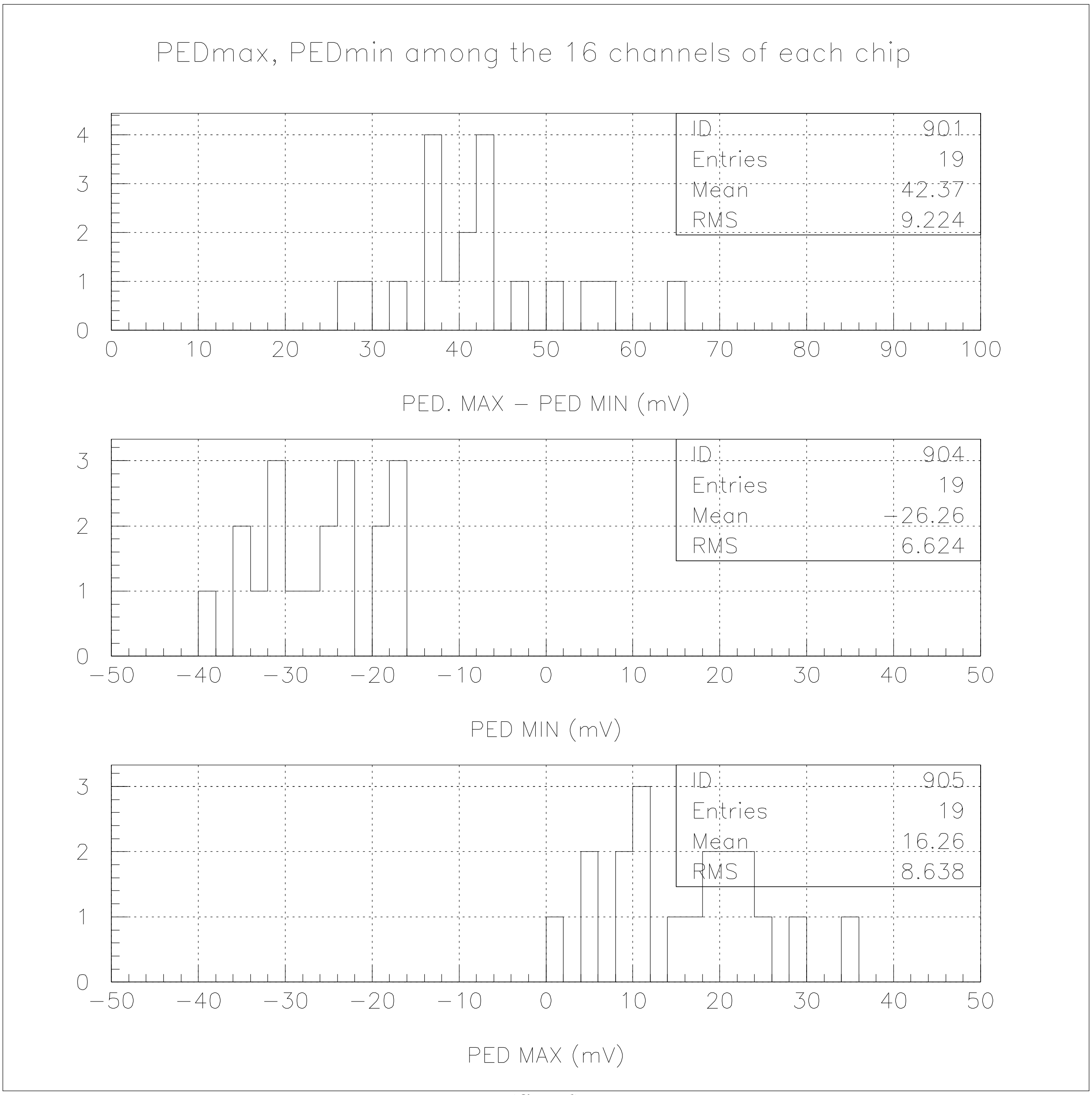
(fig. 5)

The reason for these parasitics seems to be due to the proximity of the bonding pads of the clock signal and output 2. It seems possible for the future to avoid this problem, with a different design of the bonding pads in the final version of COMPASS-GASSIPLEX, hopefully without the need of a further prototype.

6) measurement of output DC level (pedestal)

The output DC level (pedestal) with no signal at the inputs has been measured for the outputs of 19 IC' s. In this measure, the two outputs of the COMPASS-GASSIPLEX were connected to the output buffers.

In the following pictures (fig. 6) it is possible to see the difference PEDmax - PEDmin and the PEDmin and PEDmax distribution for the 19 chips tested:



(fig. 6)

In any case it will be necessary to avoid negative values of the pedestals, by adjusting the voltage Voutoff.

The pedestals dispersion between the 16 inputs of a single chip (n. 3), has been measured (fig. 7):

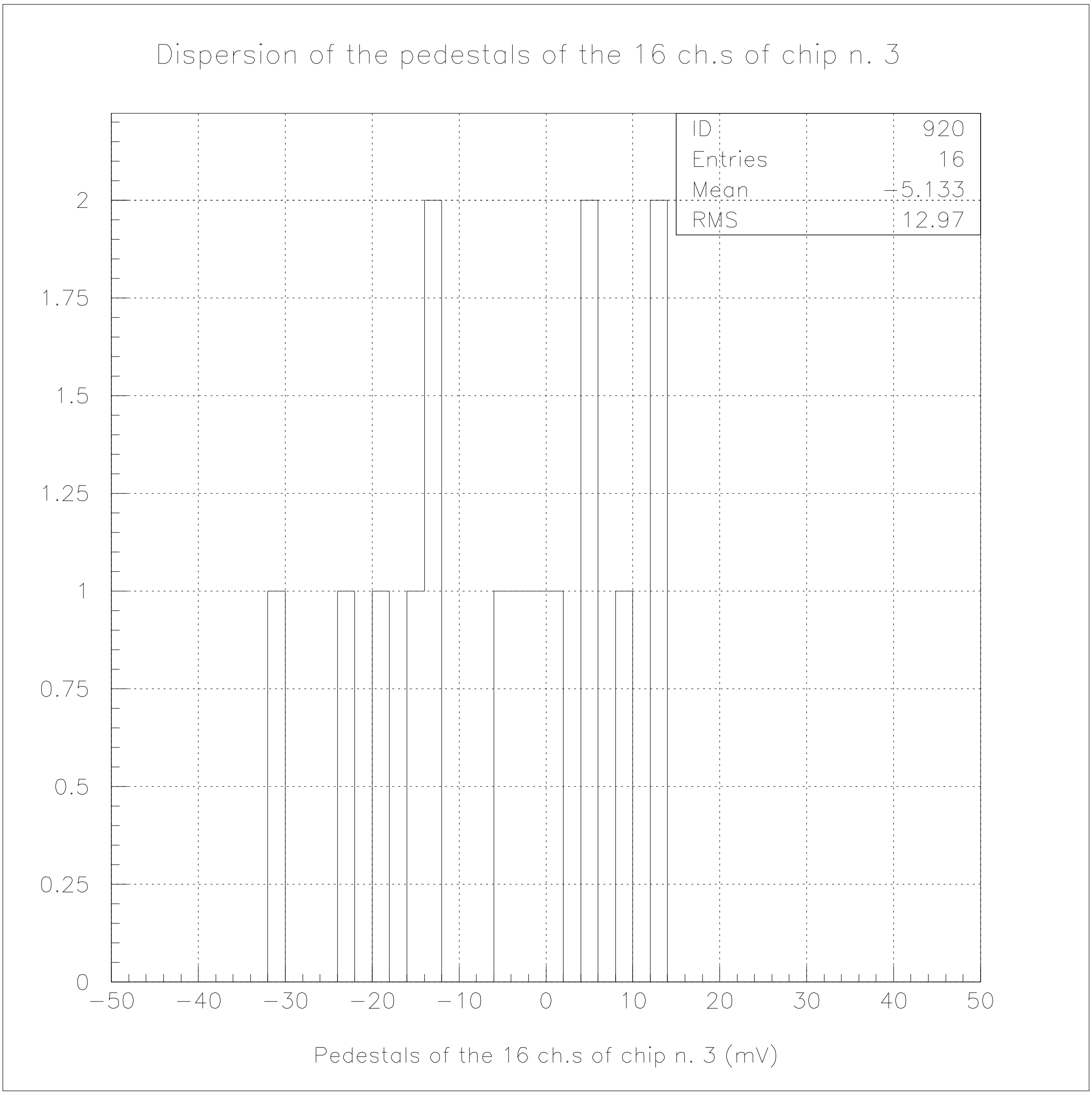


fig. 7

7) gain uniformity between different input channel

A detailed measurements of the output uniformity have been performed, and there are several data available. The measurement has been made without the output buffers, measuring directly the outputs with the scope in high impedance.

For example, in the following picture (fig. 8) it is possible to see the response of the 16 channels of chip n.3 for an input charge of 153 fC:

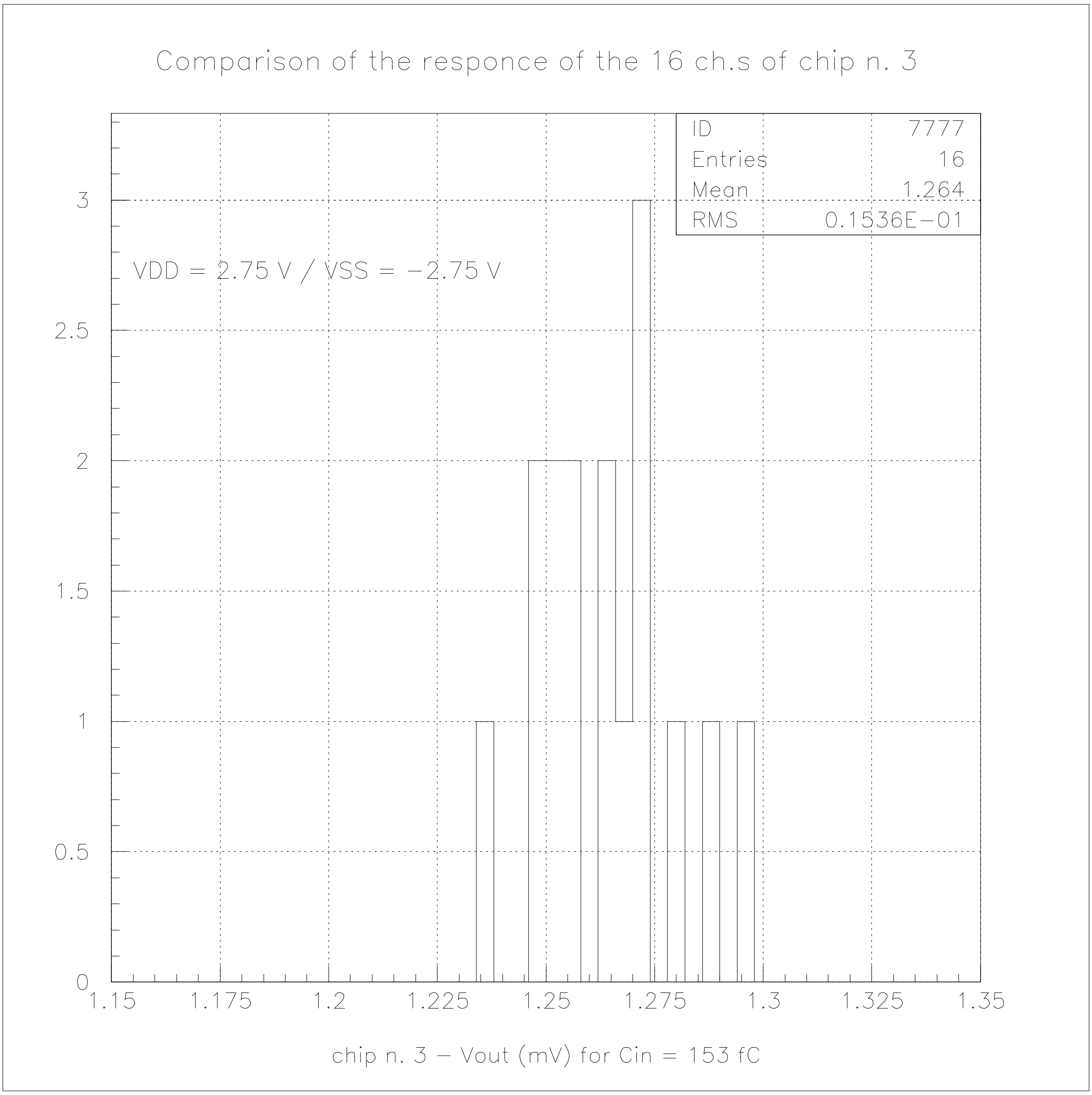


fig. 8

We have also the same measures at different value of the input charge and the dispersion in the output signal amplitude is almost the same.

8) check of peaking time variation vs. applied resistance

Another important parameter to check is the peaking time, in particular its dependence on the bias current controlled using resistor R20.

We have made this test in order to select the better value of ISHAP bias current, with a fixed input (wich correspond to an output signal of 400mV) and two different values of Vcc (+/- 2.75 V and +/- 2.5 V) (fig. 9, upper plots)

Furthemore, we have fixed the value of R20 (the resistance which set the ISAHP bias current) at two different values, and plotted the peaking time vs. Vout, to see how it fluctuate with the input signal (fig. 9, lower plots):

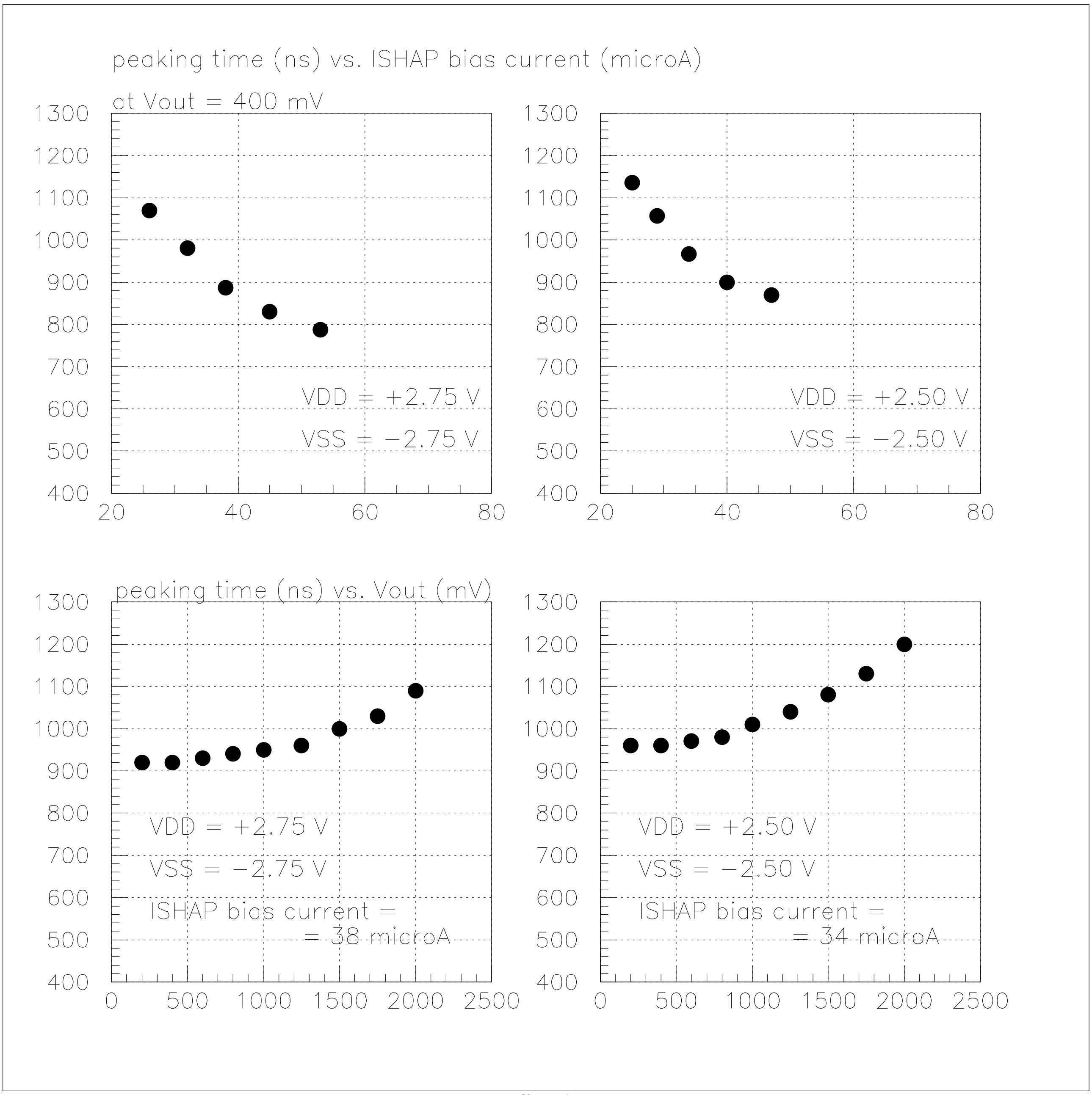


fig. 9

As it is possible to see, there is a quite considerable variation in the peaking time, that has to be taken into account in the project of the front end card and also in the evaluation of the resolution of the RICH detector. The effect is only seen in the effective linearity, and this effect is included in the measurement presented in fig. 2.

9) variation of DC level with temperature

The output DC level of several chip has been tested with two different temperature, and no relevant changes have been reported both at Vcc = +/- 2.5 V and Vcc = +/- 2.75 V (tab. II):

Vcc (V)	Temperature (C)	V output (mV)	mV/C
+/- 2.5	25	0	
+/- 2.5	57	- 4.3	- 0.13
+/- 2.75	25	0	
+/- 2.75	57	2.4	0.08

tab. II

In conclusion, it looks that the DC output level is poorly affected by the working temperature T, at least at this values of T.

10) behavior of GASSIPLEX with different supply voltages

In several of the previous tests, different values of voltage supply Vcc (in particular +/- 2.5 V, +/- 2.75 V) have been used, in order to understand how the COMPASS-GASSIPLEX chip is influenced by different values of the supply voltage.

From our test, it appears preferable for several reasons and, in particular, to obtain the best dynamic performanceses, to work at Vcc = +/- 2.75 V instead of the nominal value of Vcc = +/- 2.5 V.

11) power consumption

It is 167 mW per chip (10.4 mW per channel) for power supply set at at Vcc = +/- 2.5 V, and 182 mW per chip (11.4 mW per channel) for power supply set at at Vcc = +/- 2.75 V.

12) gain

The preliminary measurement of the gain is related to the measurement method. The value obtained is 6.5 mV/fC. Due to the different shape of the input signals, the gain for signal from MWPC’s can be slightly different.

ENCLOSURE 1

EUROPRACTICE
ASIC SERVICE

imec

Fax

To:
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From :
Katrien Marent
INVOMEC div. IMEC
fax : +32-(0)16-281584
e-mail : marentk@imec.be

Subject : design report CompassGassiplex
Date : 21/04/1998
Ref :

Message

Dear Mrs. Dalla Torre,

Please find hereafter some information on the CompassGassiplex chip.

On the last page of this fax you can find the bonding diagram of the chip.
Table below gives a complete description of the pins of the chip.

Pin #	Pin name	Pin description
1	in8	charge input of channel 8
2	in7	charge input of channel 7
3	in6	charge input of channel 6
4	in5	charge input of channel 5
5	in4	charge input of channel 4
6	in3	charge input of channel 3
7	in2	charge input of channel 2
8	in1	charge input of channel 1
9	cavity	
10	cal	calibration input
11	pre-bias	bias pin for preamplifier
12	irf	bias pin for feedback resistor of preamplifier
13	vroff	offset pin for feedback resistor of preamplifier
14	fil_ib	bias pin for filter

IMEC vzw • Kapeldreef 75 • B-3001 Leuven België • Tel.: +32 (0)16 281 250 • Fax: +32 (0)16 281 584
BTW: BE 425 260 668 • ASLK 001-1457488-42

15	shap_ib	bias pin for shaper
16	shift_bias	bias pin to tune the dynamic range, by changing this bias current the dynamic range can be slightly changed.
17	cavity	
18	gnda	analog ground
19	vss	negative supply voltage
20	vdda	positive supply voltage
21	outbuf1	output of the output buffer for the first 8 channels
22	iboutbuf	bias pin for the output buffers
23	outbuf2	output of the output buffer for the last 8 channels
24	clkin_srout	clock of the output multiplexer
25	clear_srout	clear of the output multiplexer
26	gndd	digital ground
27	vss	negative supply voltage
28	cavity	
29	vddd	positive supply voltage
30	ibth	bias pin for the track-and-hold buffer
31	phith	pin to put the track-and-hold buffer in track or hold mode
32	voutoff	offset voltage used in the shaper
33	vfilsw	pin to switch the filter on or off
34	clkin_srin	clock of the input multiplexer
35	clear_srin	clear of the input multiplexer
36	cavity	
37	in16	charge input of channel 16
38	in15	charge input of channel 15
39	in14	charge input of channel 14
40	in13	charge input of channel 13
41	in12	charge input of channel 12
42	in11	charge input of channel 11
43	in10	charge input of channel 10
44	in9	charge input of channel 9

The following bias voltages and currents are required:

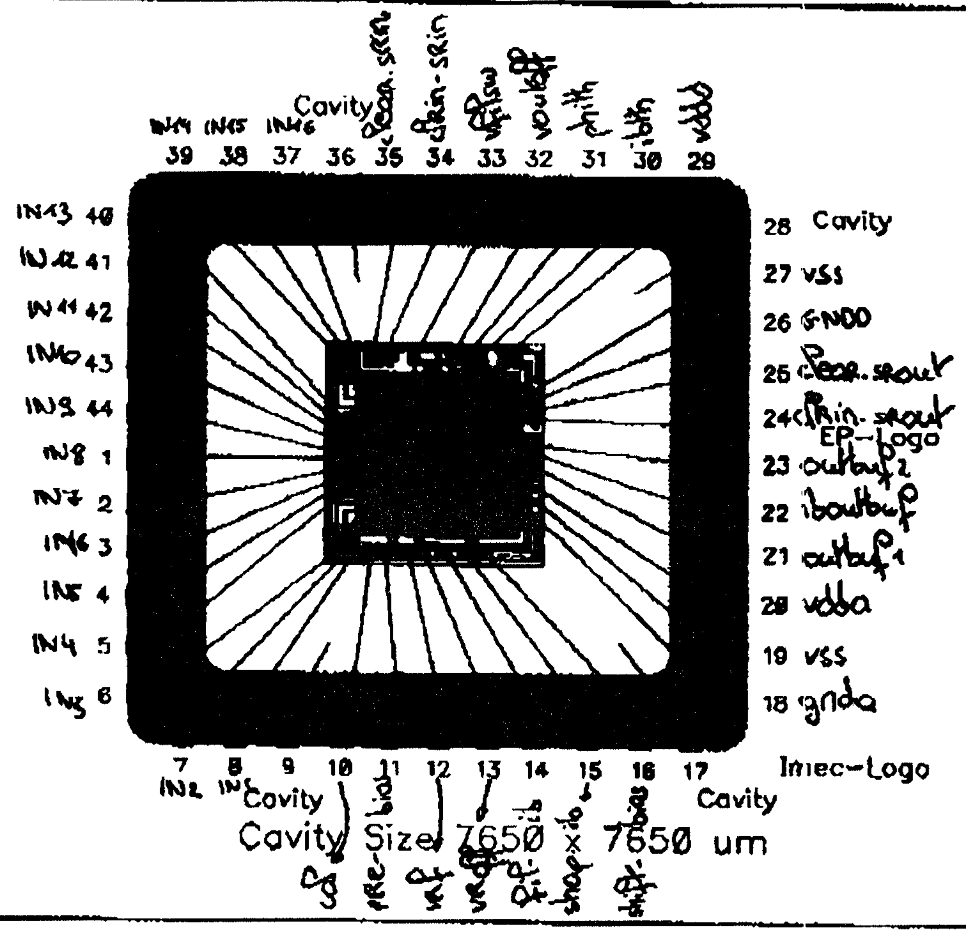
vroff	300mV
ishiftbias	6uA
irf	10uA
iprbias	50uA
ishap	35uA
ifil	5uA
ibth	20uA
ioutbuf	100uA
voutoff	125mV

The filter can be switched on by applying -2.5V to the vfilsw pin.
The input and outputmultiplexers are active when the clear is at -2.5V. So you can clear the multiplexers by applying 0V to the clear input pins.
The track-and-hold is in track mode when the 0V is applied to pin phith. It can be put in hold mode by applying -2.5V on the phith pin.
The peaking time can be adapted by changing the bias current of the shaper. In the following table you can find some simulation results of peaking time versus bias current of shaper.

shap_ib	Peaking time
40uA	950ns
35uA	1us
30uA	1.1us
25uA	1.16us

The simulated DC level on outbuf1 and outbuf2 is 6.4mV. But this value can be different on the actual chip since we cannot simulate offset accurately.

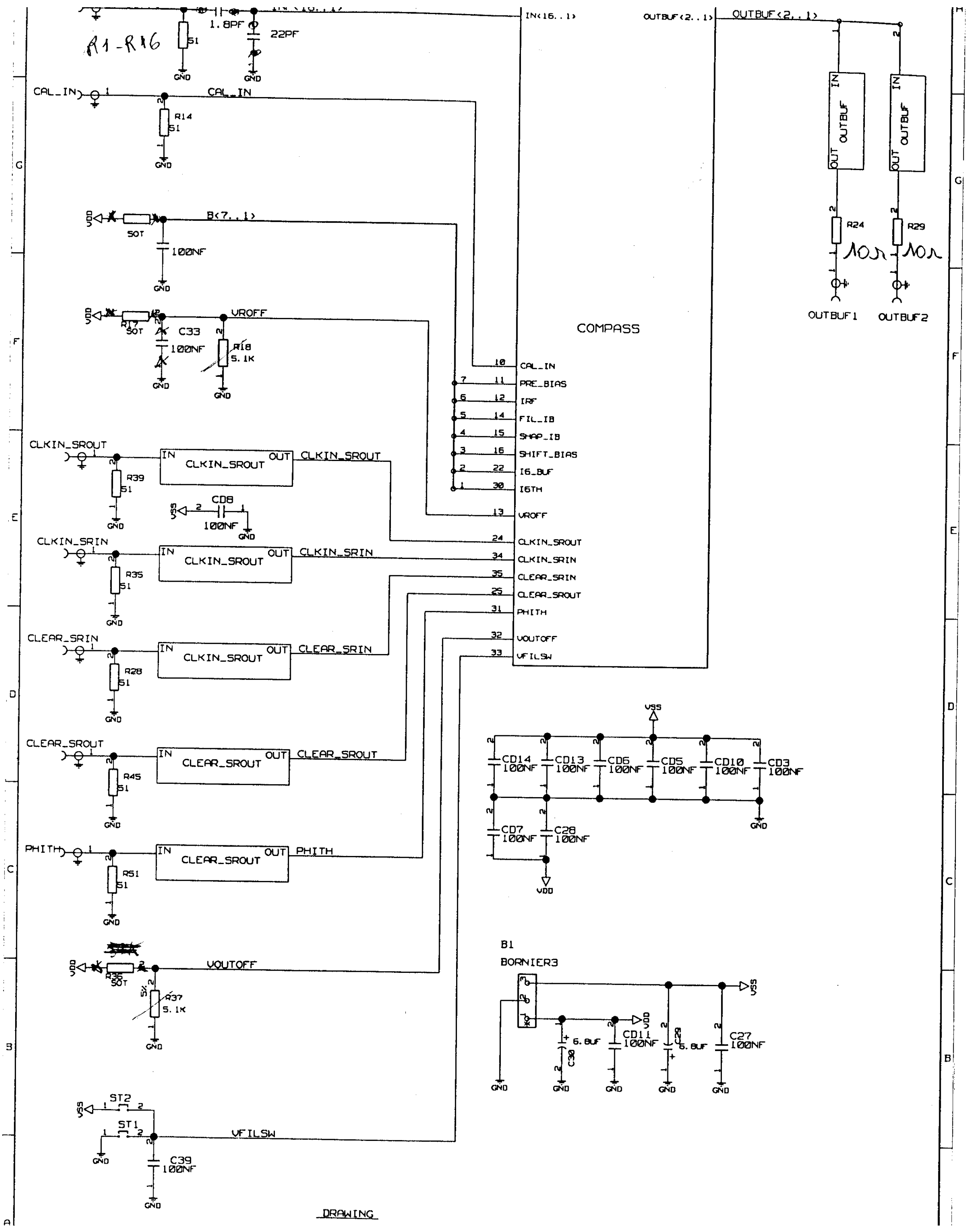
Request: EP 135 | LCC 44



Comment: Pins connected to cavity: 9-17-28-36

Project: CSND run 203	Date:	Scale 10
Die: 69203-R00360-01		
Size: 3940μ × 4300μ	Nr:	
Die Attach:	Europractice Asic Service Coordinated by IMEC	
Wire:		
Qty Samples: 20		
Lid: Taped ☒ Sealed ☐		

ENCLOSURE 2



R1-R16
1.8PF
22PF
51
GND
IN<16..1>
OUTBUF<2..1>
CAL_IN
R14
B<7..1>
50T
100NF
VROFF
R17
C33
R18
5.1K
COMPASS
CAL_IN
PRE_BIAS
IRF
FIL_IB
SHAP_IB
SHIFT_BIAS
I6_BUF
I6TH
VROFF
CLKIN_SROUT
CLKIN_SRIN
CLEAR_SRIN
CLEAR_SROUT
PHITH
VOUTOFF
VFILSW
R39
CD8
R35
R28
R45
R51
CLEAR_SRIN
CLEAR_SROUT
PHITH
VOUTOFF
R36
R37
ST2
ST1
VFILSW
C39
OUTBUF
R24
R29
10Ω
OUTBUF1
OUTBUF2
VSS
VDD
CD14
CD13
CD6
CD5
CD10
CD3
CD7
C28
B1
BORNIER3
6.8UF
C30
CD11
C29
C27
DRAWING