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FURTHER TESTS OF THE COMPASS-GASSIPLEX CHIP, WITH A DEDICATED EVALUATION BOARD

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1 Introduction

A new version of the COMPASS-GASSIPLEX (CG) chip is now available (second prototype, after the first one available in Spring 1998); the chip modification consists of a different design of the bonding pads to avoid the proximity of the "output 2" pad and the clock pad, which is probably the cause of some spikes observed in the output signals from "output 2" (for a description of the fault, see: F. Benedetti et al., "First tests of the COMPASS-GASSIPLEX chip", June 1998, Internal COMPASS Note 1998-3). The prototypes of this second iteration are encapsulated in a plastic package.

After some preliminary tests performed using the set-up already available for the tests of the first prototype, a new dedicated evaluation board has been designed with the aims of:

i. measuring the effective noise level from the CG in an environment as similar as possible to the final lay-out
ii. progress in the chip characterisation
iii. check and improve the PCB lay-out for the CG use.

This evaluation board consists of the first stage of the BORA Board (see G. Baum et al., "BORA: a front-end board, with local intelligence, for the RICH detector of the COMPASS collaboration", Nucl. Instr. Meth. A 433 (1999) 426) and it will be indicated in the following as BORA Board Prototype (BBP).

In this note, we report about the work done, which concerns mainly items (i) and (iii); priority has been given to study item (i) as the noise level is the crucial parameter to validate the chip design. Advances concerning item (iii) are a by-product. The chip characterisation (ii) will continue further.

2 Description of the equipment used for the measurements

The BBP is composed by two stages (fig. 1):

- Front-end electronics (based on the 16-channel front-end chip COMPASS-GASSIPLEX 0.7, custom);
- ADC converters (based on the dual channel, 20 MHz, 10 bit resolution SMOS ADC AD9201ARS by Analog Devices).

The timing diagram and the levels of control signals needed to operate the BBP are shown in fig. 2. The control signals are generated externally by standard generators (fig. 1) and have TTL level. The "Track and hold" (T/H) and "Reset" (RST) signals are generated by a pulse generator PM5786GB by Philips. The "Clock" signals (CLK) for COMPASS-GASSIPLEX and ADC are given by the Arbitrary Waveform Generator LW420A by LeCroy and have constant and stable time delay, so that the jitter between these CLK signals is minimised. The standard operation frequency of the clocks is 20 MHz, the same frequency that will be used in the final application.

The equipment used for the measurements (fig. 1) consists of:

- Oscilloscopes Tektronix 2465B and LeCroy 9354, used to measure the CG output and input analogic signals
- Logic Analysis System Mainframe Hewlett Packard 16500A to read the digital output from AD9201ARS
- Multimeter Hewlett Packard 34401A to measure constant levels, in particular the DC level from the battery for the ADC calibration.

The levels of the control signals are the following:

- CLK, RST and T/H signals for CG:
level logic "high" "1" : 0 V
level logic "low" "0" : - 2.0V

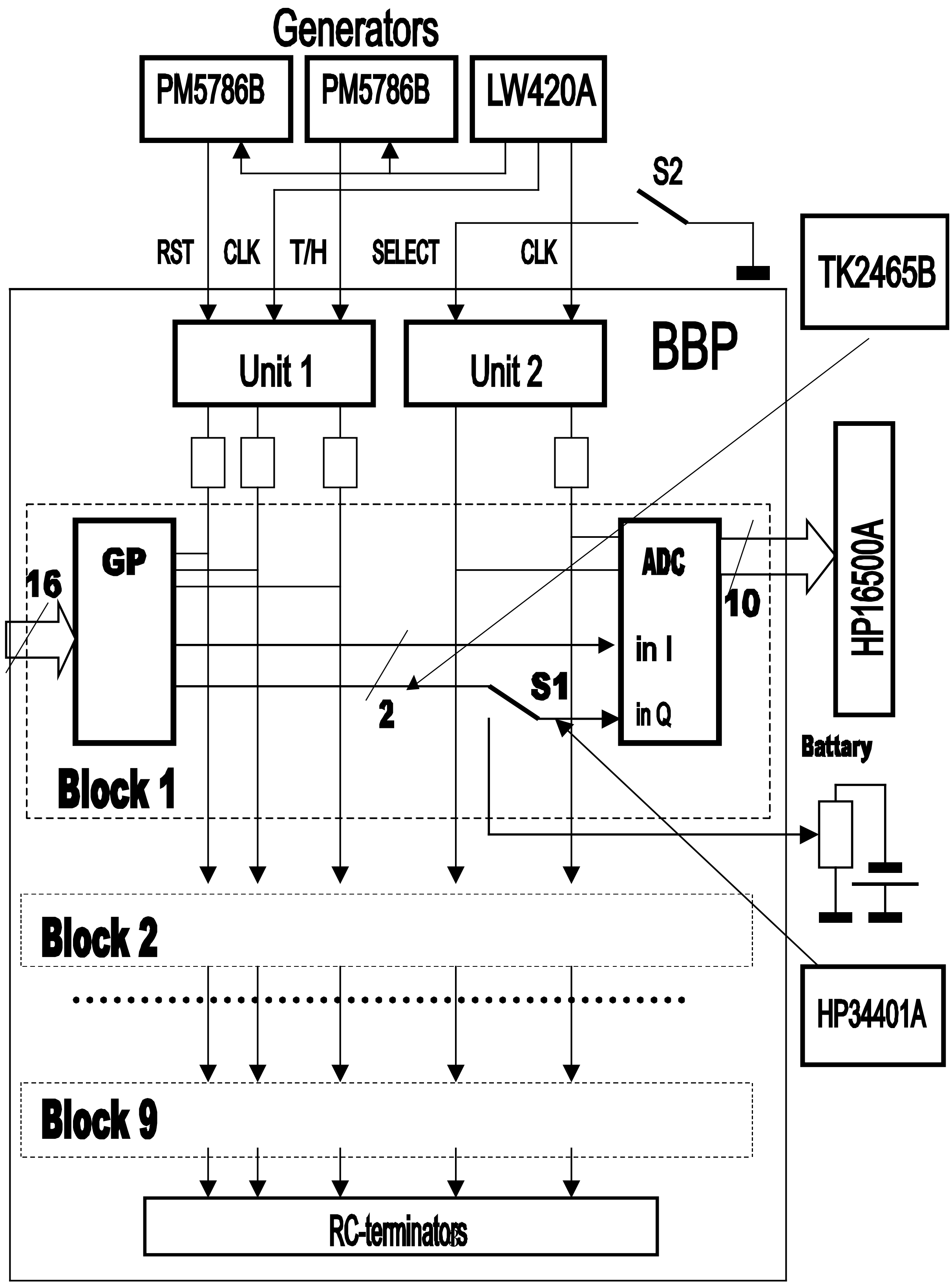

Figure 1: Schematic diagram of the BBP and main equipment used for the tests.

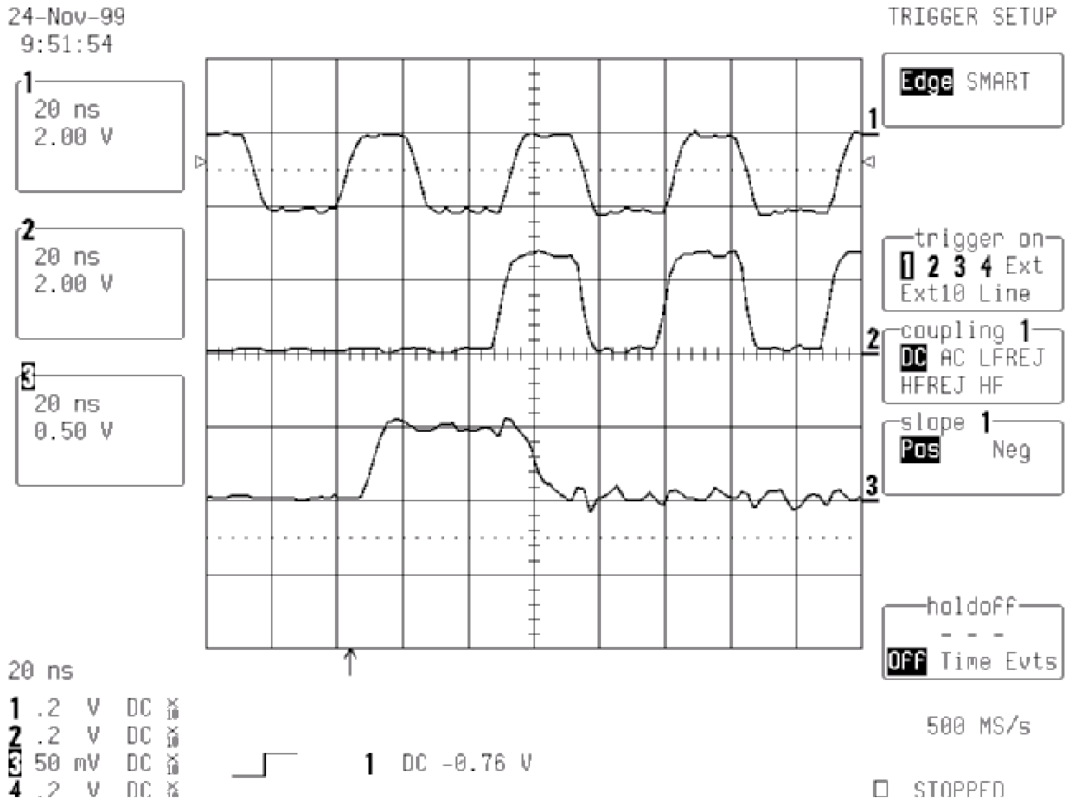

Figure 2: Timing diagram and control signals levels for the CG and the ADC; channel 1: CG CLK, channel 2: ADC CLK, channel 3: CG output 2 (charge is injected in the CG input channel 9, corresponding to output 2, channel 1).

- CLK and Select signals for AD9201ARS:
  level logic "high" "1" : + 2.4V
  level logic "low" "0" : 0V.

3 The noise level on the BBP

3.1 Sources of noise on the BBP

There are different sources of the noise on the BBP; the main ones are:

- noise from the ADC operation mode
- noise from the CG and ADC control signals.

As a first step, the various sources of noise have been studied and minimised.

3.2 The noise due to the control signals

The noise introduced by control signals (to the CG: T/H, CLK and RST; to the ADC: CLK and Select) depends on the non correct matching of these signals that can produce reflections and oscillations. To remove this kind of the noise, we have introduced rejection filters; in particular, the two units (fig. 1) that provide logical signal to the CG and the ADC can be described as follows:

- unit 1 for the CG (the non standard level required for the control signals to the CG is taken into account); unit 1 is a level shifter from TTL low voltage to CG levels; the use of a Schmidt trigger chip (74LCX14 by Fairchild) removes the mismatching effect due to the load. In fig. 3, the shape of the CLK signals at CG input is shown, before and after signal matching.
- unit 2 (PCEL driver - receiver) for the ADC; unit 2 is build with chips SY100ELT22 and SY100ELT23 by SYNERGY. The waveform of CLK for the ADC before and after matching the signals is shown in fig. 4.

3.3 Direct measurement of the CG noise level

Using the oscilloscope Tektronix 2465B we measured the the CG output noise (after removing the oscillations and reflections due to the control signals). The observed noise level is less than 3 mV ptp (see, for example, fig. 5); please note that part of the noise observed at the oscilloscope is due to the oscilloscope sensor.

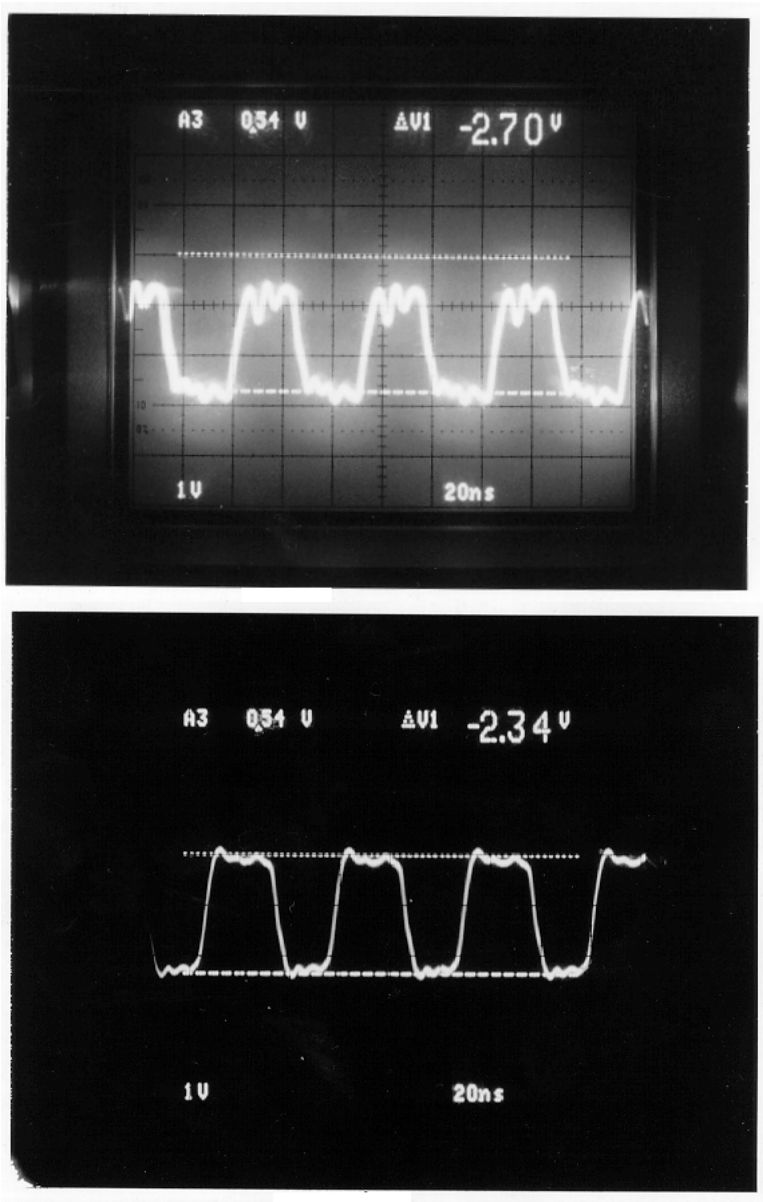

Figure 3: Shape of the CLK signals at CG input, before and after signal matching.

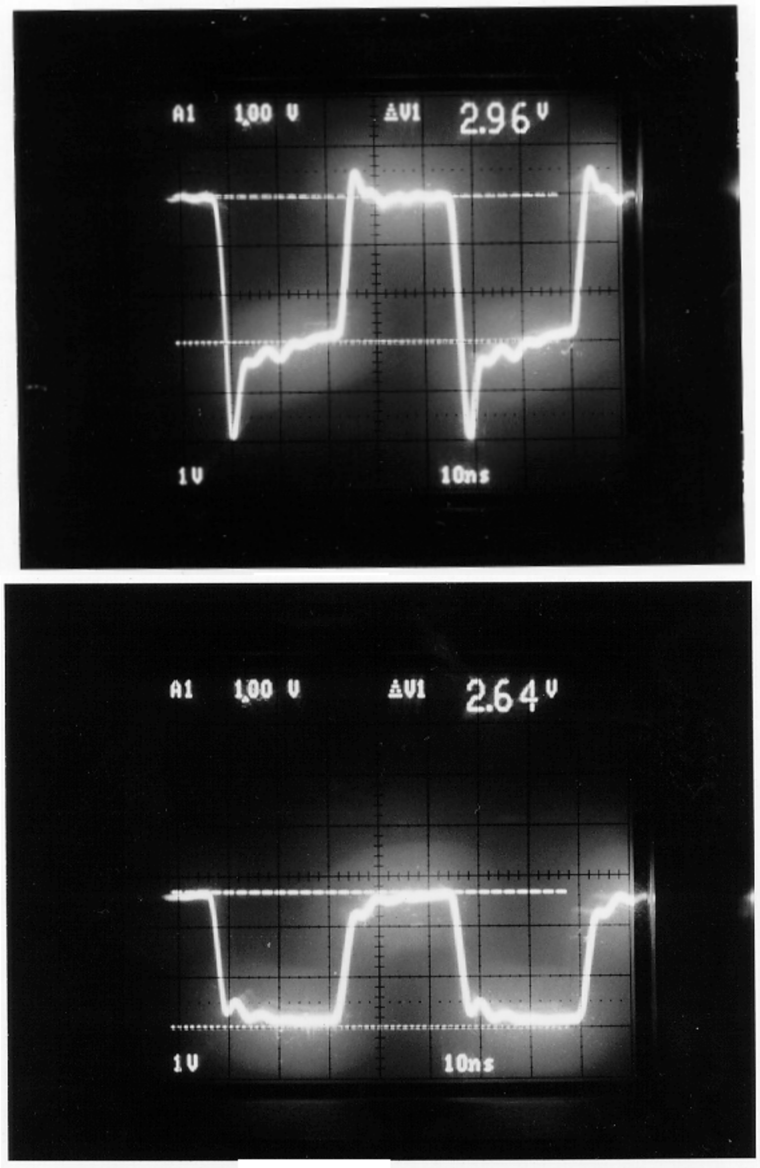

Figure 4: Shape of the CLK signals at ADC input, before and after signal matching.

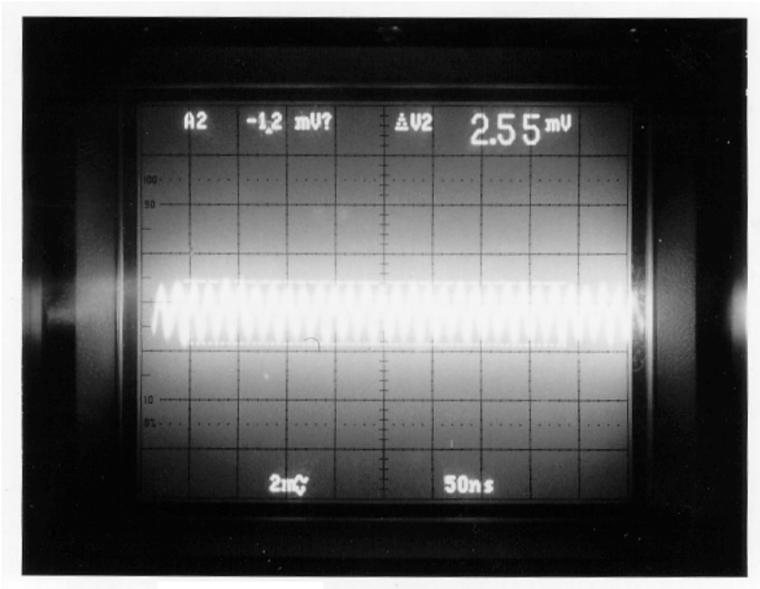

Figure 5: CG, output 2, channel 1: baseline observed at the oscilloscope; no CLK, no T/H signals are used.

4 Calibration of the ADC

4.1 Measurement of the ADC effective noise

A constant voltage level from a battery is applied at the input of AD9201ARS through the resistance divider, acting on switching S1 (fig. 1) to measure the intrinsic effective noise due to the ADC response. In spite the ADC specifications state that a single reference decoupling filter is enought for both ADC input channels, we could verify that this is not the case: in fig. 6, the distribution of the ADC output is shown, as obtained when using one filter or two filters: the use of two filters is necessary. As we can see in fig. 7, the intrinsic effective noise due to the ADC is, after introducing the second filter, less then one bit.

4.2 Calibration of ADC AD9201ARS

Using a constant voltage level from the battery, we have obtained the dependence of the output signal from the input voltage in the range 0 - 1.5 V (fig. 8). The line is the best fit of the measured points above 400 mV. In fig. 9, the deviation from linearity (i.e. from the fitted line) is presented.

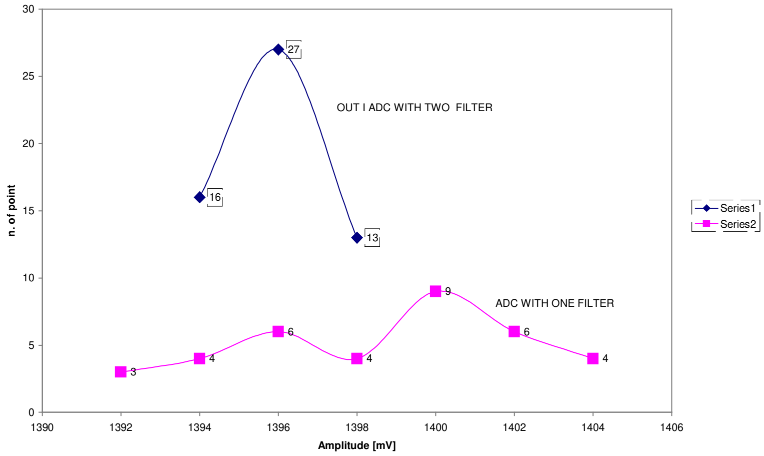

Figure 6: AD9201ARS response for the same DC input voltage using one or two filters (see text); the following conversion function (”ideal” calibration) is used: U = (2000 / 1024) $\times$ A, where A is the ADC response in ADC channels, U is the amplitude in mV.

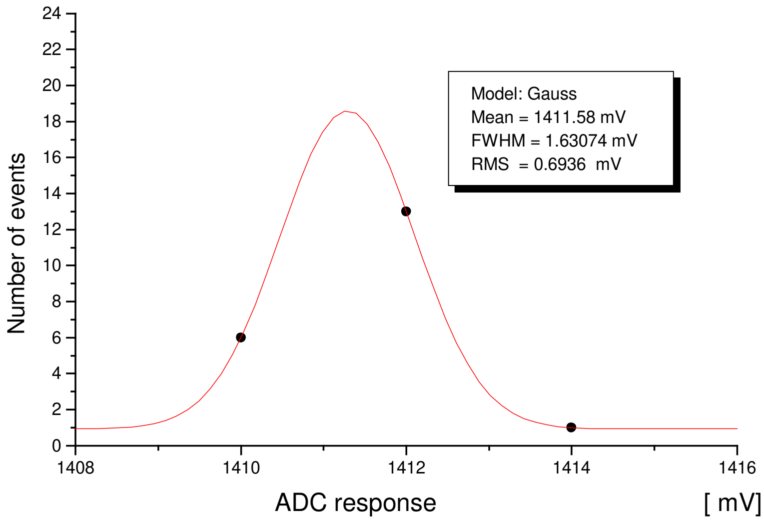

Figure 7: AD9201ARS response for a DC input voltage of 1416 mV; the following conversion function (”ideal” calibration) is used: U = (2000 / 1024) $\times$ A, where A is the ADC response in ADC channels, U is the amplitude in mV.

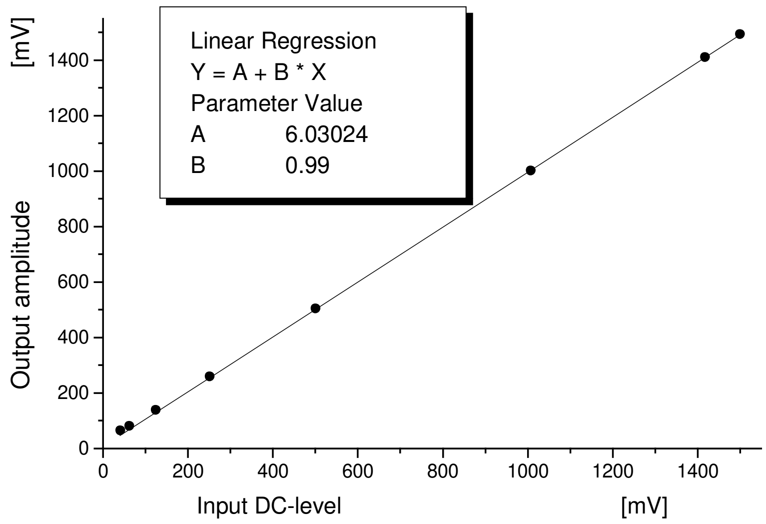

Figure 8: ADC AD9201ARS calibration measurement; the line is the linear fit of the measured points above 400 mV.

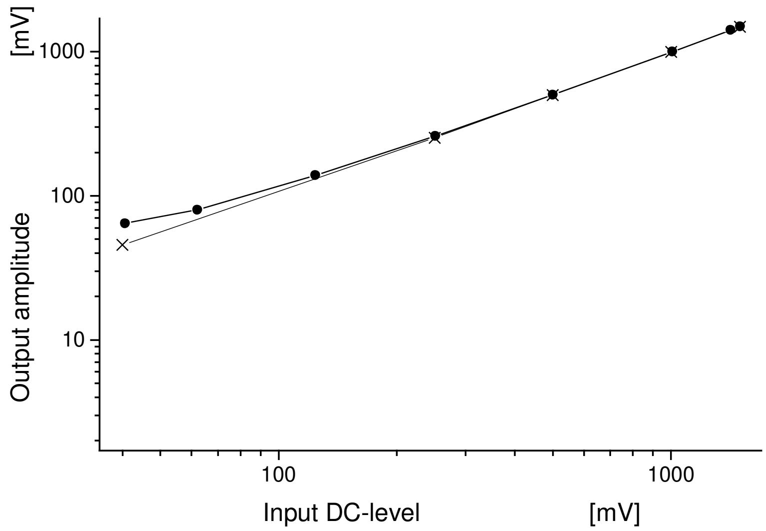

Figure 9: Deviations of ADC AD9201ARS from linearity; the line is the linear fit of the measured points above 400 mV.

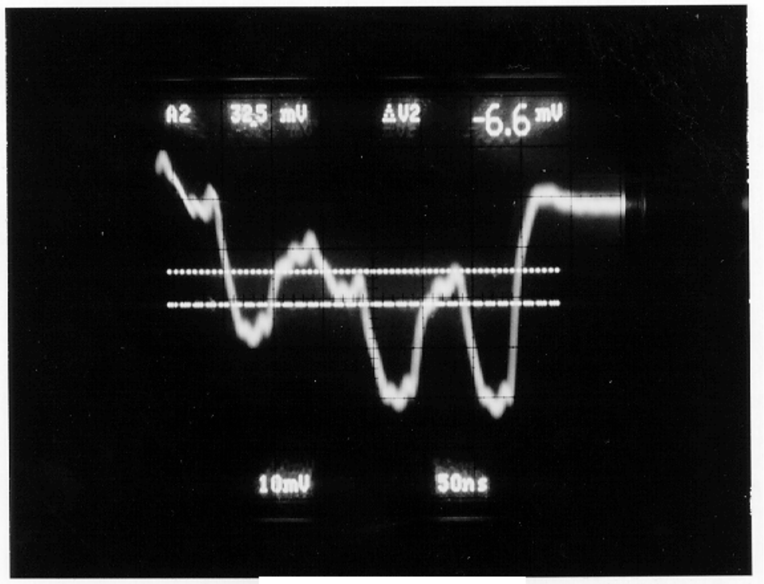

Figure 10: CG output 2, no input charge to any CG channel.

5 COMPASS-GASSIPLEX noise

5.1 Measurement of the GASSIPLEX pedestal (baseline) and noise level

The delay between CG CLK and ADC CLK (see fig.2) has been optimised chosing the delay value that minimise the noise and that allows to read the amplitude in the flat top region in the whole amplifier dynamic range. As shown in fig. 10, each CG channel has a different baseline level (pedestal).

The width (noise) of the distribution of the measured base-line levels has been obtained reading the ADC by the Analyser HP 16500A.

5.1.1 Noise with no input load, no input charge

The distributions of the pedestals for two adjacent channels (channel 1 and channel 2, output2) are shown in fig. 11. The measured fluctuations of the baseline are very small (r.m.s. $\leq$ 0.7 mV) and both pedestal value and noise are very stable in time, as shown in fig. 12.

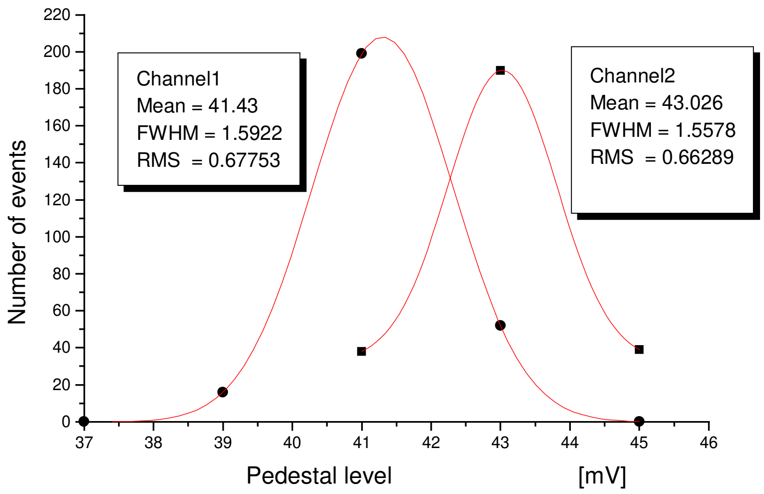

Figure 11: Distributions of the baseline fluctuations for CG, output 2, channels 1 and 2, at 20 MHz CLK frequency.

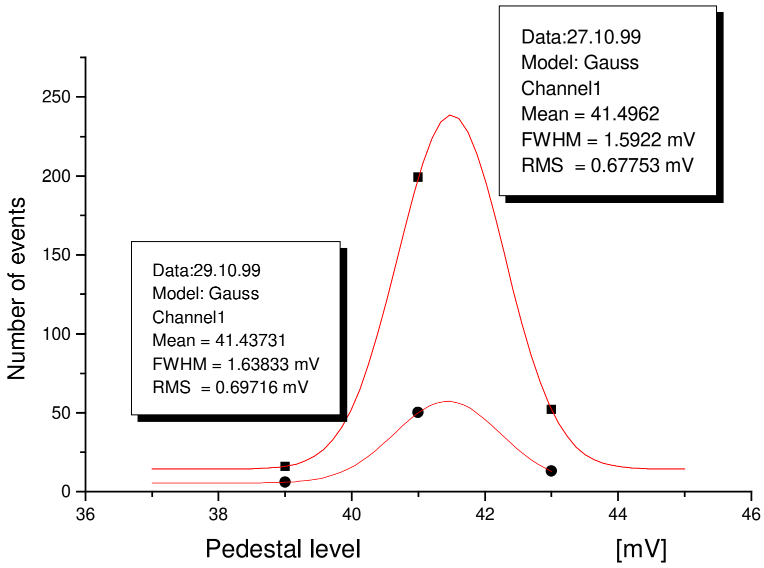

Figure 12: Distribution of the baseline level fluctuations for CG output2, channel 1, measured using ADC9201ARS at 20 MHz CLK frequencies; two different measurements performed on different days are shown.

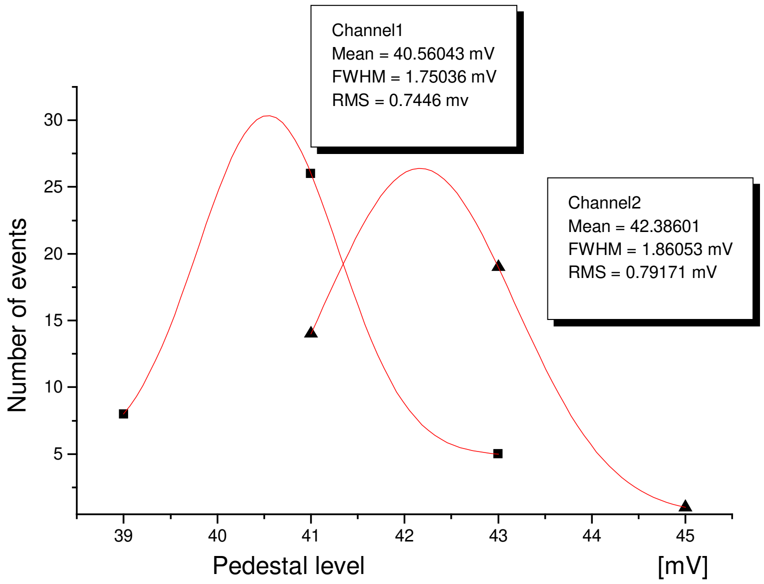

Figure 13: Distributions of the baseline fluctuations for CG, output 2, channels 1 and 2, at 20 MHz CLK frequency; a 10 pF capacitor ia applied between each CG input pin and the ground.

5.1.2 Noise with input capacitive load, no input charge

Figure 13 shows the distributions of the pedestals for the two adjacent channels (channel 1 and channel 2, output2) obtained adding a 10 pF capacitor (C_{in}) between each CG input pin and the ground (for reference, it is estimated that there will be a capacity of about 6 pF between each CG input pin and the ground when the CG chips, mounted on the BORA Board, are used to read the photon detectors): the noise level deterioration is very limited (the noise distribution r.m.s. is ≤ 0.8 mV).

5.1.3 Noise with input charge in adjacent channels

The possible deterioration of the noise level due to large amplitude signals in the preceding channel (according to the read-out order of the CG output multiplexers) has also been investigated. The pedestal distributions have been measured applying different input charges to the input pin of the preceding channel (for more details about injection of input charge, see section 5.2). In fig. 14, measured pedestal distributions for channel 2, output 2 are presented and the corresponding measured output signal amplitudes for channel 1, output 2 are indicated. At very large

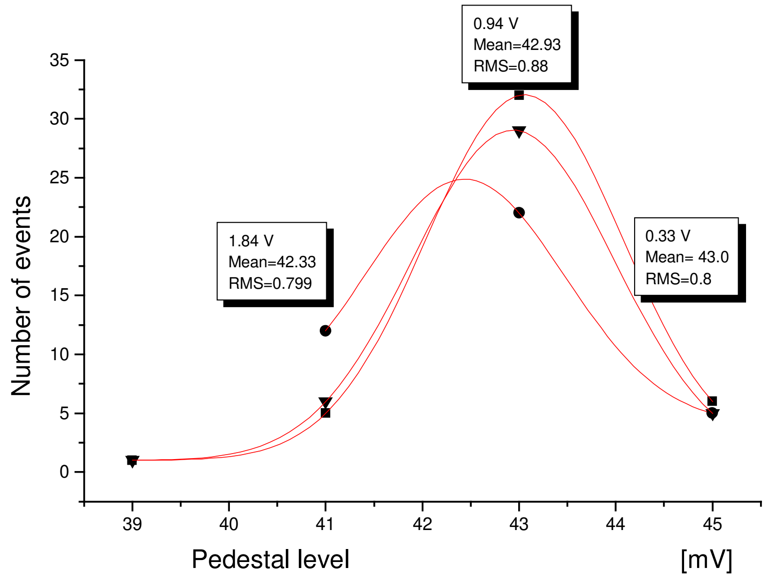

Figure 14: Three measured pedestal distributions, channel 2, output 2 for different input charge in channel 1, output 2; the corresponding measured output signal amplitudes for channel 1, output 2 are also indicated.

amplitudes, the distribution central value is slightly displaced (< 1 mV), while the distribution width remains unchanged.

5.1.4 Noise at high T/H rate

To minimise the experiment dead-time due to the CG read-out, it is necessary that the CG can accept a second T/H a short time after the preceding one. The minimum delay between two consecutive T/H control signals due to the CG architecture is 450 ns. The possible degradation of the noise level at high T/H rate has been investigated. The minimum T/H interval we can set is $\sim$680ns (shorter intervals are not possible due to the limitations of the set-up external to the BBP) and the timing diagram is shown in fig. 15. The distributions of the pedestals for the two channels (channel 1 and channel 2, output 2) are shown in fig. 16; also in this case, the noise level deterioration is very limited (the noise distribution r.m.s. is ≤ 0.9 mV).

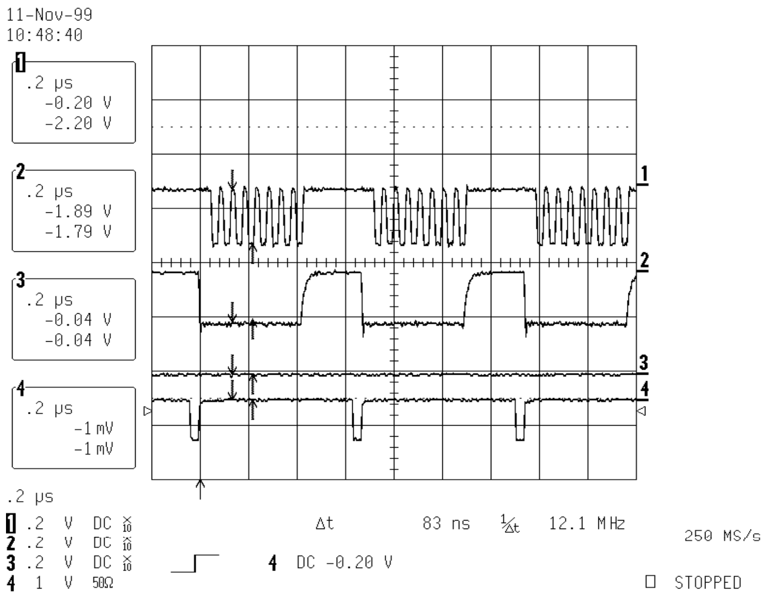

Figure 15: Timing diagram for the measurement at high T/H rate; channel 1: CLK, channel 2: T/H, Channel 4: general clock of the test system.

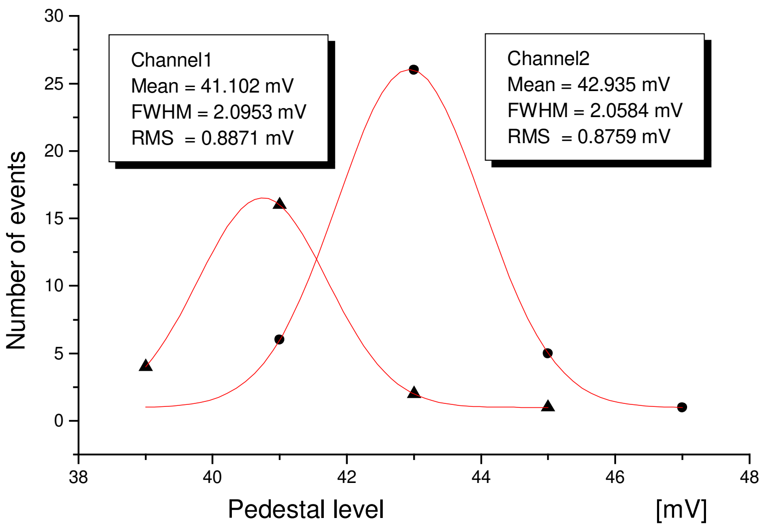

Figure 16: Distributions of the baseline fluctuations for CG, output 2, channels 1 and 2, at high T/H rate: T/H time interval is ∼680 ns.

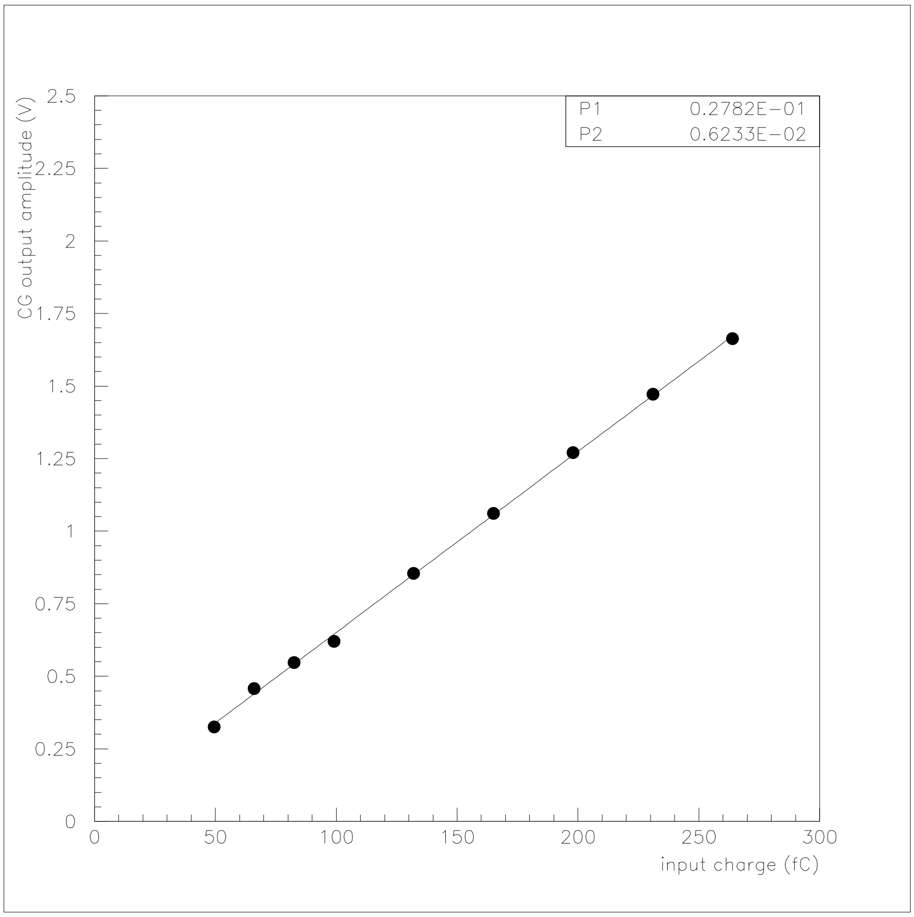

Figure 17: CG calibration.

5.2 Calibration of the GASSIPLEX

A preliminary calibration of the CG has been obtained measuring the output amplitude as a function of the input charge $U_{out} = F\ (Q_{in})$. The input charge is generated charging a capacitor with the rising edge of a logic signal from a pulse generator (the falling edge of the signal is outside the T/H time window). The contribution of the parasitic capacitance is removed. The result is presented in fig. 17. The measured gain is about 6 mV / fC .

6 Conclusions

The CG prototypes are fully functional at the nominal output multiplexer rate (20 MHz). The study of the CG noise level is quite complete: the intrinsic noise level of the prototypes with plastic package is as expected also at the nominal output multiplexer rate and no major degradation has been observed due to

- capacitive input load
- cross-talk from adjacent channels with large input signals
- high T/H rate.

The gain is in the expected range. The present design of the CG is adequate for the read-out of the COMPASS RICH-1 photon detectors.

As a by product of these studies, we have learned more concerning ADC AD9201ARS performances. The BBP has also allowed us to optimised the lay-out for CG and ADC AD9201ARS implementation.