BORA: a Front End Board, with local intelligence, for the RICH Detector of the Compass Collaboration

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Abstract

In this paper we describe the design of the re-configurable front-end boards (BORA boards) for the 82944 channel RICH-1 (Ring Imaging CHerenkov) of the Compass Collaboration (NA58). The front-end electronics controls the sample-and-hold operation after the arrival of an event trigger, acquires the analog voltages from the pre-amp VLSI and converts them into 10 bits at a rate of 20 Ms/s per analog channel. After the analogue values are digitized they are written into FIFOs. A subsequent operation compares the readings of each and every channel with corresponding programmable thresholds, and transmits those values larger than the threshold, together with the channel number, through an optical fiber to subsequent processing stages of the acquisition system.

The overall operation of the board is controlled and supervised by a fast DSP. The availability of local intelligence allows the board to present innovative features such as: to be part of a computer network that connects several similar boards of the detector with a PC. The presence of the DSP allows testing the operability and linearity of the analog channels; and creating engineering frames containing local temperatures and voltages and transmitting the results through the network. The operator can reconfigure the hardware and software of the board by downloading programs from the PC

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1. Introduction

The desired specifications of front-ends for new generation RICHes [1] present many new challenges to the designer. Amongst them: the large number of channels, asynchronous triggering, trigger rates as high as 10^5 events/s and the necessity to filter data locally in order to lower the enormous amount of data generated by large instruments. Also, since the Compass [2] experiment will last for a decade, the front-end must be flexible enough in order to adapt itself to new experimental conditions.

Our front-end board was designed for acquiring, converting, zero-suppressing and transmitting data at 10^5 triggers per second with 5% average pixel occupancy. After zero-suppression the significant data is packed into data frames containing 32 bits per hit channel. Each event frame contains the channel number and reading, plus a header and a trailer word. On the average, each front-end board – called BORA and shown in figure 3- transmits 75.8 Mbit/s through the fiber optics link that connects the board to the rest of the data acquisition system. The whole RICH transmits through its 192 fiber a total of 14.55 Gbit/s, a huge data flow indeed.

For the sake of brevity our description will remain necessarily at the architectural level, leaving for a future publication the details of the implementation.

2. The General Architecture

Figure 1 shows the general physical architecture of the front-end system. There are 192 BORA boards connected to the pixels of the instrument. Each BORA has an on-board 32-bit ADSP-65021L [3] digital signal processor (DSP) that controls and supervises the board. They also have a large XILINX [4] FPGA that acts as: a trigger hold-time controller; a parallel processor that performs several threshold subtractions and comparisons at a time; a fiber optics transmitter controller; and as a generator of control signals for the pre-amp VLSIs, ADC chips and data FIFOs. Since the FPGA is software programmable, at reset time, the chip is programmed through the DSP. Hence the operation of the FPGA is not defined at design-time but can be reprogrammed at run-time. This re-programmability allows adding new features, improving performance or correcting errors of the original implementation.

Each BORA board communicates with the outside world through either a fast fiber optics link, used to transmit event data, or through a dedicated 10 Mbit/s network formed by the 24 DSPs of a chamber and an extra DSP placed within a PC. The whole RICH has eight such dedicated networks, one for each chamber, as shown in figure 1. The ADSP-21065L has been designed to handle the signals for the dedicated time-division-multiplexed network. The network is a two-way communication link that allows the board to receive data and instructions from the controller within the PC and to send status data about the operation of the board. The status information can be engineering data such as voltages and local temperatures or channel operation parameters required for the off-line analysis of the data. The DSP periodically analyzes the operation of the data channel by measuring pedestals, noise, linearity and amplification of each channel.

The PC is connected to the rest of the world through the internet and through it the PC sends and receives data and instructions from the slow control of the whole experiment.

3. The BORA board

The RICH sensitive pixels are 0.8 x 0.8 cm pads on a printed circuit board of 60 x 60 cm. Each pixel is the starting point a one data channel. As shown in fig.1 two PCBs are called a chamber. The PCB implemented back plane is shown in detail in figure 2. A BORA board is connected to the pixels through a row of nine connectors, hence 24 BORAs are needed to process the pixels corresponding to one chamber. Each back-plane connector receives the signal coming from 48 pads.

The heart of the system is the BORA. At reset time the DSP reports to the PC and then it receives, through the dedicated network, the bit stream necessary to program the FPGA as well as the initial operating parameters. Unless commanded to proceed otherwise the system waits for an external trigger to arrive. When the trigger arrives to the BORA the FPGA broadcasts the trigger to the DSP and immediately starts a counter to wait for the 1 μs needed for the output signals of the Compass-Gassiplex [6] to reach their peak. When the signals reach their peak the FPGA holds the values of the signals. Then it proceeds, either automatically or under the command of the DSP, to execute the first data acquisition procedure. This first procedure consists in reading all channel signals from the Gassiplexes, converting then into 10-bit numbers using AD9201 [5] ADCs and writing the digital data -corresponding to three channels at a time- into a 32-bit wide FIFO. Figure 4 shows in detail the schematic of the electronics, corresponding to one of the nine connectors, controlled by the FPGA during the acquisition phase.

There is a second phase where the FPGA is launched into analyzing which readings, already stored in the FIFOs, are above the threshold and consequently must be sent to the rest of the data acquisition system through the fiber optics link. The readings of the analog channels and the analysis are two separated phases because the first phase time duration is always 400 ns, while the duration of the second phase depends on the number of hits above the threshold that need to be transmitted. A second trigger can be accepted if it is separated by more than 400 ns from the previous trigger, while the average analysis of a full event takes approximately 5-7 μs.

The difference in processing time between the two phases forced us to place in between a FIFO capable of buffering 100 events.

4. Conclusion

The front-end system for the Compass experiment at CERN (NA58) is based on 192 BORA boards. These boards have local intelligence due to the inclusion of a DSP capable of re-programming a large FPGA and of controlling and supervising the data acquisition process. The DSP is also capable of performing housekeeping chores such as evaluating pedestals, noise and linearity of the channels. It also controls a local network that communicates all DSPs within a chamber to a PC. The board delivers the data coming from an event through a fast fiber optics link.

The flexibility and performance of this architecture allows it to be a valid implementation capable of lasting for the ten-year life cycle of the experiment.

References

[1] See for example, R. Arnold et al., Nucl. Instrum. Methods A273 (1988) 466.

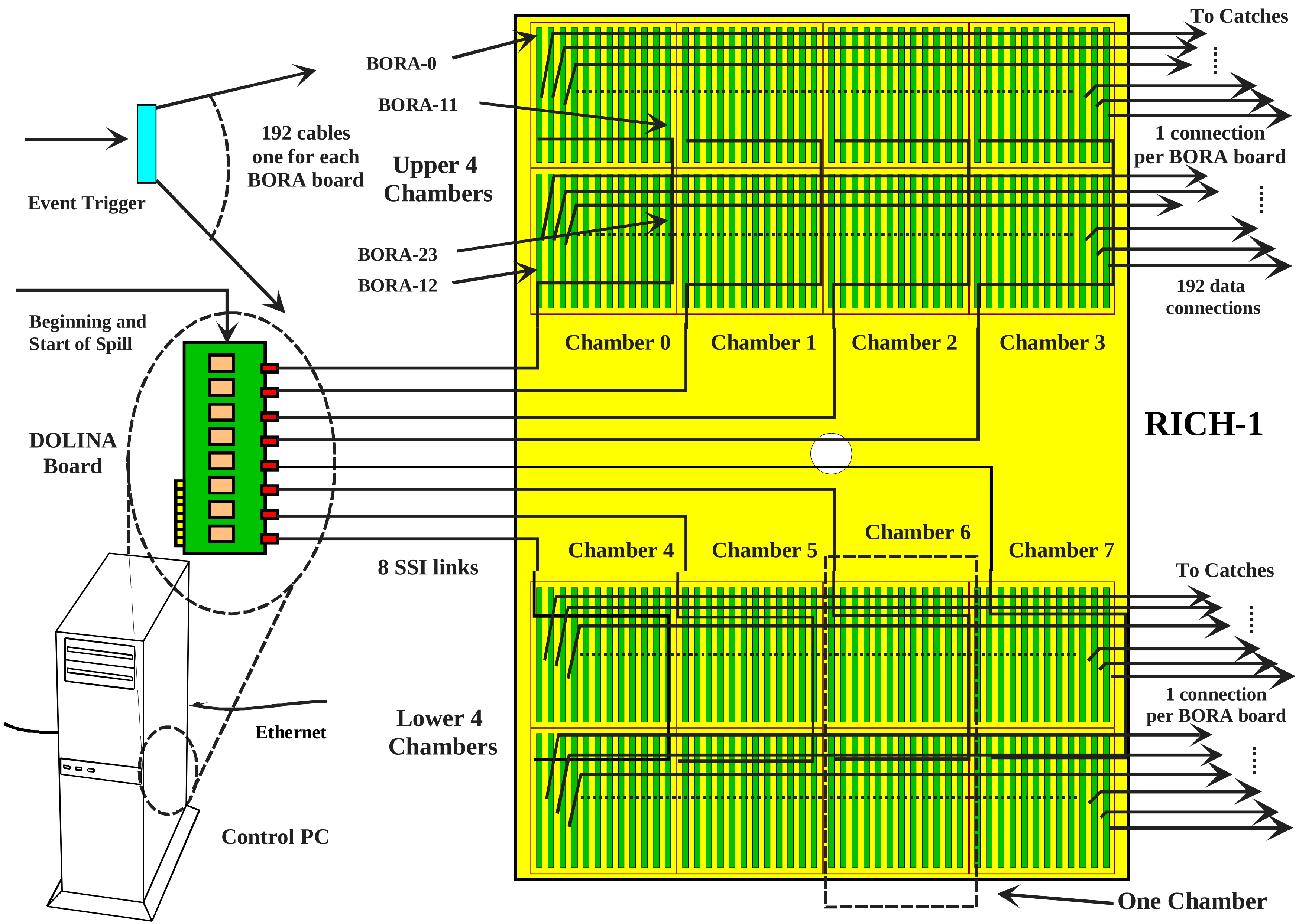
[2] COMPASS Collaboration, *Proposal for a Common Muon-Proton Apparatus for Structure and Spectroscopy*, CERN SPSLC/P297, CERN, March 1996.

[3] ADSP-21000 Family Applications Handbook V.1, Analog Devices, Norwood, MA, USA.

[4] Spartan and Spartan XL Families of Field Programmable Gate Arrays, Xilinx Inc., San Jose, CA, USA.

[5] AD9201, Dual Channel, 20 MHz 10-bit resolution CMOS ADC, Analog Devices, Norwood, MA, USA.

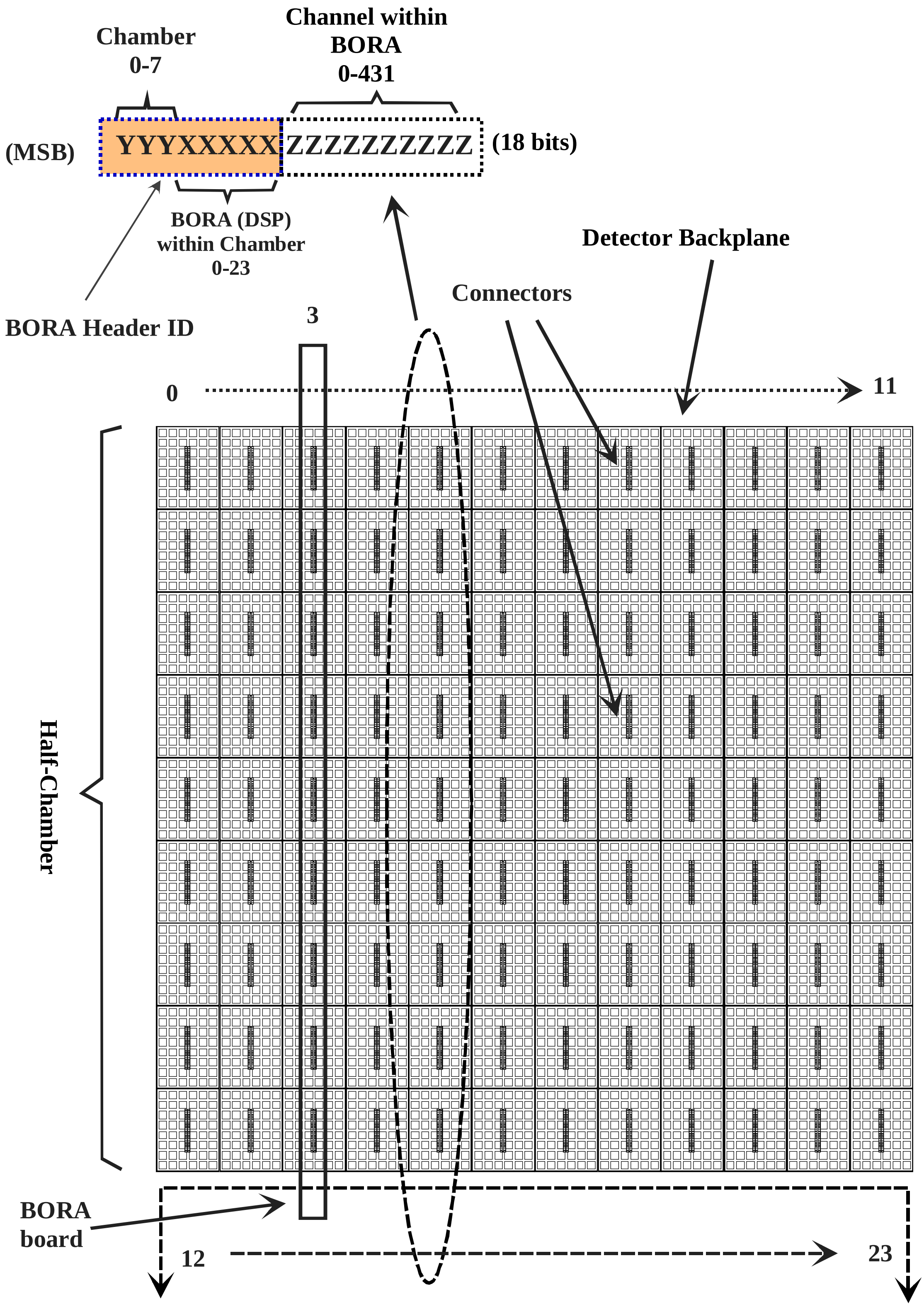
[6] J. C. Santiard et al, *Gasplex: a low noise analog signal Processor for readout of gaseous detectors*, presented at the 6th Pisa Meeting on Advanced Detector, La Biodola, Isola d'Elba, Italy, 22-28 May 1994.



To Catches
BORA-0
BORA-11
192 cables
one for each
BORA board
Upper 4
Chambers
Event Trigger
1 connection
per BORA board
BORA-23
BORA-12
192 data
connections
Beginning and
Start of Spill
Chamber 0
Chamber 1
Chamber 2
Chamber 3
RICH-1
DOLINA
Board
Chamber 4
Chamber 5
Chamber 6
Chamber 7
8 SSI links
To Catches
1 connection
per BORA board
Ethernet
Lower 4
Chambers
Control PC
One Chamber

Figure 1 Caption

The figure shows a top-level view of the front-end data acquisition for the Compass Collaboration RICH. Each of the 192 BORA boards is directly connected through a one-way 240 Mb/s fiber optic link to the rest of the apparatus and through a slower network to other boards and to the controlling PC computer. The fiber optics link transmits event data while the slower network is used for downloading programs to the DSPs and for transmitting engineering data such as voltages and temperatures and channel noise figures needed to recalculate channel thresholds.



Chamber
0-7
Channel within
BORA
0-431
(MSB)
YYYXXXXX
ZZZZZZZZZZ
(18 bits)
BORA (DSP)
within Chamber
0-23
Detector Backplane
Connectors
BORA Header ID
3
0
11
Half-Chamber
BORA
board
12
23

Figure 2 Caption

View of the layout of the back plane printed circuit board of half a chamber. Notice that each BORA board is connected to one row of nine connectors of the back plane. To fully identify a channel we need three bits for the chamber number; five bits for the BORA board number within the chamber and ten bits for the channel within the BORA controlled row.

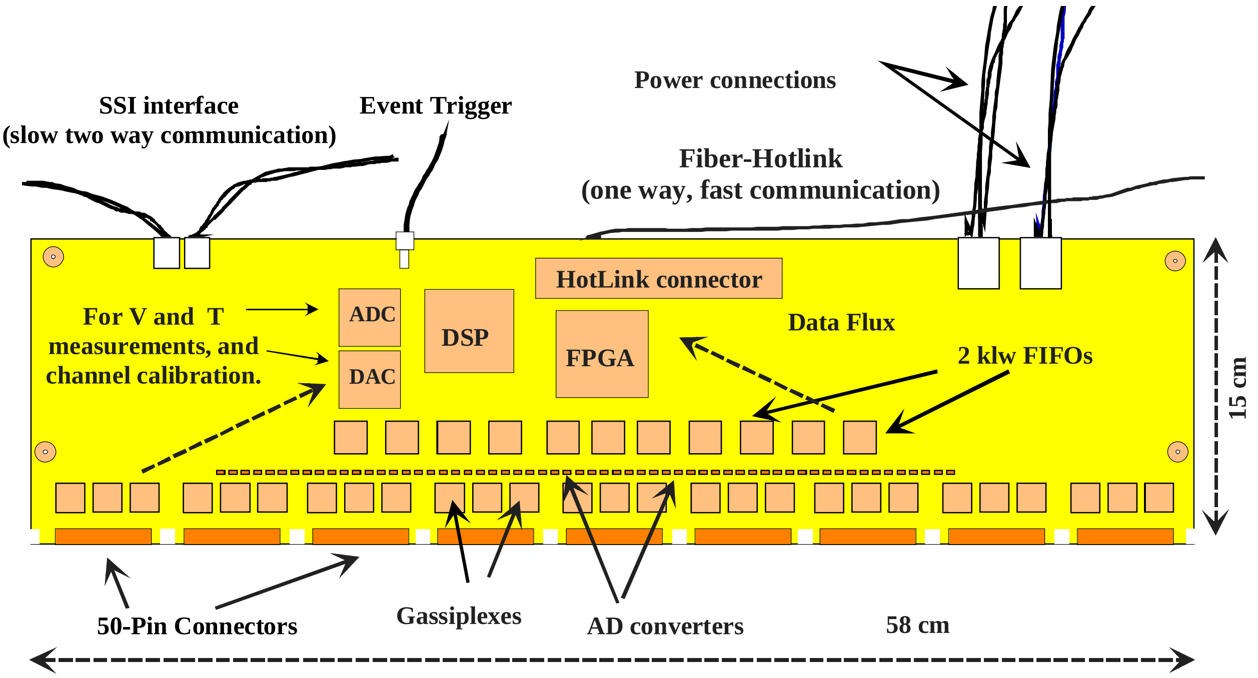

SSI interface
(slow two way communication)
Event Trigger
Power connections
Fiber-Hotlink
(one way, fast communication)
HotLink connector
For V and T
measurements, and
channel calibration.
ADC
DAC
DSP
FPGA
Data Flux
2 klw FIFOs
15 cm
50-Pin Connectors
Gassiplexes
AD converters
58 cm

Figure 3 Caption

The figure shows a schematic view of a BORA front-end board. The board has one Field Programmable Gate Array, a ADSP-21065L digital signal processor. The board communicates with the rest of the system through a fast fiber optics link and dedicated time division network.

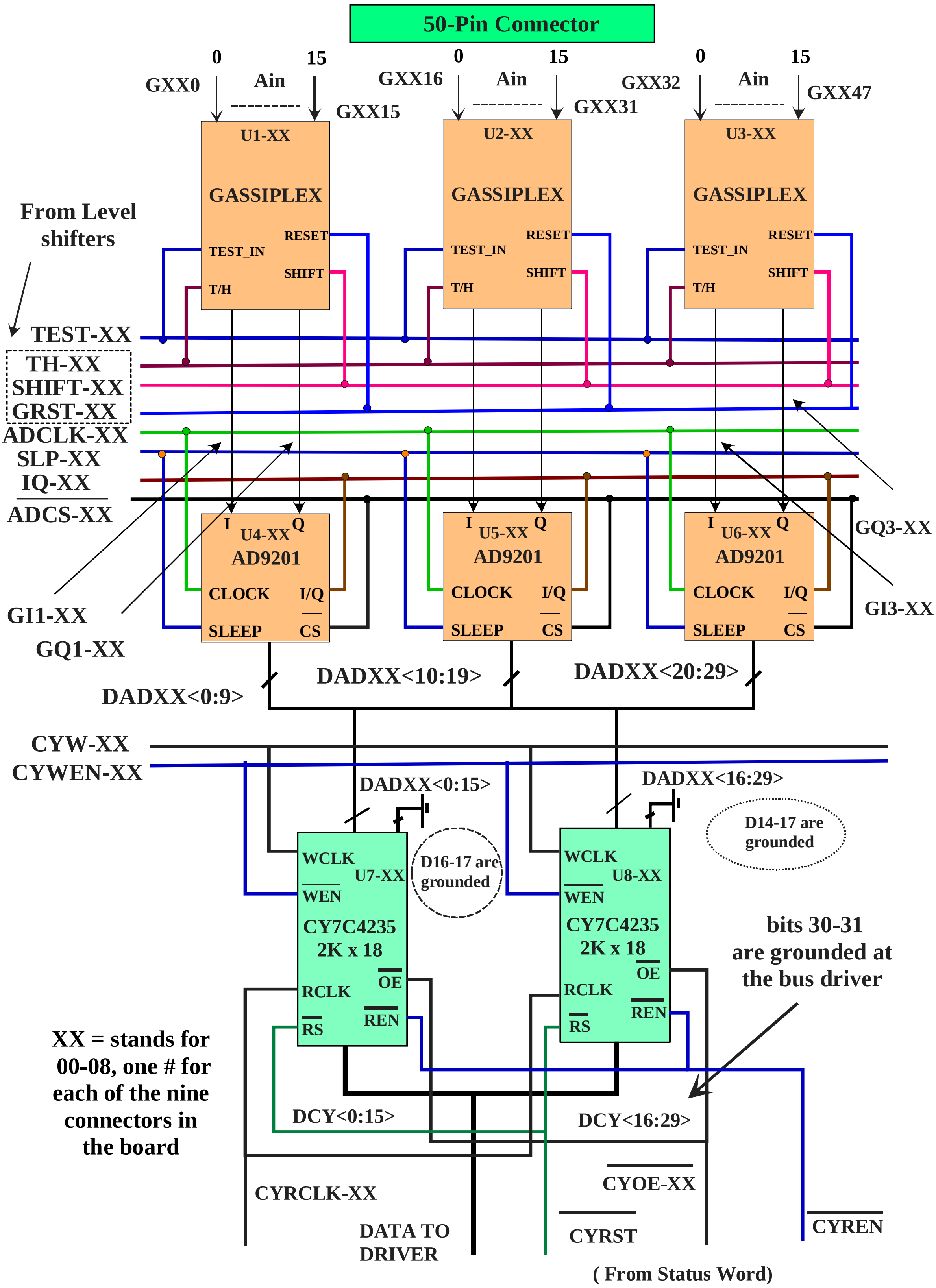

50-Pin Connector
0
15
Ain
GXX0
GXX15
GXX16
GXX31
GXX32
GXX47
U1-XX
U2-XX
U3-XX
GASSIPLEX
RESET
TEST_IN
SHIFT
T/H
From Level shifters
TEST-XX
TH-XX
SHIFT-XX
GRST-XX
ADCLK-XX
SLP-XX
IQ-XX
ADCS-XX
I
Q
U4-XX
U5-XX
U6-XX
AD9201
CLOCK
I/Q
SLEEP
CS
GI1-XX
GQ1-XX
GQ3-XX
GI3-XX
DADXX<0:9>
DADXX<10:19>
DADXX<20:29>
CYW-XX
CYWEN-XX
DADXX<0:15>
DADXX<16:29>
D16-17 are grounded
D14-17 are grounded
WCLK
U7-XX
U8-XX
WEN
CY7C4235
2K x 18
OE
RCLK
REN
RS
bits 30-31 are grounded at the bus driver
XX = stands for 00-08, one # for each of the nine connectors in the board
DCY<0:15>
DCY<16:29>
CYOE-XX
CYRCLK-XX
DATA TO DRIVER
CYRST
CYREN
(From Status Word)

Figure 4 Caption

The figure shows in detail the electronics controlled by the FPGA during the phase of analog data acquisition. The Gassiplex chips read 16 analog pixel inputs. The deliver the analog signals through two outputs at a time. These analog outputs are converted into 10-bit digital numbers by the AD9201 ADCs. The digital values are packed, in groups of the 10-bit readings, into the 32-bit wide FIFOs.