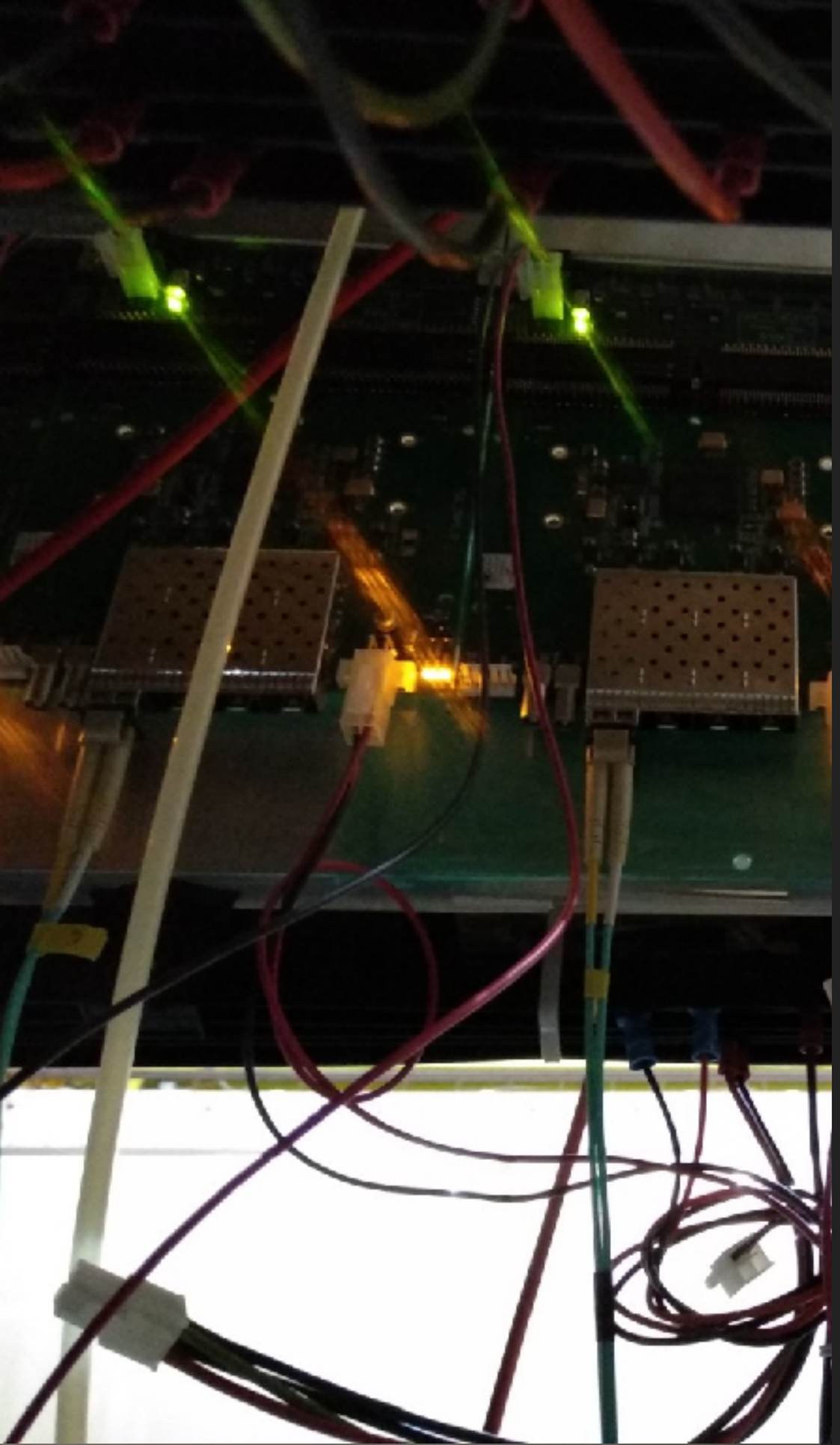

# MWPC

# TEST OF THE NEW FE

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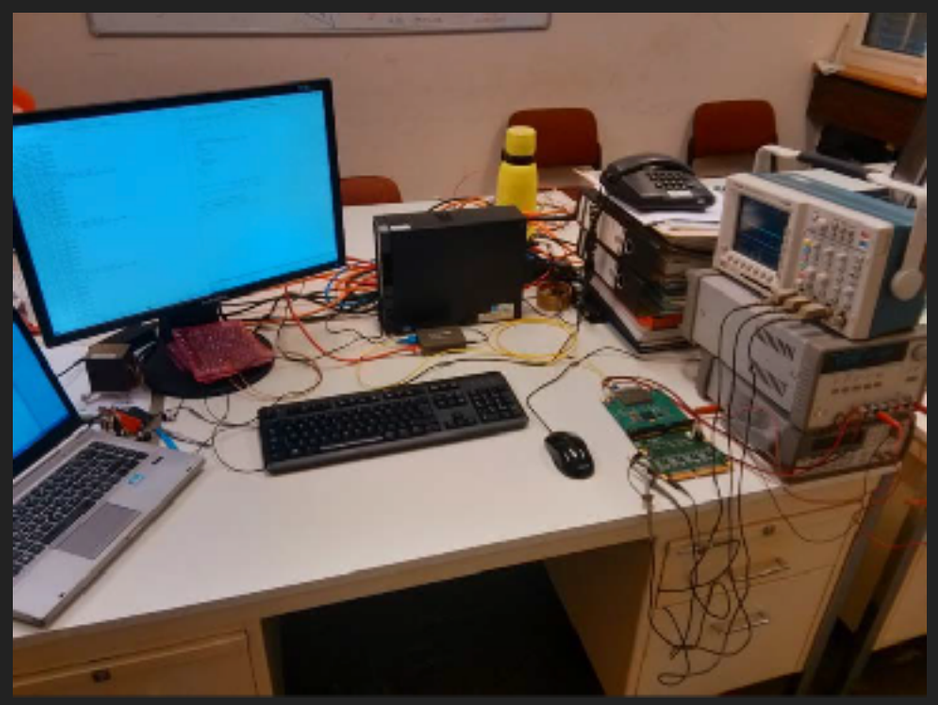
WEEKLY MEETING, CERN, 9 NOV 2018

# THE NEW FE

- built around an FPGA based TDC and CMAD ASICs
- the main advantages are the change of the RO scheme to optical and the use of proven production ready components
- we expect that this solution would solve the main problems present in the current FEs
- we have made a first “on beam” test during the last 5 hours of the 2017 running
- the first test has shown a complete integration into the COMPASS DAQ but failed to provide useful data due to an error in the threshold programming software
- the error was since then identified, corrected and the operation was extensively tested in lab condition

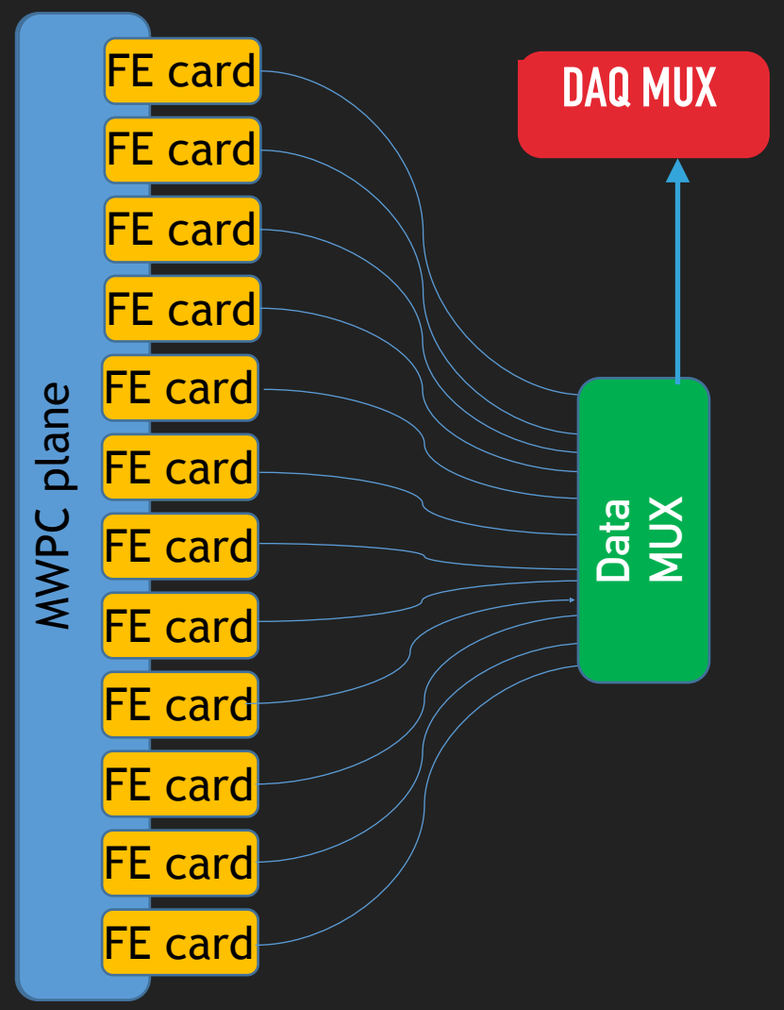


# FE TEST BEAM: SET UP AND TIMELINE

- we would substitute 4 standard triplets by 12 new FEs on PA05X
  On Wed 7 Nov: 3-5 hours for power cabling and fibers installation

- We will use the FPGA based TDC boards developed and produced in Munich coupled to the CMAD based analog FE cards developed in Torino and successfully tested on MWPCs in 2012 (with F1 boards - see the other slides)

- Optical Read-out: we will use 12 direct fibers to the Data MUX; one single fibre to the DAQ



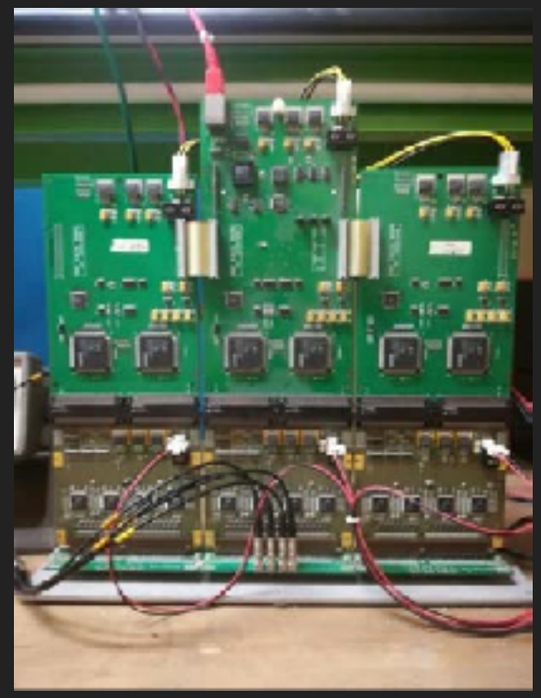

- All the CMAD boards (10 already existent + 6 newly produced) have been tested and calibrated in Torino Lab

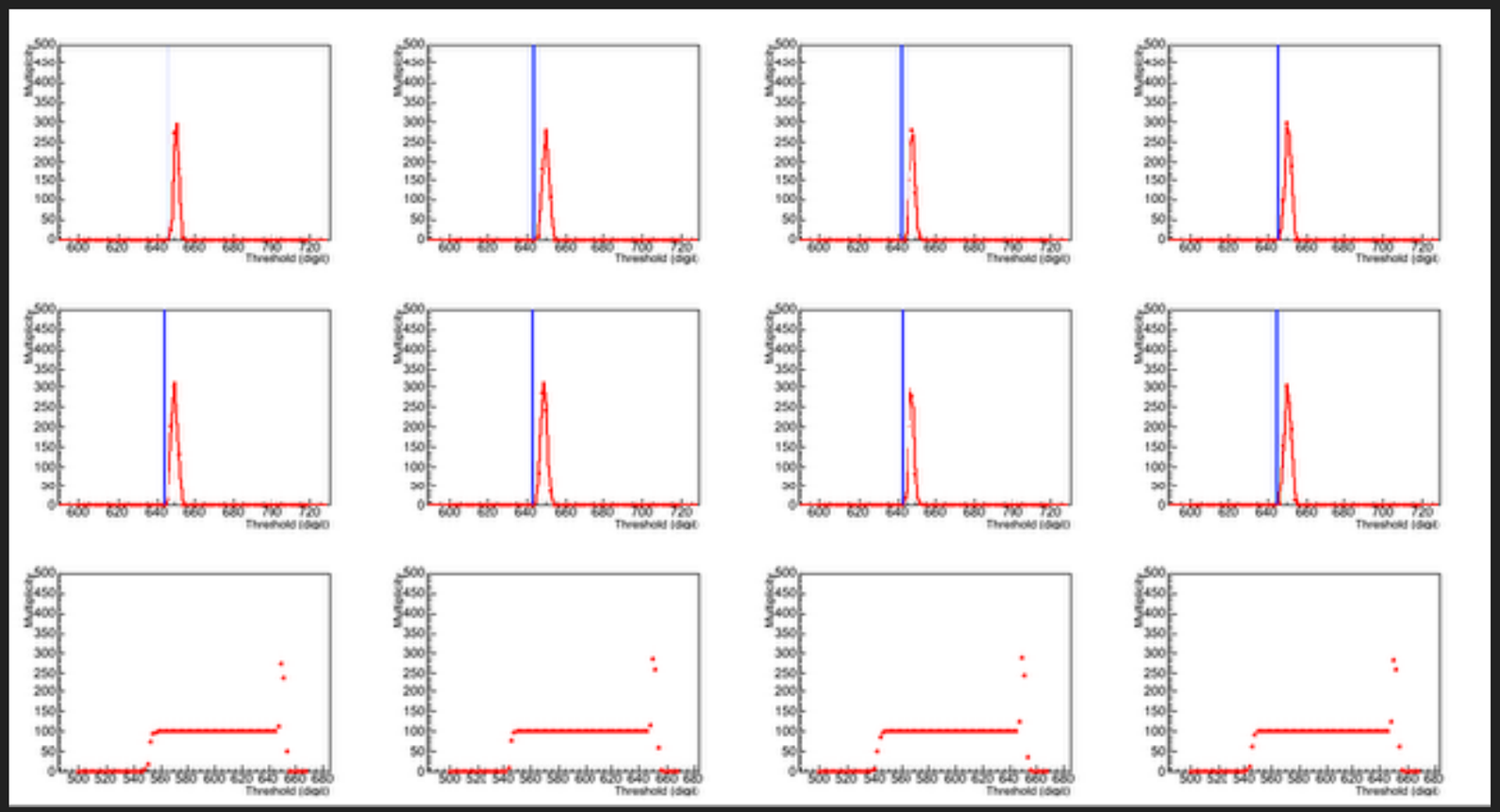
- CMAD + FPGA-TDC: CMAD programming performed and tested in Torino Lab

- CMAD + FPGA-TDC: final test-setup installed in the DAQ barrack at 888; CMAD programming performed and tested; DAQ tested

# FE TEST BEAM: CMAD CARDS CALIBRATION AND TEST

- Threshold scan performed on all 16 boards (1024 channels) for noise threshold setting and baseline equalisation
- 16 calibration files, one per board, have been produced for baseline setting
- Boards response to an injected external test pulse has also been tested
- Torino Lab test setup based on F1 boards read-out

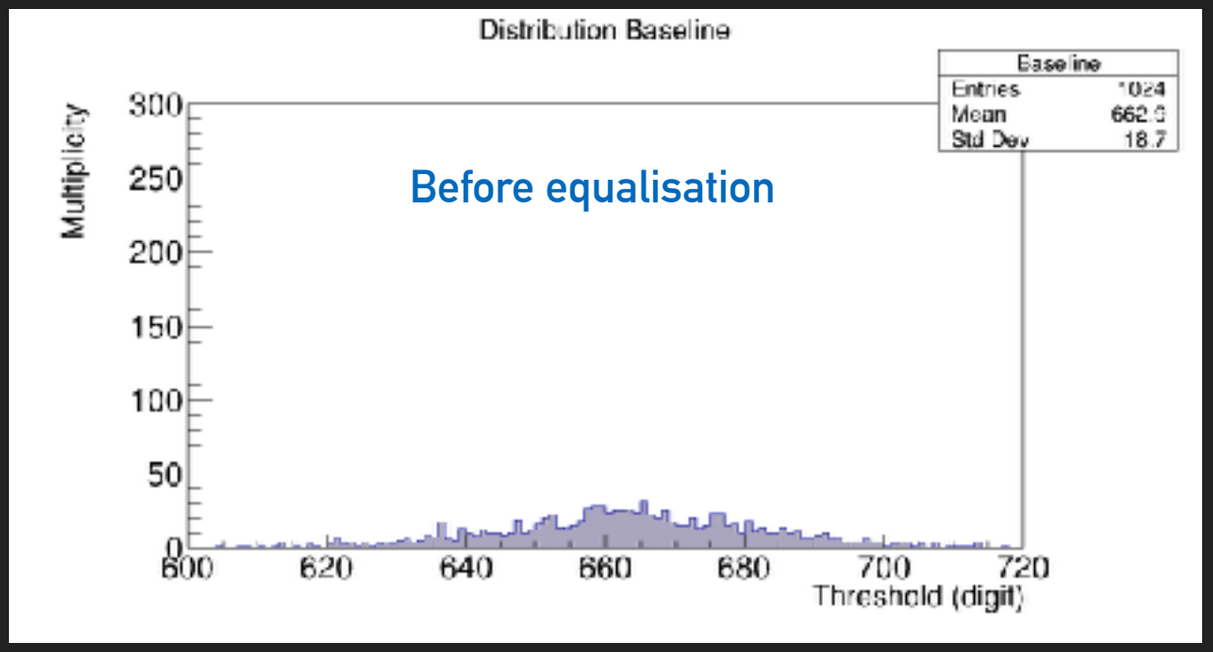


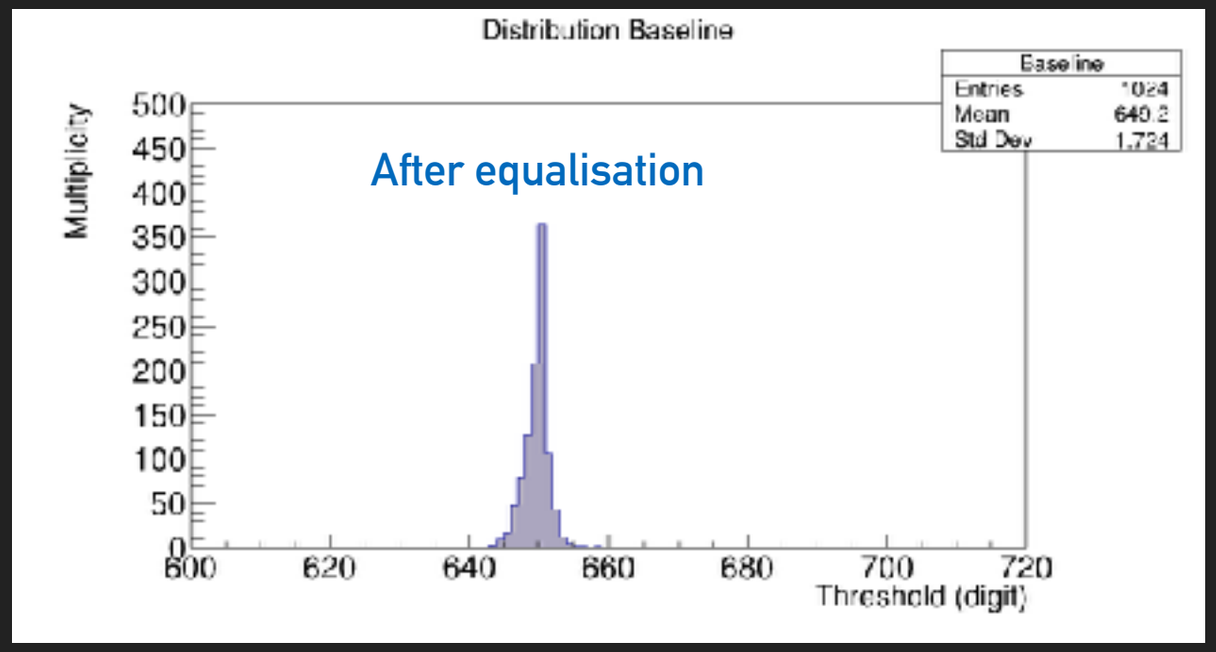


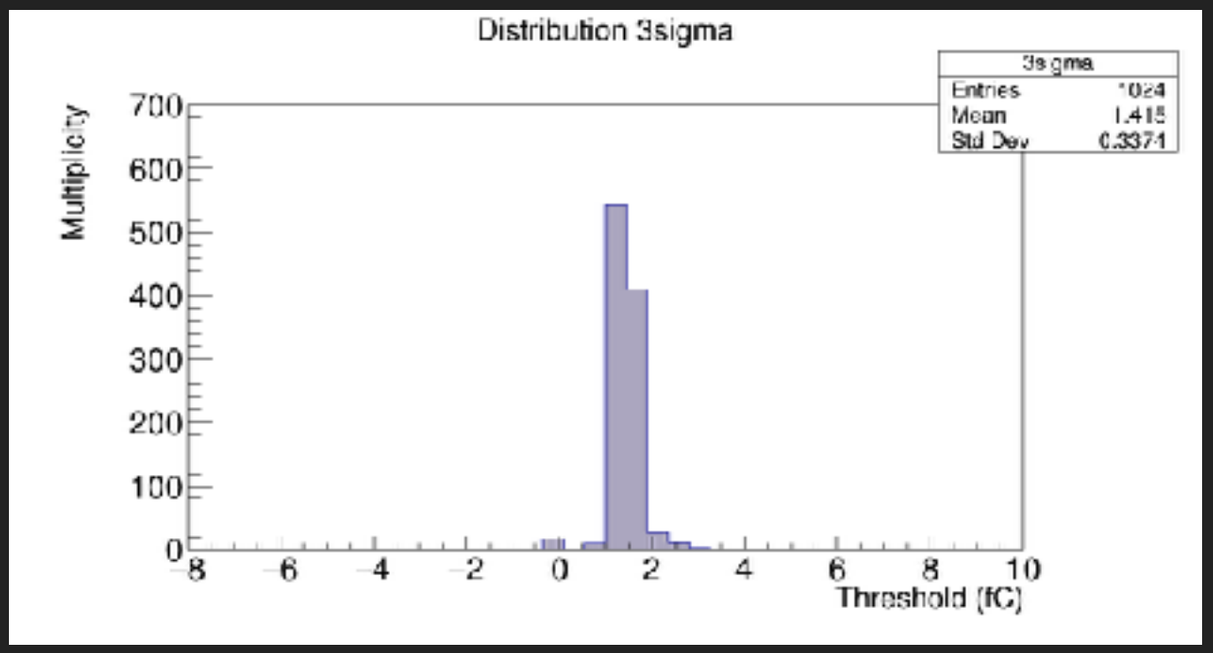
Noise Threshold Scan

Threshold Scan with Ext pulse

# FE TEST BEAM: CMAD CARDS CALIBRATION AND TEST



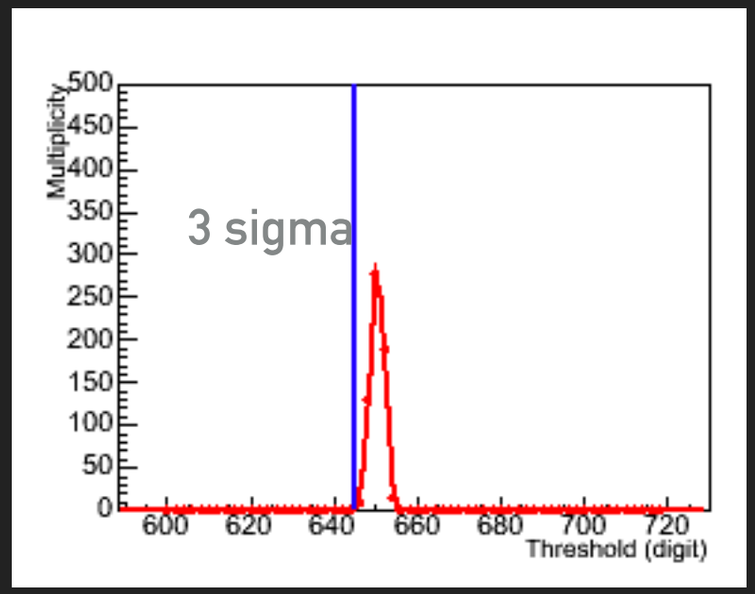




Noise value:
3 sigma of the gaussian distribution

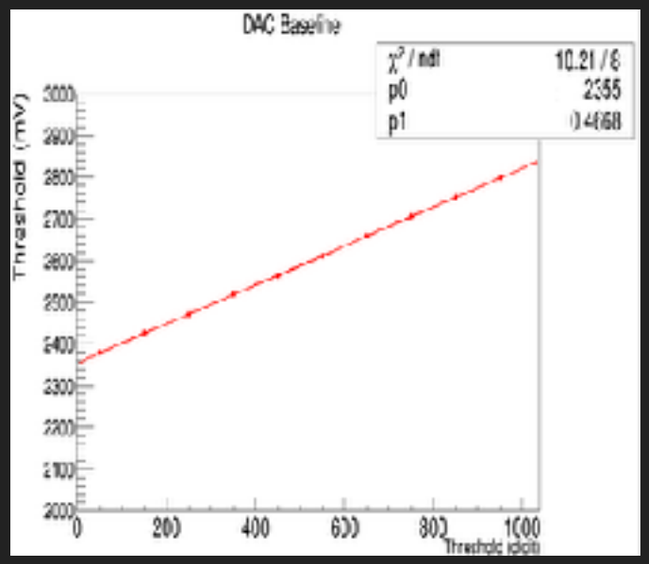
Conversion from dig to fC:

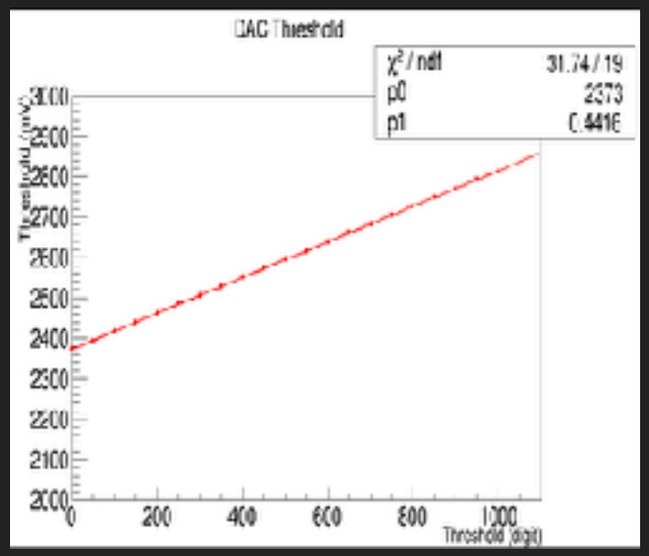
1dig = 0.4 fC with a gain of 1.2 mV/dig

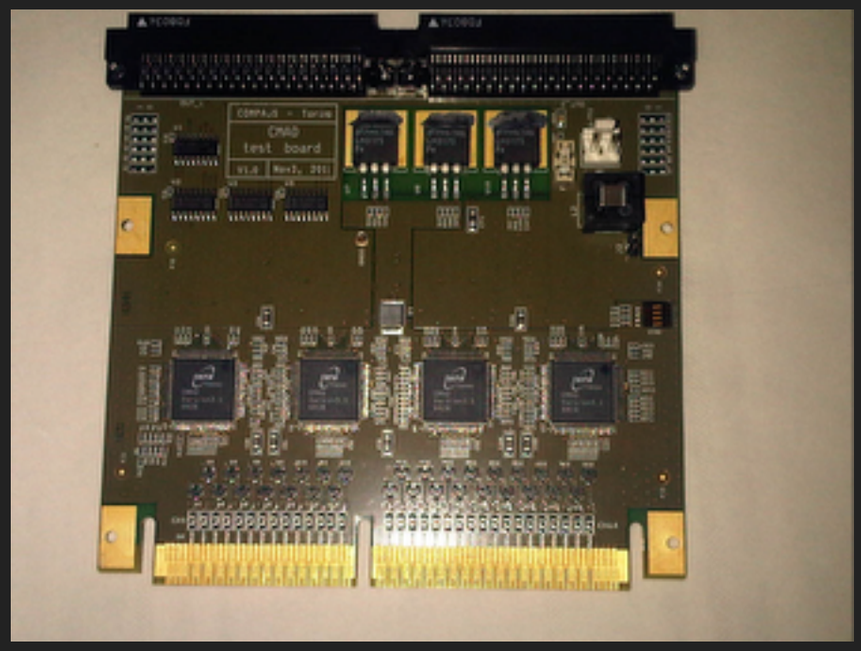


# FE TEST BEAM: CMAD CARDS PROGRAMMING

- The correct programming of the CMAD DACs (for thresholds and baseline) through the TDC FPGA has been tested measuring the set thresholds and baseline voltages on the CMAD card test-pads
- The calibration files are correctly loaded
- No DAQ system for TDC FPGA was yet available for Torino Lab test



# FE TEST BEAM: CMAD+FPGA-TDC TEST AT 888

➢ final test-setup installed last week in the DAQ barrack
➢ CMAD boards programming tested
➢ The new FE included in DAQ and tested

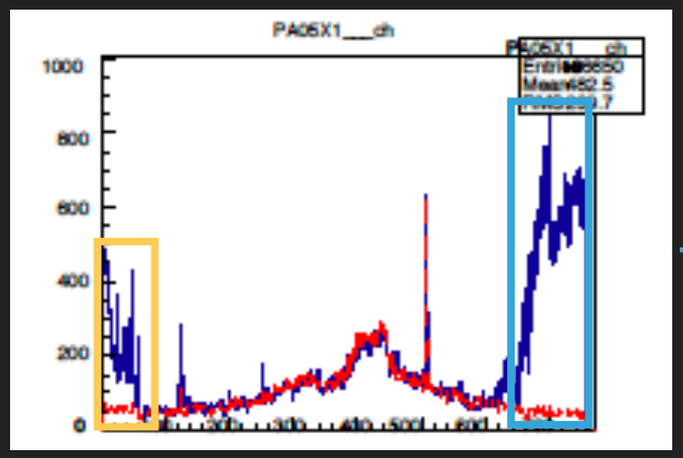
## Installation in the COMPASS hall (Wednesday 7 Nov, MD)

➢ All the 4 triplets on PA05X (bottom side) have been replaced with 12 new boards

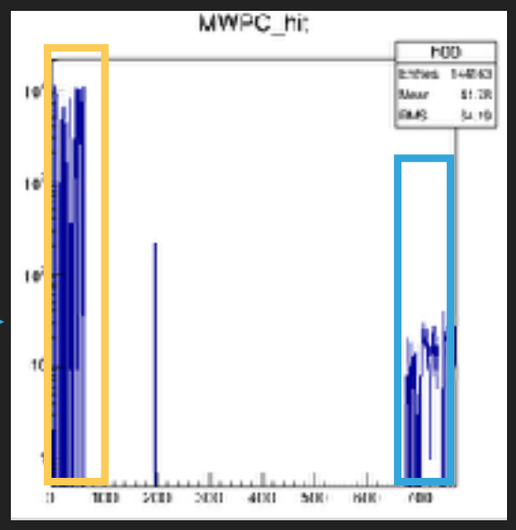
➢ DAQ MUX installed in available slot in richwall mux crate and the fibres were connected

➢ We performed a threshold scan to check the noise level in the Experimental environment
—> Thr set to 4fC on all the channels except for the noisy channels of the plane which have been later excluded

PA05X bookies - Mon 5 Nov



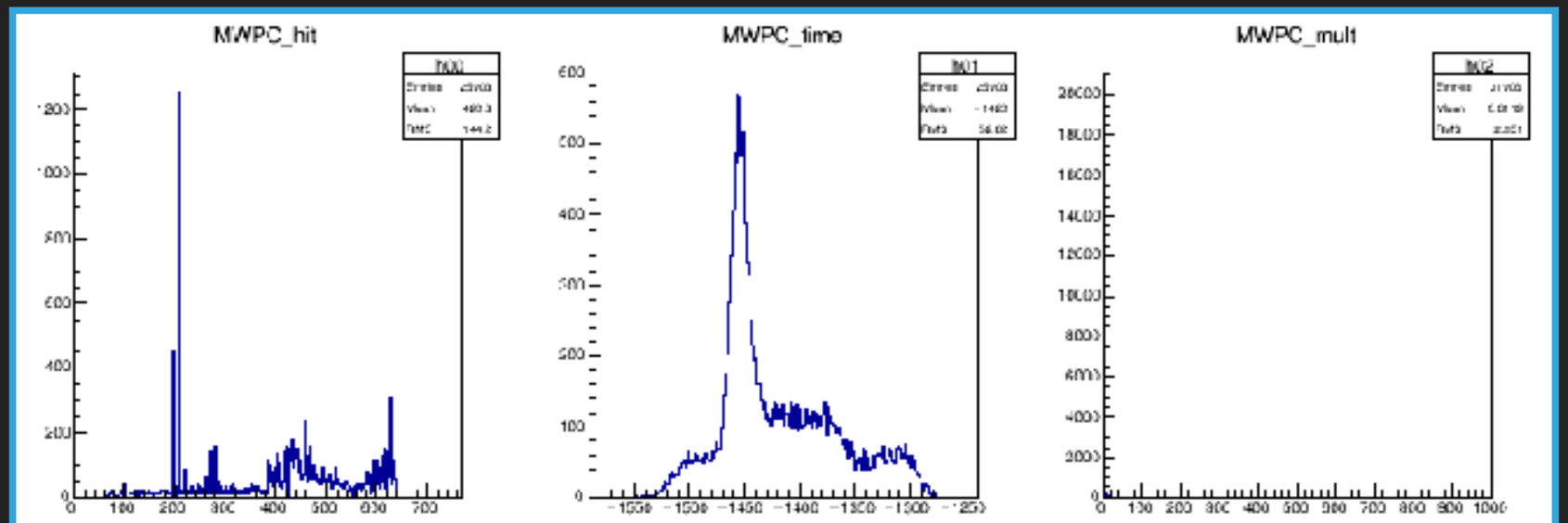

New FE - 4fC threshold

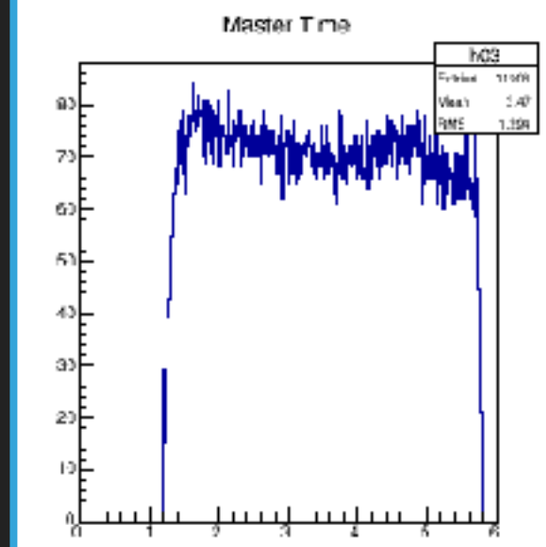


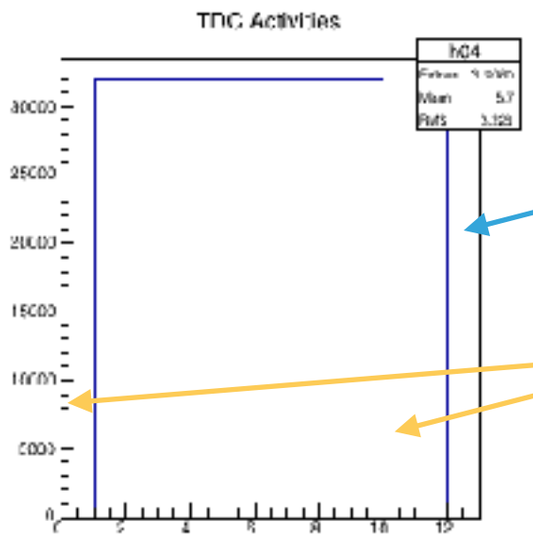

# FE TEST BEAM: CMAD+FPGA-TDC TEST AT 888

## Test with beam (7 Nov)

➢ Latency scan performed to find the signal peak with beam: Latency set to about 3 microseconds, Time window set to about 240 nanoseconds




**Master time: mux port 12**

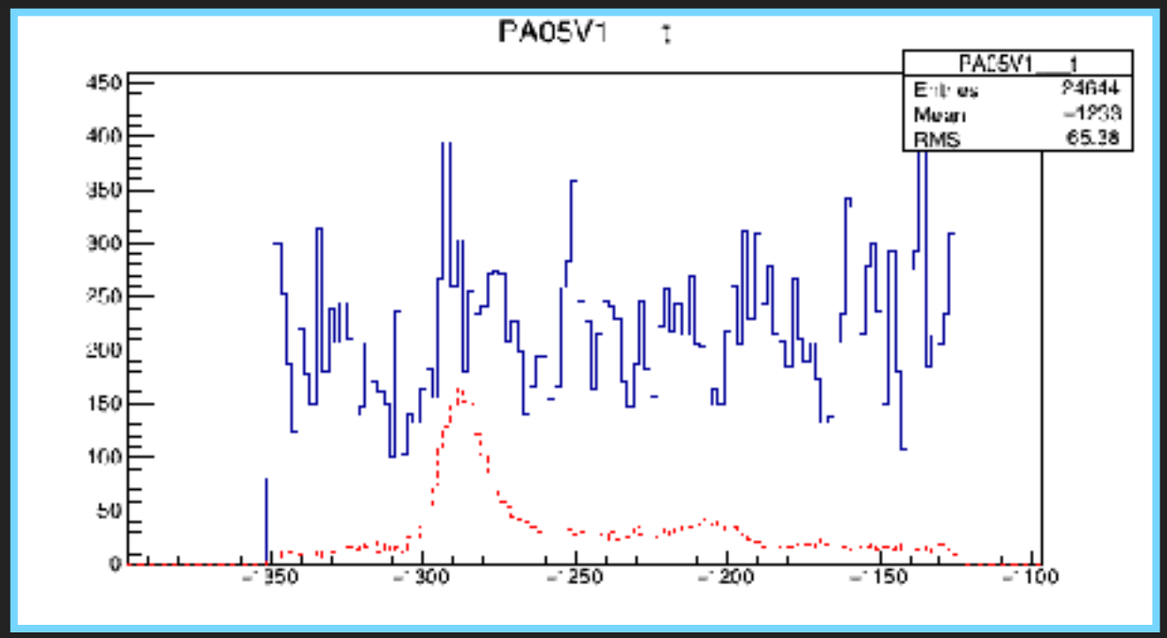
**Excluded channels: mux ports 0, 10, 11**

# FE TEST BEAM: CMAD+FPGA-TDC TEST AT 888

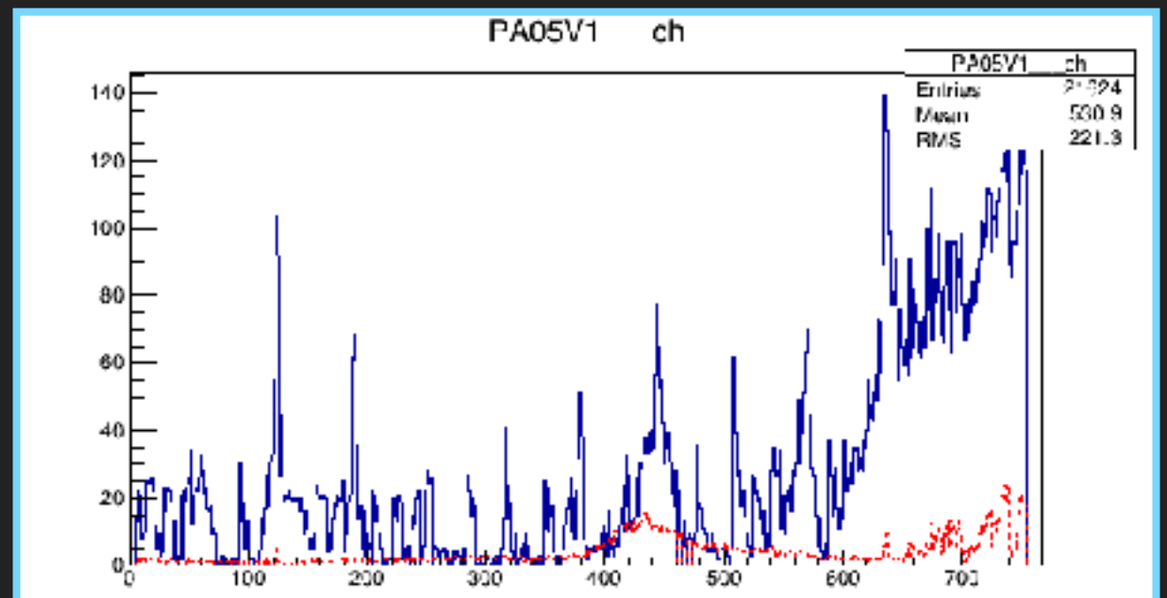
Test with beam (8 Nov): setting DAQ dead time < 4 microsecond

➢ DAQ DT setting: 3_10_250

PA05V: standard FE




low intensity beam, because target polarisation was ongoing:
40cm Be target
collimators 6mm



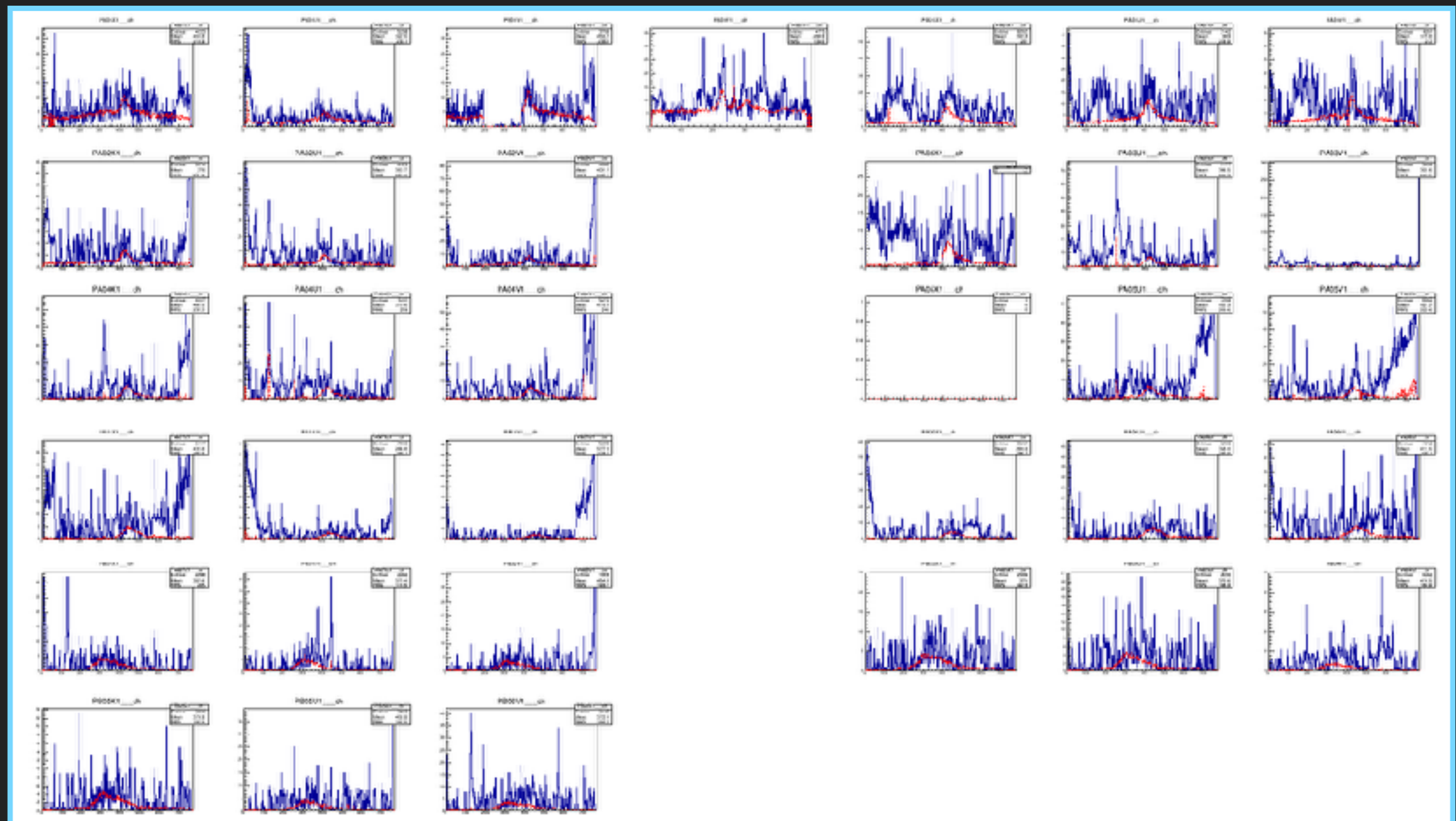

Trigger Setting for Trigger Efficiency study

# FE TEST BEAM: CMAD+FPGA-TDC TEST AT 888

## Test with beam (8 Nov): setting DAQ dead time < 4 microsecond

➢ DAQ DT setting: 1_10_250

MWPC hit Mult: standard FE

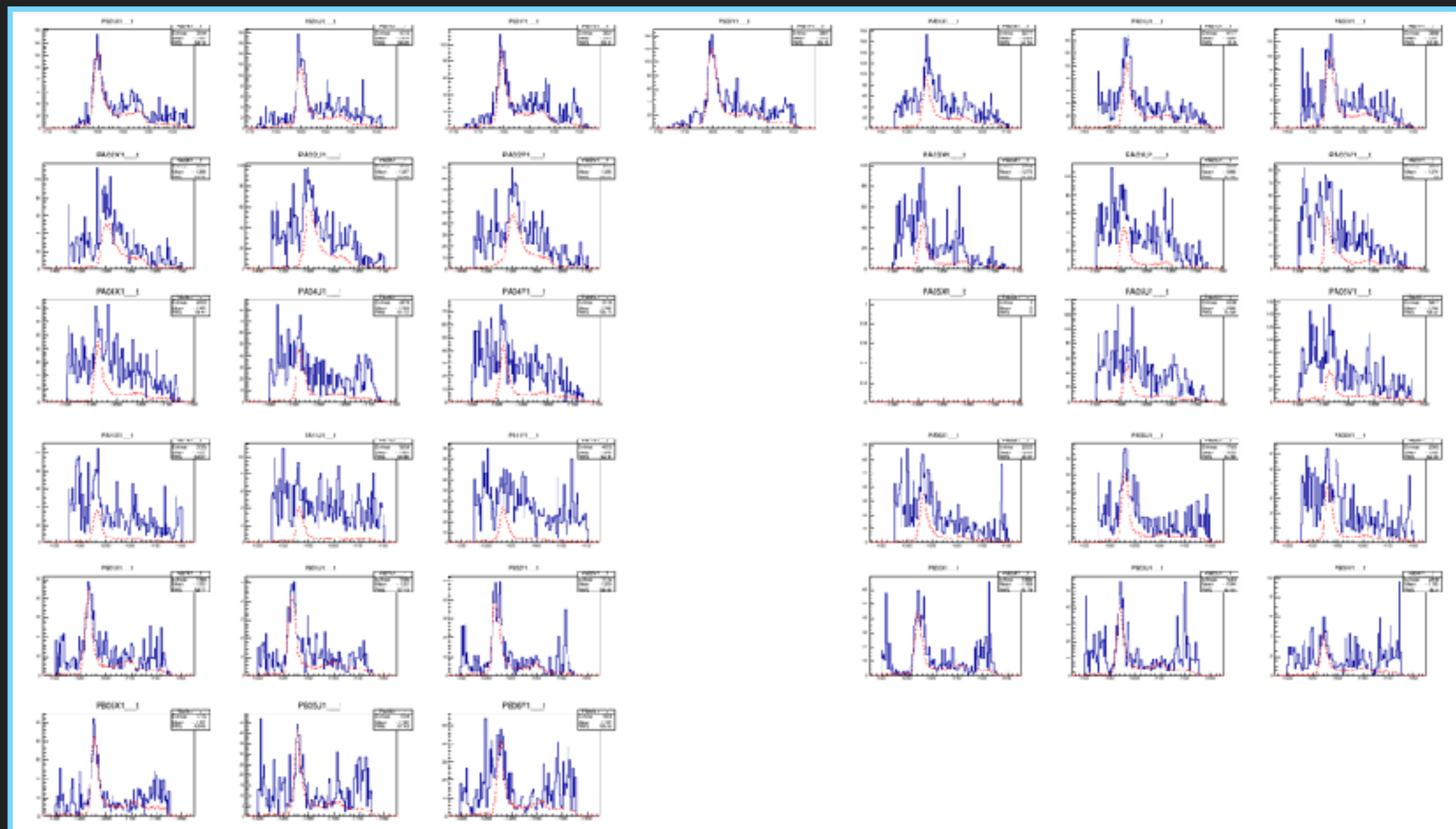


# FE TEST BEAM: CMAD+FPGA-TDC TEST AT 888

Test with beam (8 Nov): setting DAQ dead time < 4 microsecond

➢ DAQ DT setting: 1_10_250

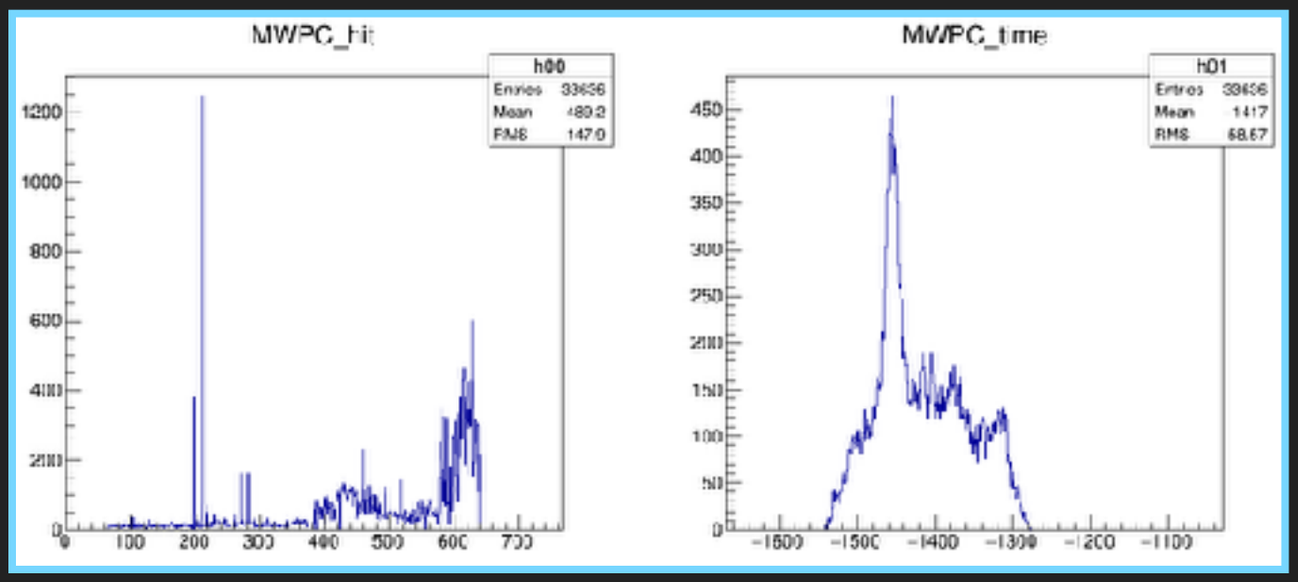
MWPC Time Dist: standard FE



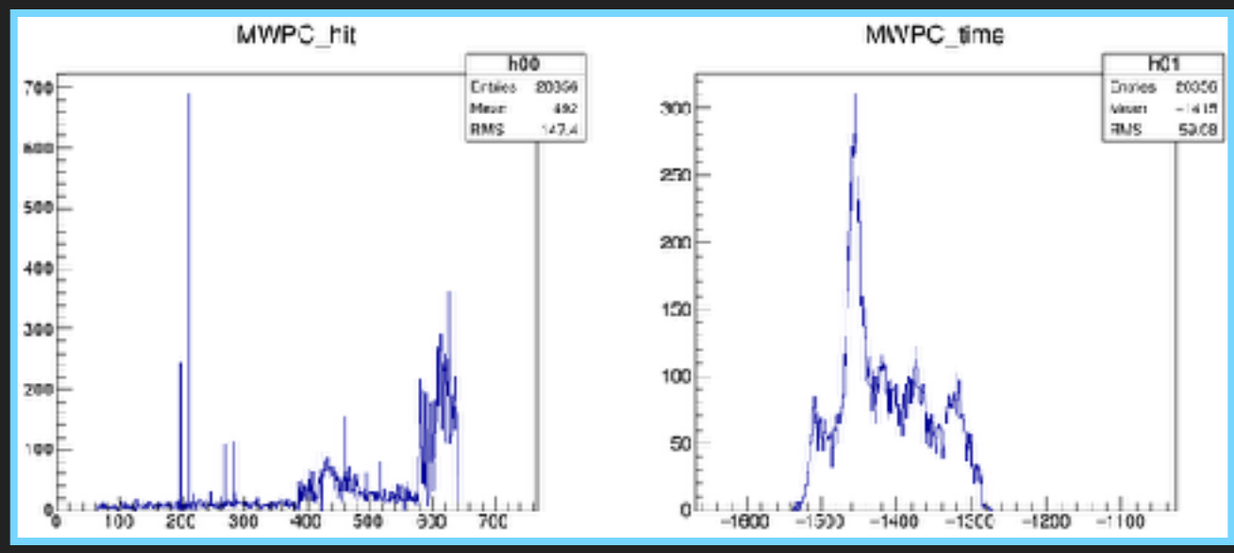
# FE TEST BEAM: CMAD+FPGA-TDC TEST AT 888

## Test with beam (8 Nov): setting DAQ dead time < 4 microsecond

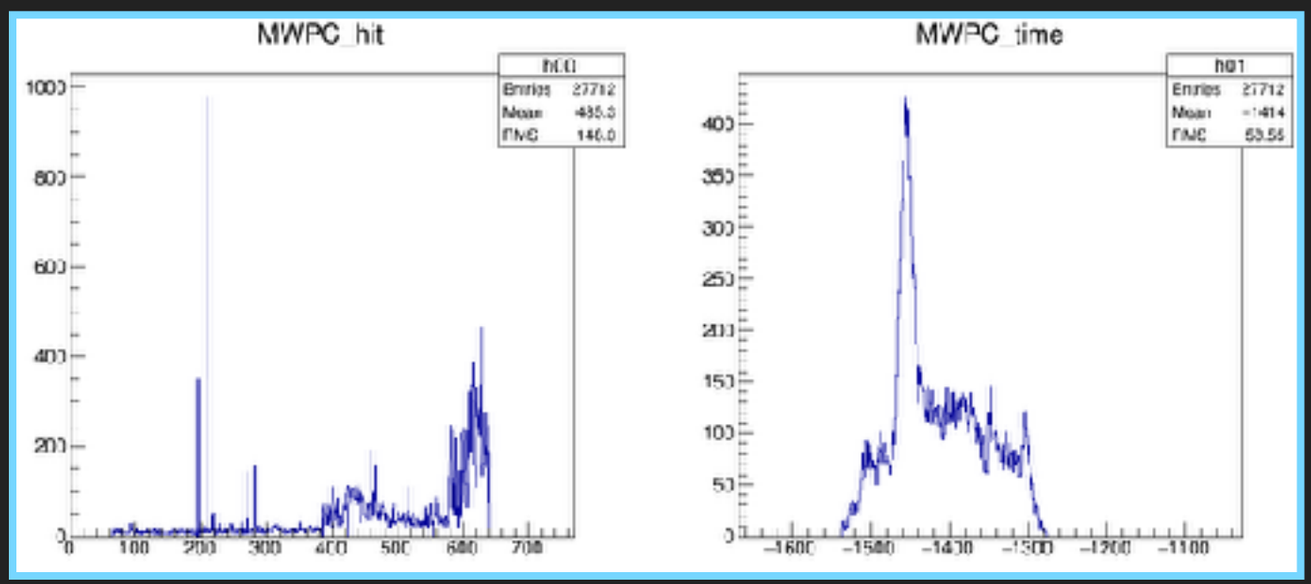
➢ DAQ DT setting: 3_10_250



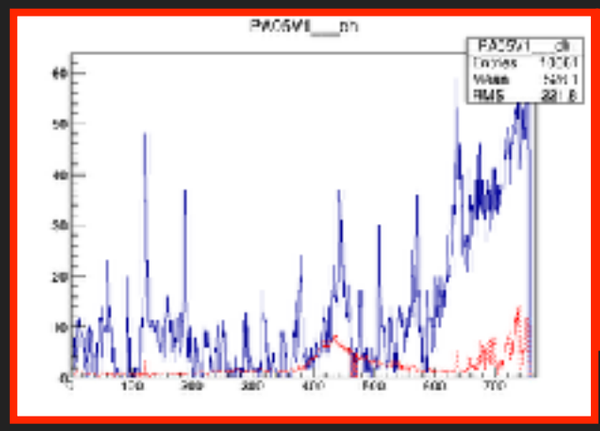

➢ DAQ DT setting: 1_10_250

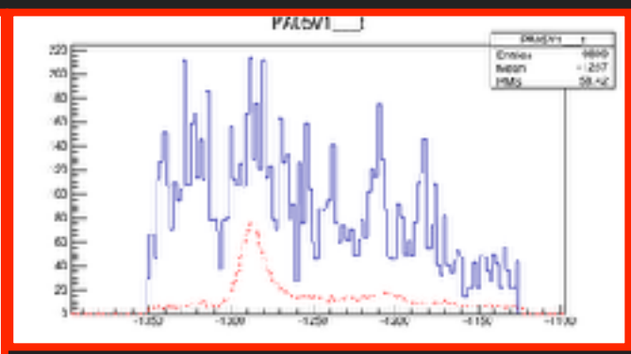


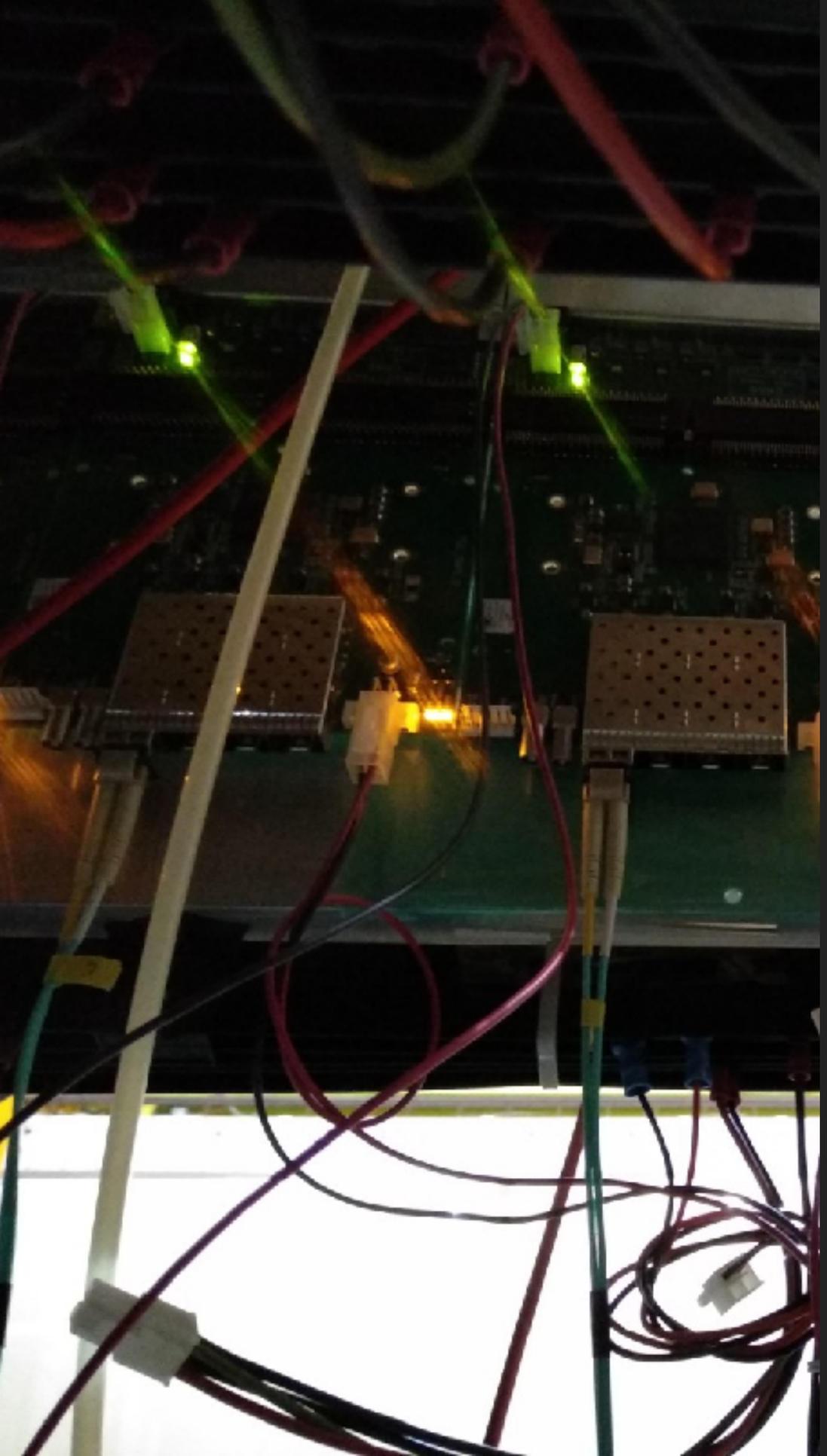

➢ DAQ DT setting: 2_10_250




➢ DAQ DT setting: 1_10_250, Standard FE





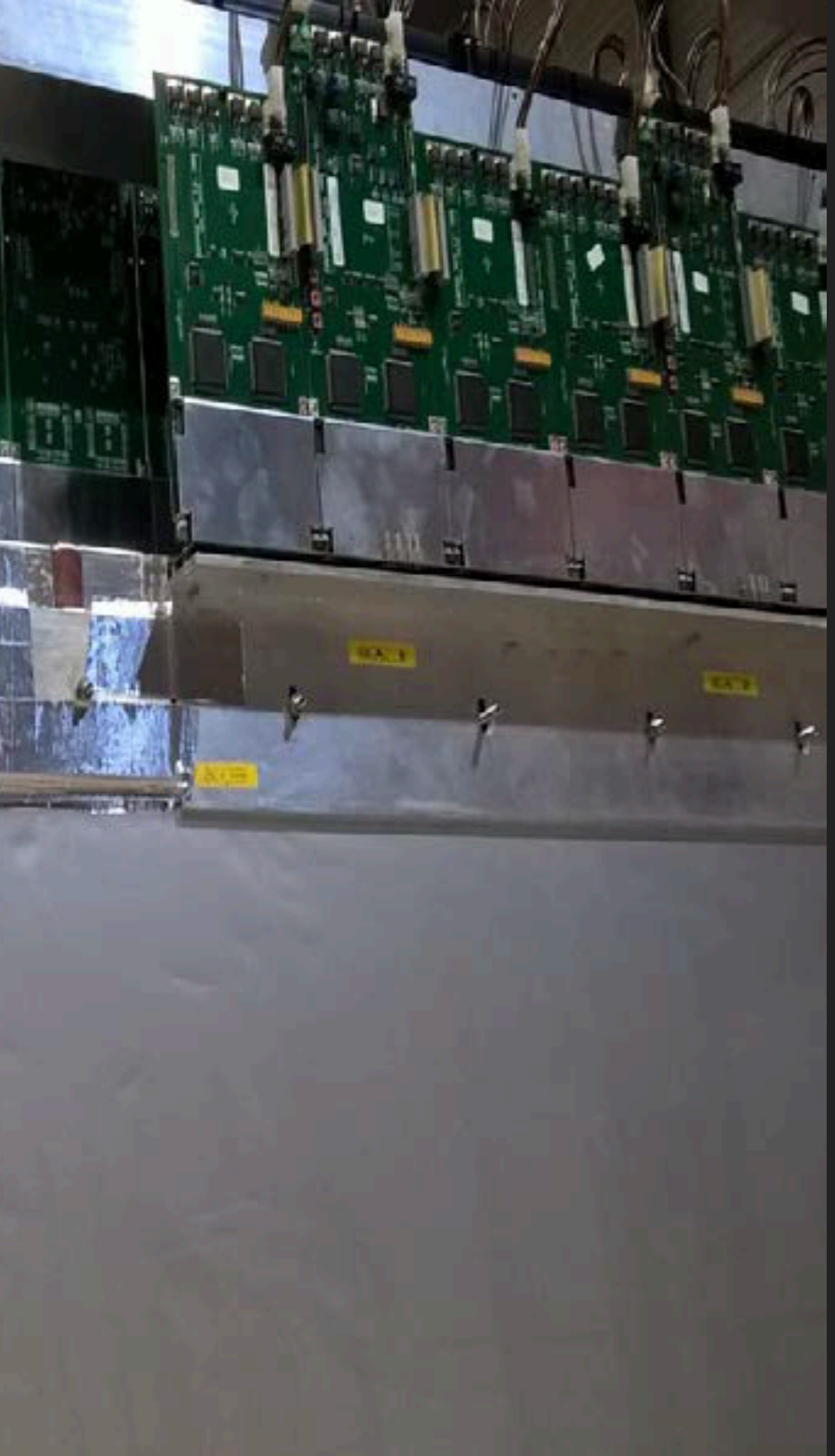


Still to be done: take further data with full intensity beam, performing again a test with DAQ DT < 4 microsecond
With nominal beam intensity and nominal trigger rate and setting

# MANY THANKS TO


ALL THE TEAM INVOLVED, AT CERN AND IN MUNICH AND TORINO

M. ALEXEEV, A. AMOROSO, J. BERENGUER, M. CHIOSSO, D. D'AGO, P. DI CRESCENZO, V. FROLOV, I. KONOROV, A. MAGGIORA

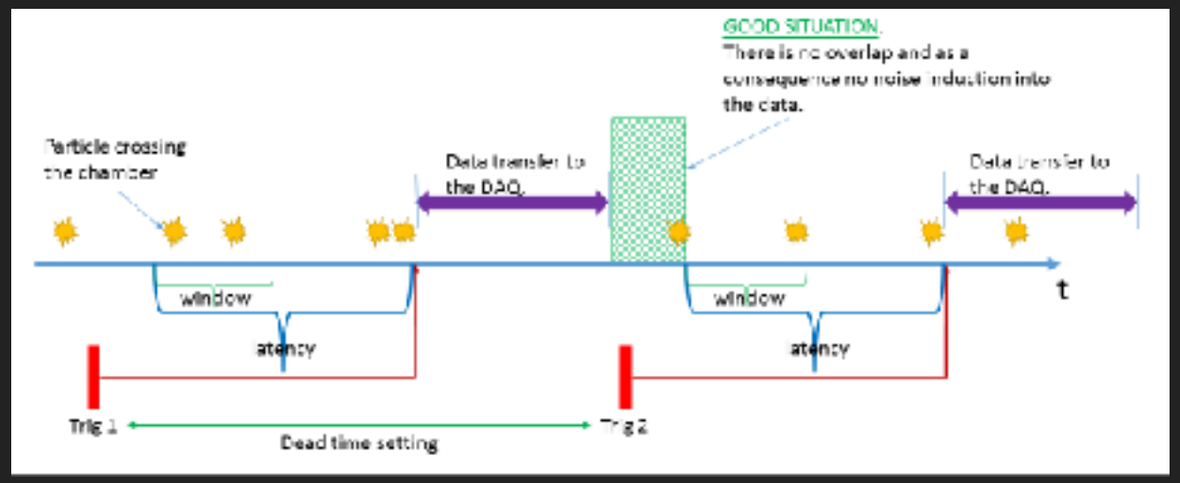


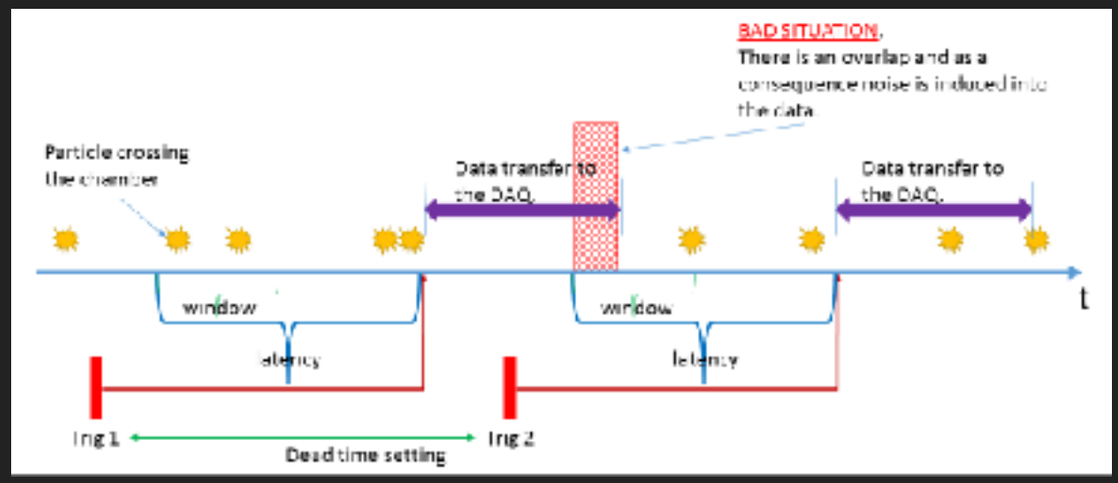
# MWPC

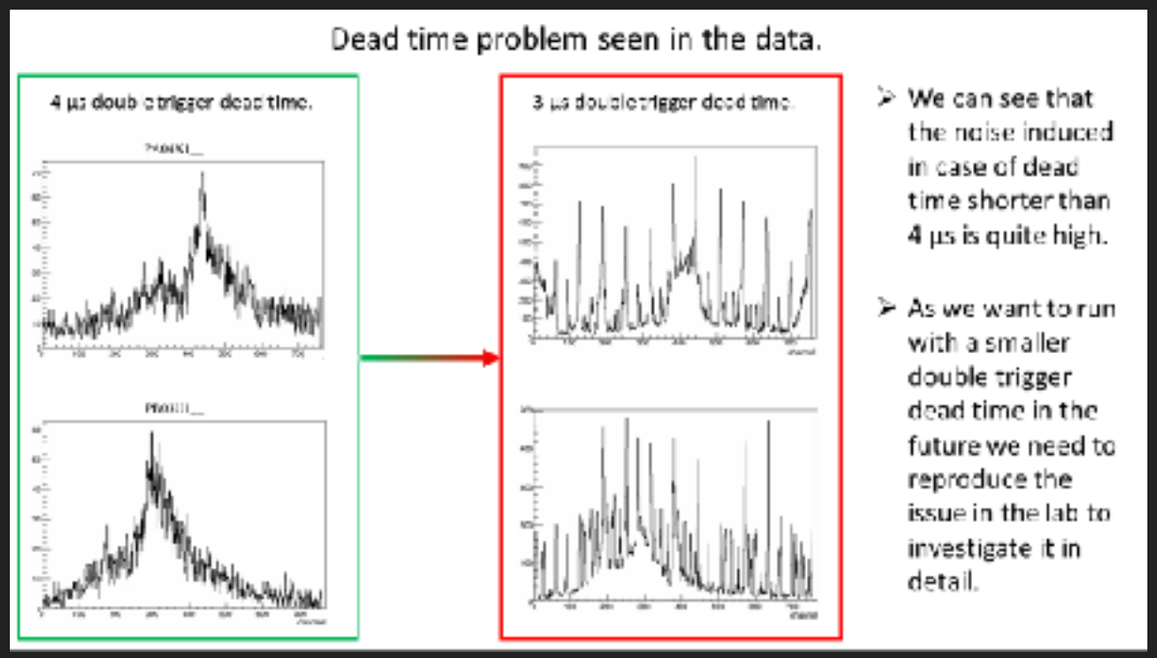
# TEST OF THE NEW FE

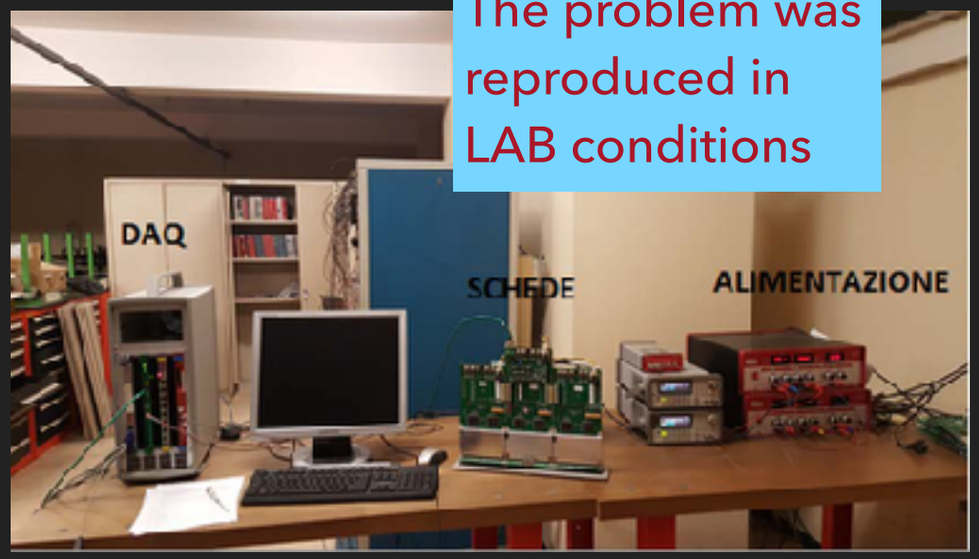
SPARE SLIDES

# OLD FE ELECTRONICS: THE NOISE PROBLEM



# CMAD: GAIN

| *Set Digital Value [dig]* | *Gain [mV/fC]* | *Conversion factor [fC/dig]* |
|---|---|---|
| 0 | 1.1 | 0.41 |
| 1 | 1.0 | 0.45 |
| 2 | 0.9 | 0.51 |
| 3 | 0.8 | 0.55 |
| 4 | 0.7 | 0.59 |
| 5 | 0.6 | 0.70 |
| 6 | 0.5 | 0.86 |
| 7 | 0.40 | 1.10 |
| 8 | 4.4 | 0.10 |
| 9 | 4.0 | 0.11 |
| 10 | 3.6 | 0.12 |
| 11 | 3.2 | 0.14 |
| 12 | 2.8 | 0.16 |
| 13 | 2.4 | 0.18 |
| 14 | 2.0 | 0.22 |
| 15 | 1.6 | 0.28 |

Conversion factor = 0.44[mV/dig] / Gain [mV/fC] ; where 0.44mV/dig = DAC granularity