COMPASS++/AMBER DAQ

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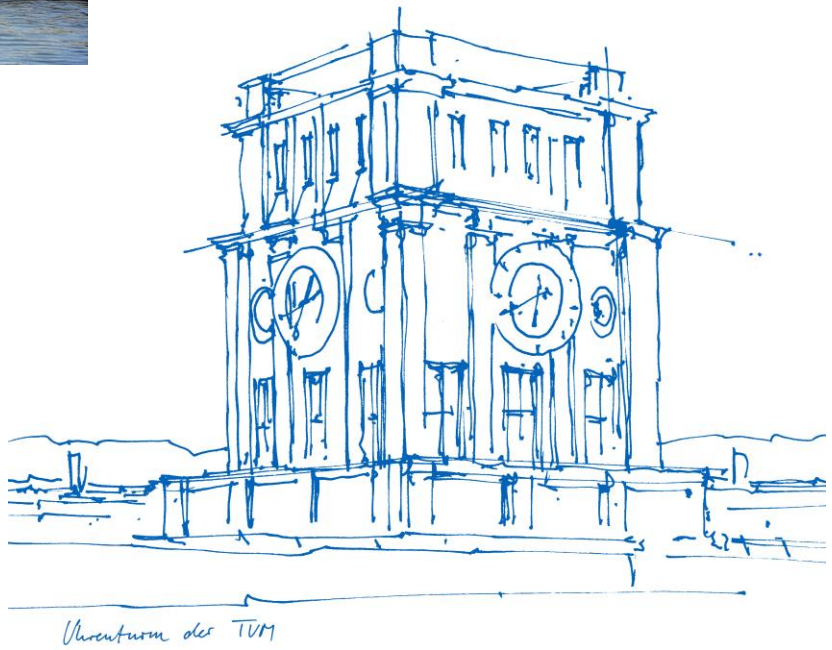
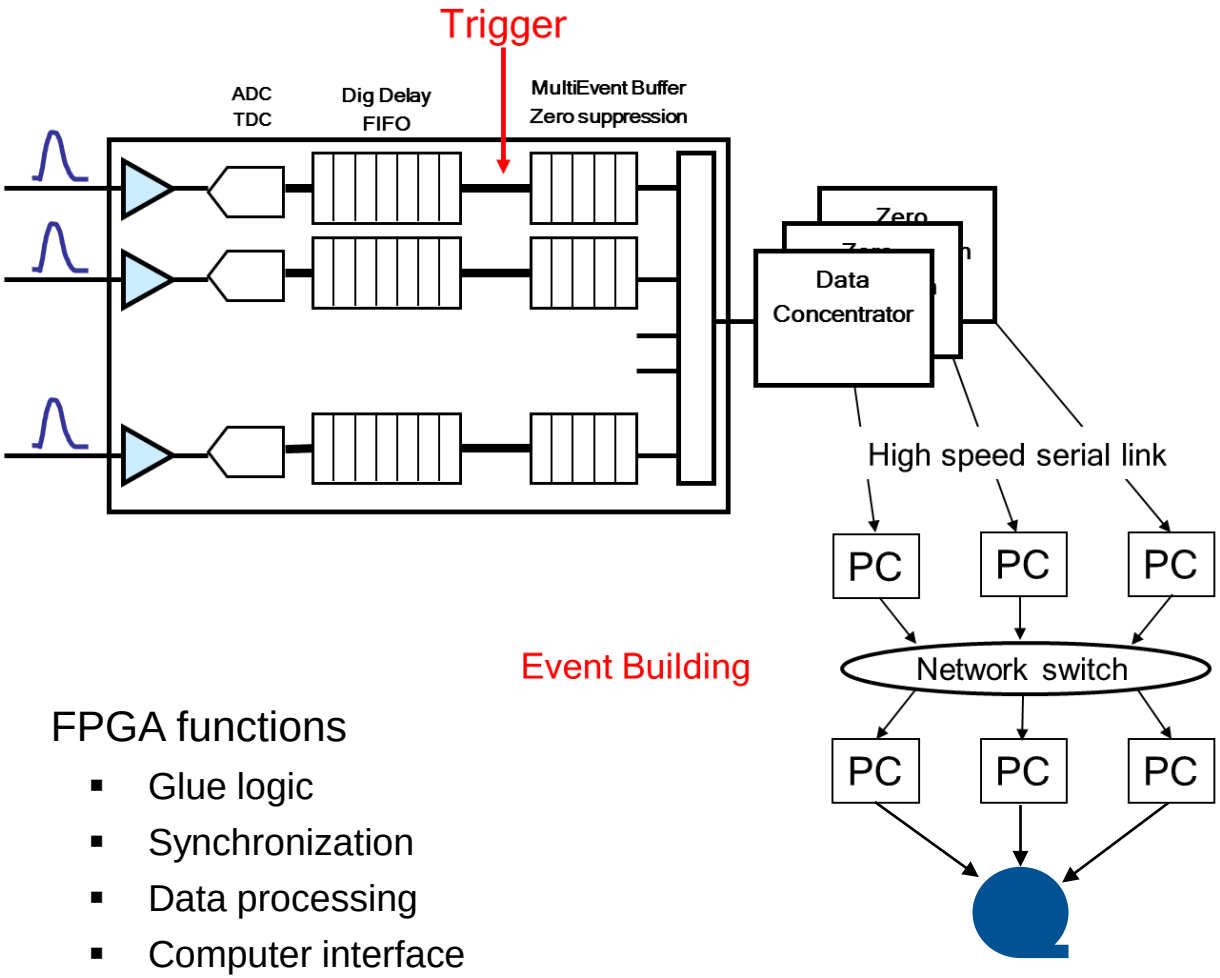


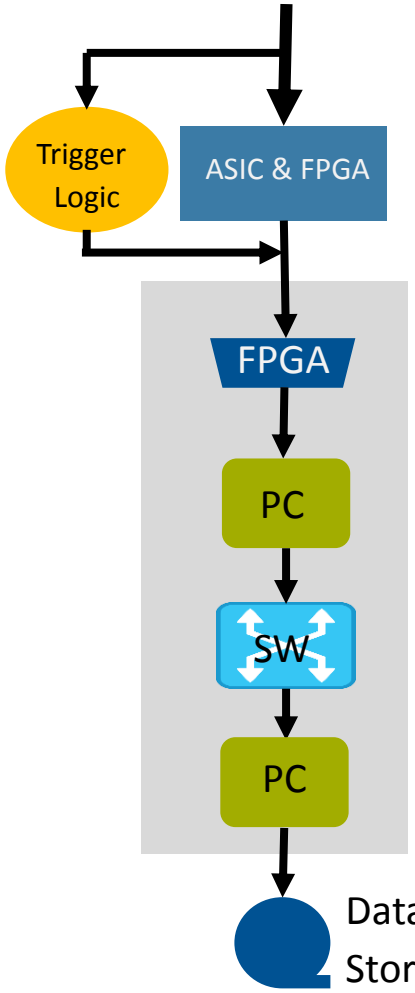
Overview

- COMPASS iFDAQ
- Evolution of FPGA technology
- COMPASS++/AMBER DAQ requirements
- Continuous DAQ Architecture
- Summary

COMPASS DAQ



Event Building

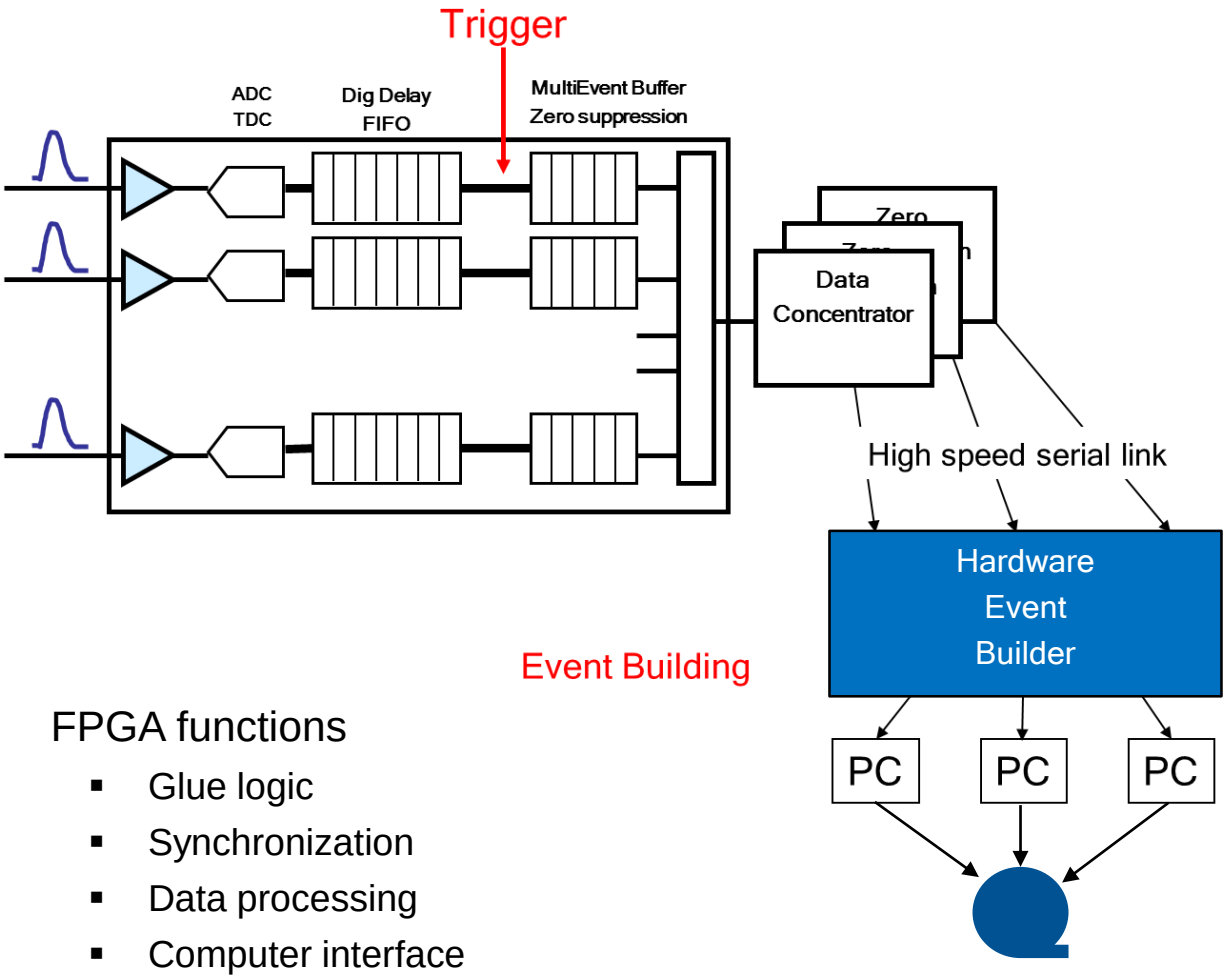


FPGA functions

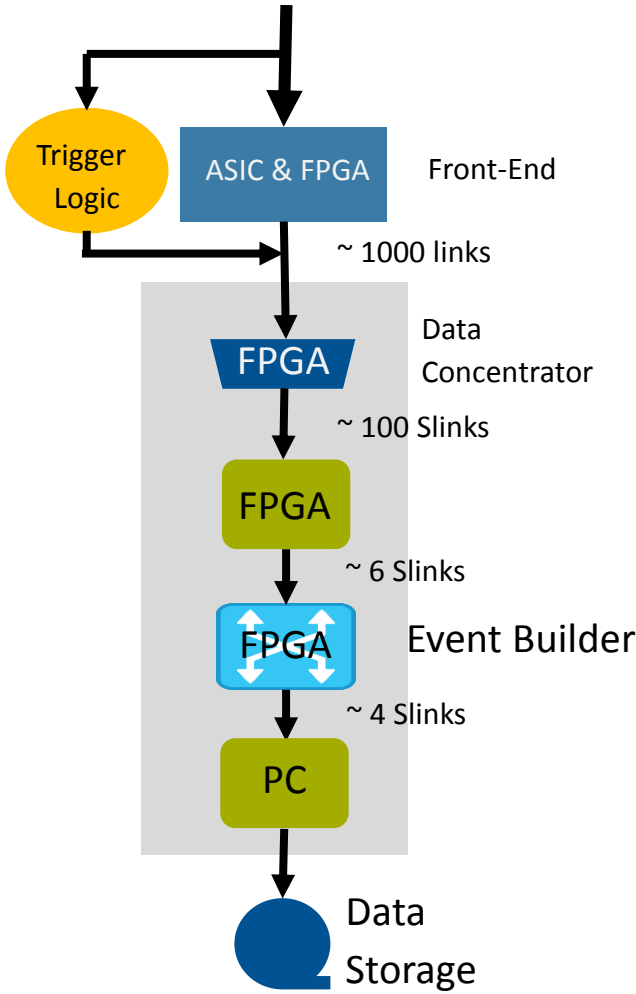
- Glue logic
- Synchronization
- Data processing
- Computer interface

40kHz, 50kB/event

Intelligent FPGA DAQ, after upgrade 2014



Event Building



FPGA functions

- Glue logic
- Synchronization
- Data processing
- Computer interface
- Event builder

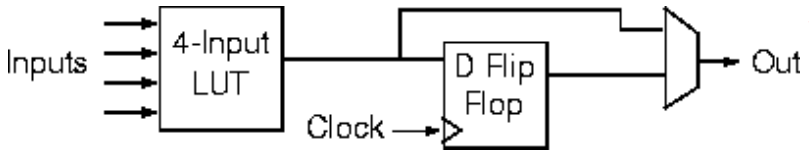
40kHz, 50kB/event

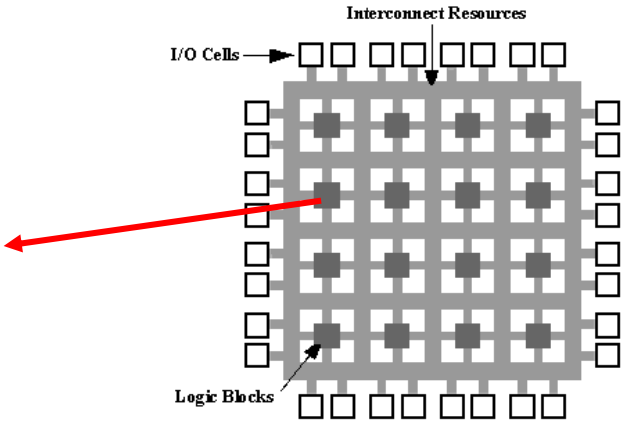
2 GB/s in spill

FPGA Technology Evolution

Field Programmable Gate Array

- 2-D structure of configurable logical block





- Programmable logic and interconnections
- Allows to create very complex digital circuits, limited by number of CLBs
- Maximum frequencies up to 200-400 MHz

Additional circuits:

- Memory blocks
- DSP for integer multiplication and summation
- High bandwidth of serial links, 10 GB/s for low cost FPGA, 300 GB/s for high end FPGAs
- Support external DRAMs

FPGA Technology Evolution

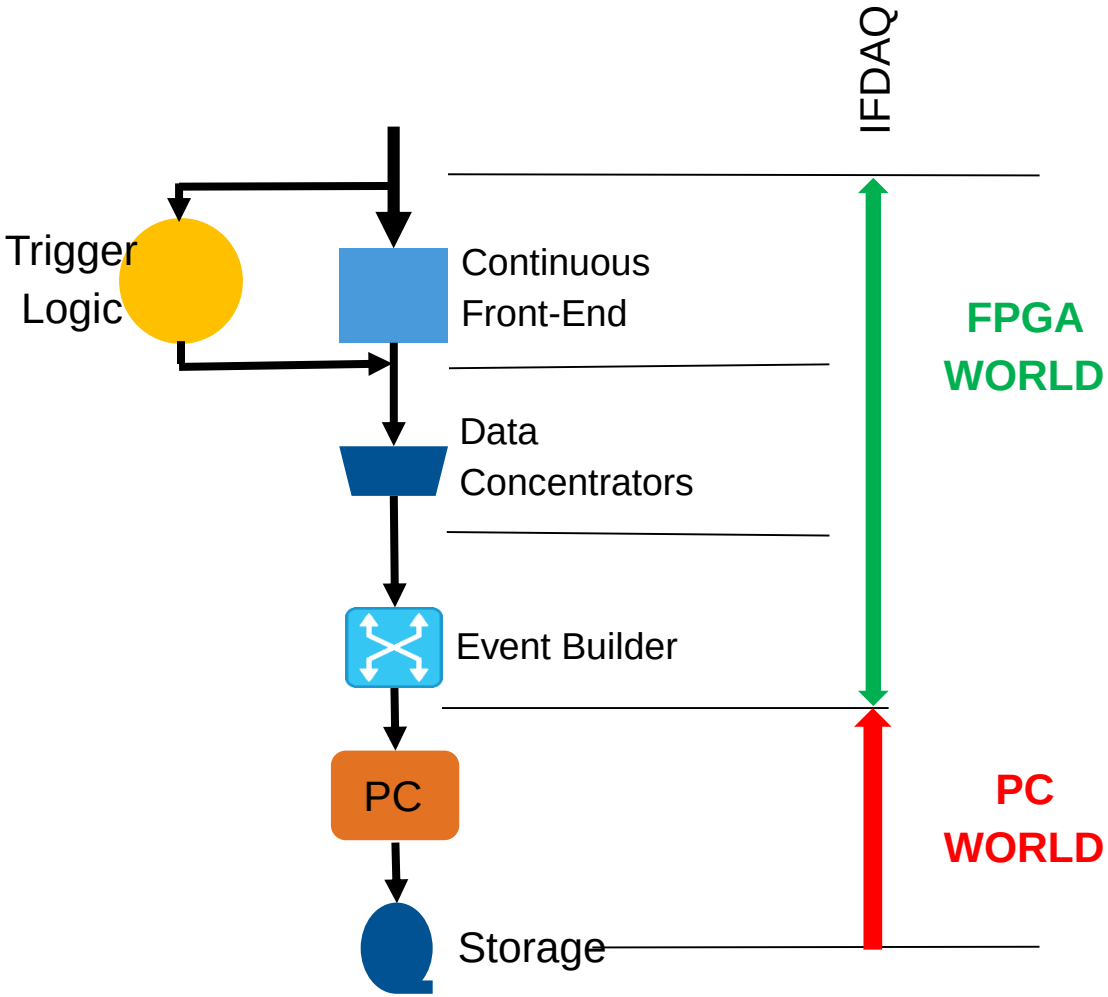
Chip	Manufacturer	Technology	Transistor count
AMD RYZEN 7 3750	AMD	12 nm	19 200 000 000
Intel XEON GOLD 6154	Intel	14 nm	8 000 000 000
FPGA Ultra Scale Plus	Xilinx	16 nm	20 000 000 000

- Highly parallel architecture
- Enormous IO bandwidth
- Low cost , low power
- Long development time => Software tools for a moment behind complexity of HW technology
- Intel and Xilinx apply FPGA technology for data centers

FPGA is ideal technology
for development reliable, high performant, low cost DAQ system

iFDAQ (intelligent FPGA DAQ)
Reliability achieved by smart recovery algorithms included in FPGA

DAQ Architectures



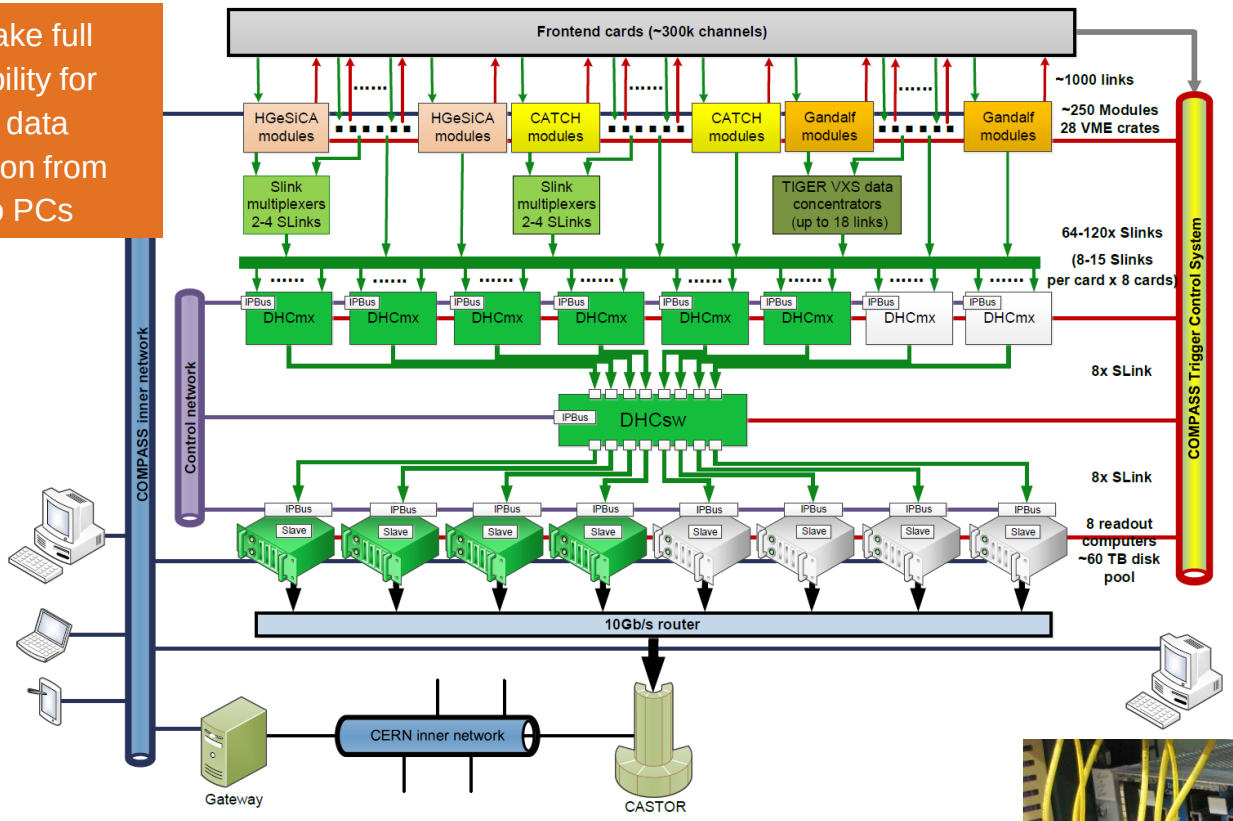
Motivation for hardware event builder
- FPGA is real realtime technology
- Minimize number of real-time software processes
- Simplify software functionality => increase reliability
- Fast recovery time after crash

iFDAQ Frame work
- Implementing congestion free Event Builder
- Intelligent data handling
- Unified Interfaces
- Unified FPGA IP Cores

Advantages
- Increased compactness
- Increased reliability
- Reduced cost

iFDAQ Architecture

FPGAs take full responsibility for reliable data transmission from FEEs to PCs



DHmx, DHsw

- Virtex6 XC6V75
- 4GB, DDR3
- 16x6.5 Gb/s links

Intelligence elements in hardware:

- Self synchronized data flow (backpressure and throttling)
- FEE Error diagnostics and handling to prevent DAQ crashes => monitoring ,
- Automatic resynchronization of FEEs

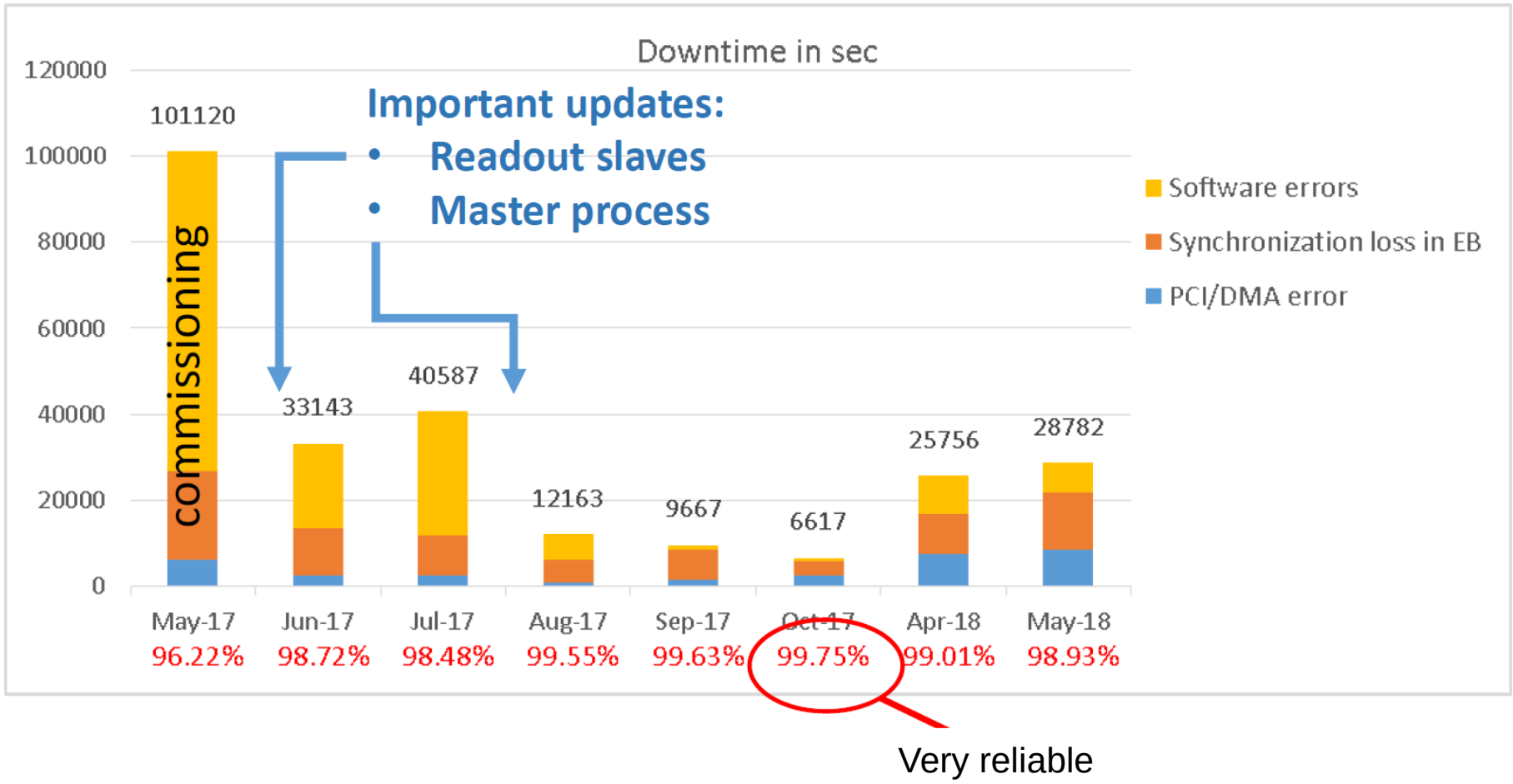
⇒ FEEs can be attached/detached at any time

- Continuous data taking. Stop only in case of problems

Unified interfaces:

- Slink for data transmission
- TCS for time and trigger distribution
- IPBUS for monitoring and configuration

iFDAQ Up Time



COMPASS++/AMBER Requirements

Programme	Physics Goals	Beam Energy [GeV]	Beam Intensity [s^{-1}]	Trigger Rate [kHz]	Beam Type	Target	Hardware additions
muon-proton elastic scattering	Precision proton-radius measurement	100	$4 \cdot 10^6$	100	$\mu^{\pm}$	high-pressure H2	active TPC, SciFi trigger, silicon tracking
Drell-Yan	Pion PDFs	190	$7 \cdot 10^7$	50	$\pi^{\pm}$	C/W	target modification
Input for Dark Matter Search	$\overline{p}$ production cross section	20-280	$5 \cdot 10^5$	25	p	LH2, LHe	liquid helium target, RICH?

Challenges

- Precision measurements => high statistics, high data rate
- Variable set of detectors
- Big variation of detector time resolutions from sub nanoseconds to 60 microseconds
- Different and complex trigger algorithms
  - PRM : Recoil proton (TPC, 60 us drift time) and scattered muon trigger (SciFi, Pixel Silicon)
  - Drell-Yan : Target pointing muon trajectories and muon multiplicity

COMPASS++/AMBER DAQ

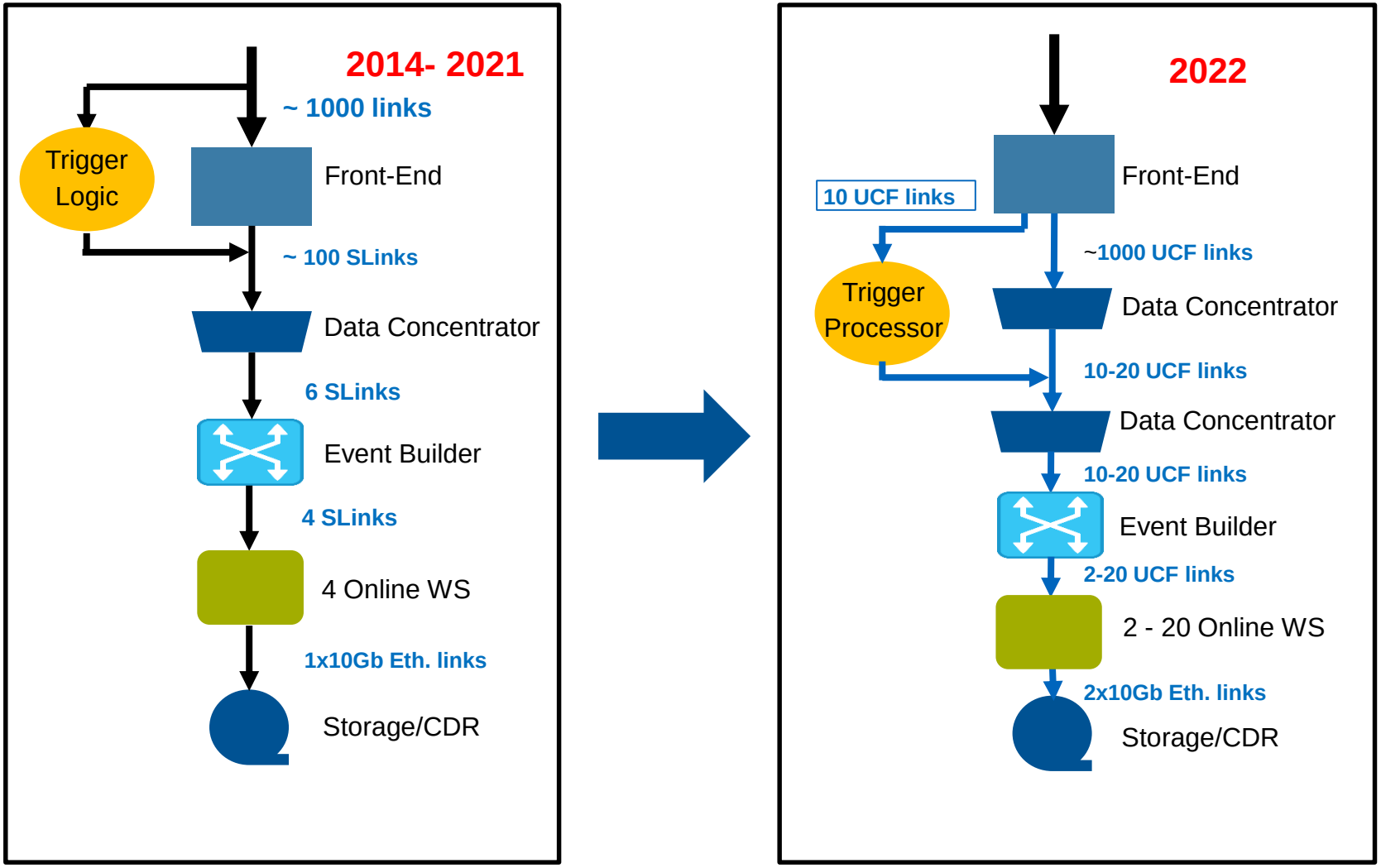
DAQ architecture

- Continuous or trigger less front-end electronics with signal detection and feature extraction
  - HIT : channel ID, amplitude and/or Time Tag
- Information from any detector can be included in trigger logic
- Provision of big trigger latency in order of milliseconds or even seconds
- Programmable Hardware Trigger Processor
- Configurable DAQ topology by employing cross-switch
- High data rate capable event builder

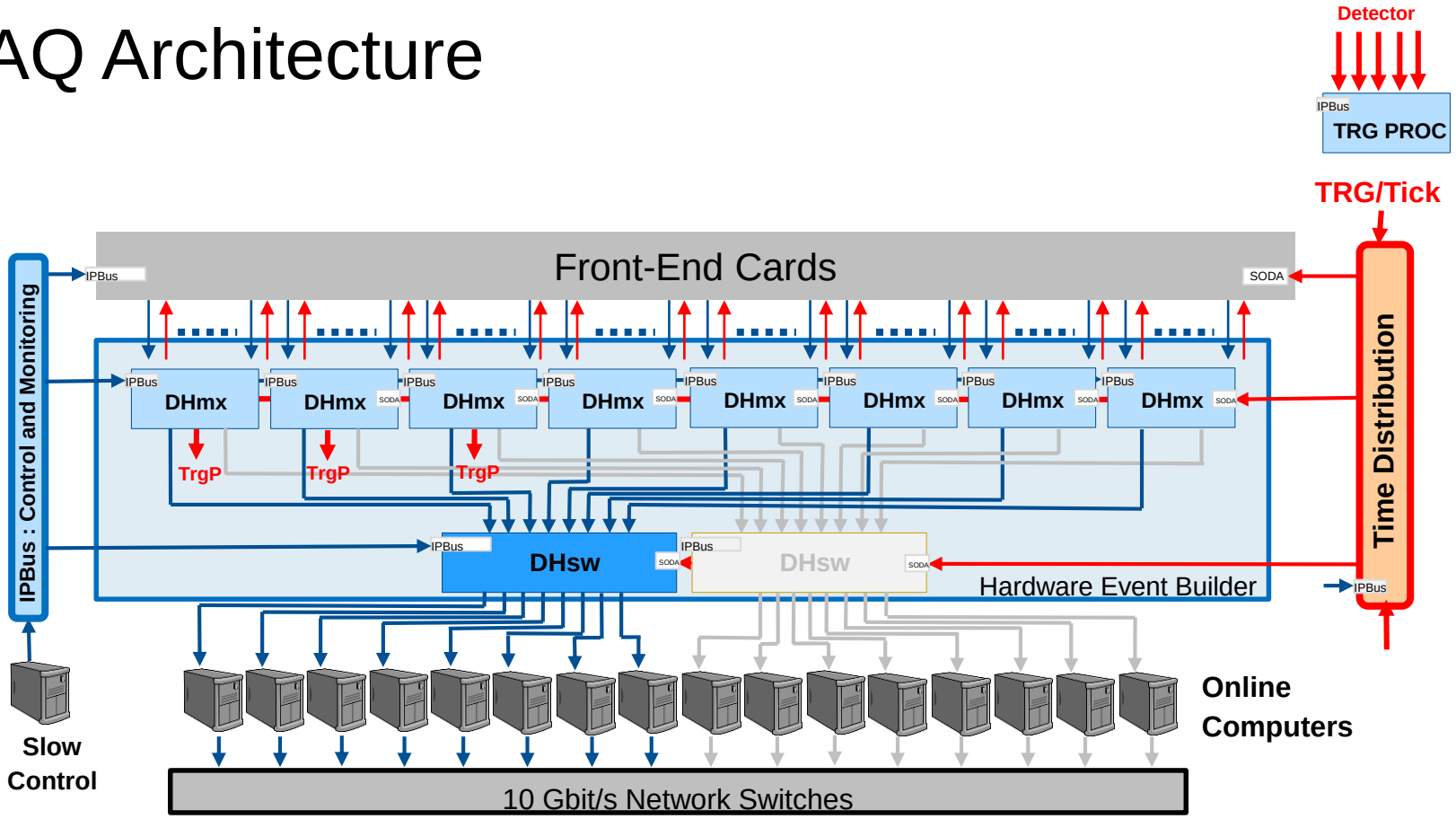
Data rate

Programme 2022-2024	Beam Rate	Trigger rate	Non triggered Data Rate	Final Data rate limited by storage
Proton Radius Measurement	$2 \cdot 10^6 - 10^7$	100 kHz	10 GB/s in spill, 3GB/s sustained	< 2 GB/s
Drell-Yan	$7 \cdot 10^7$	50kHz	30 GB/s in spill 10 GB/s sustained	500 MB/s
Input for Dark Matter search	$5 \cdot 10^5$	25 kHz	?	250 MB/s

Evolution of COMPASS DAQ Architecture



iFDAQ Architecture

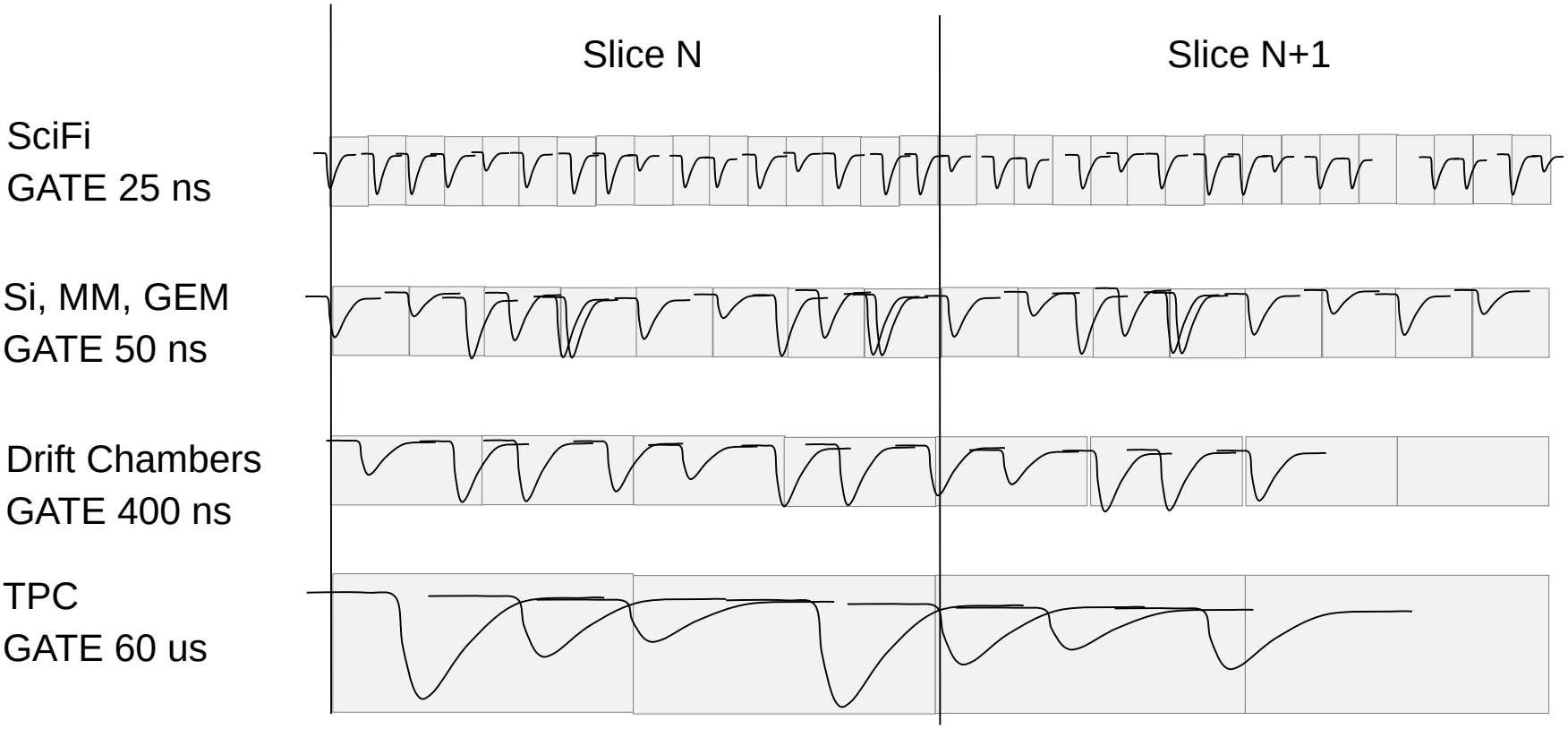


Serial link bandwidth is 10 Gb/s (1GB/s)

Event builder is scalable to 20 GB/s sustained data rate

Expected single PC bandwidth 1GB/s

Data Structure of Continuous DAQ

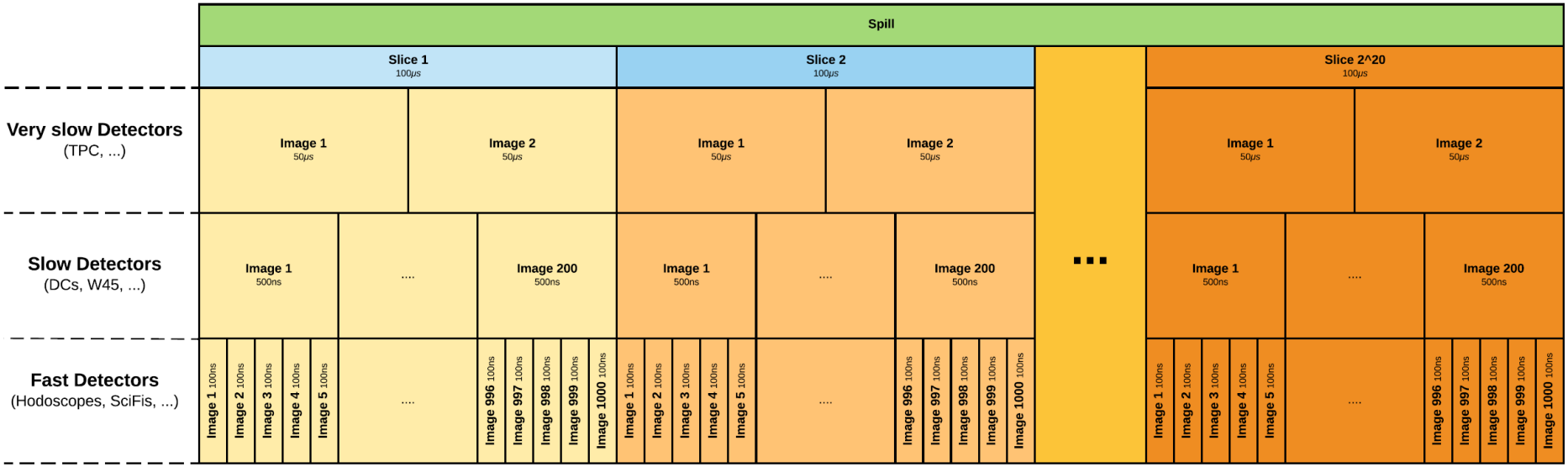


For 2022 it's foreseen to collect data in untriggered mode

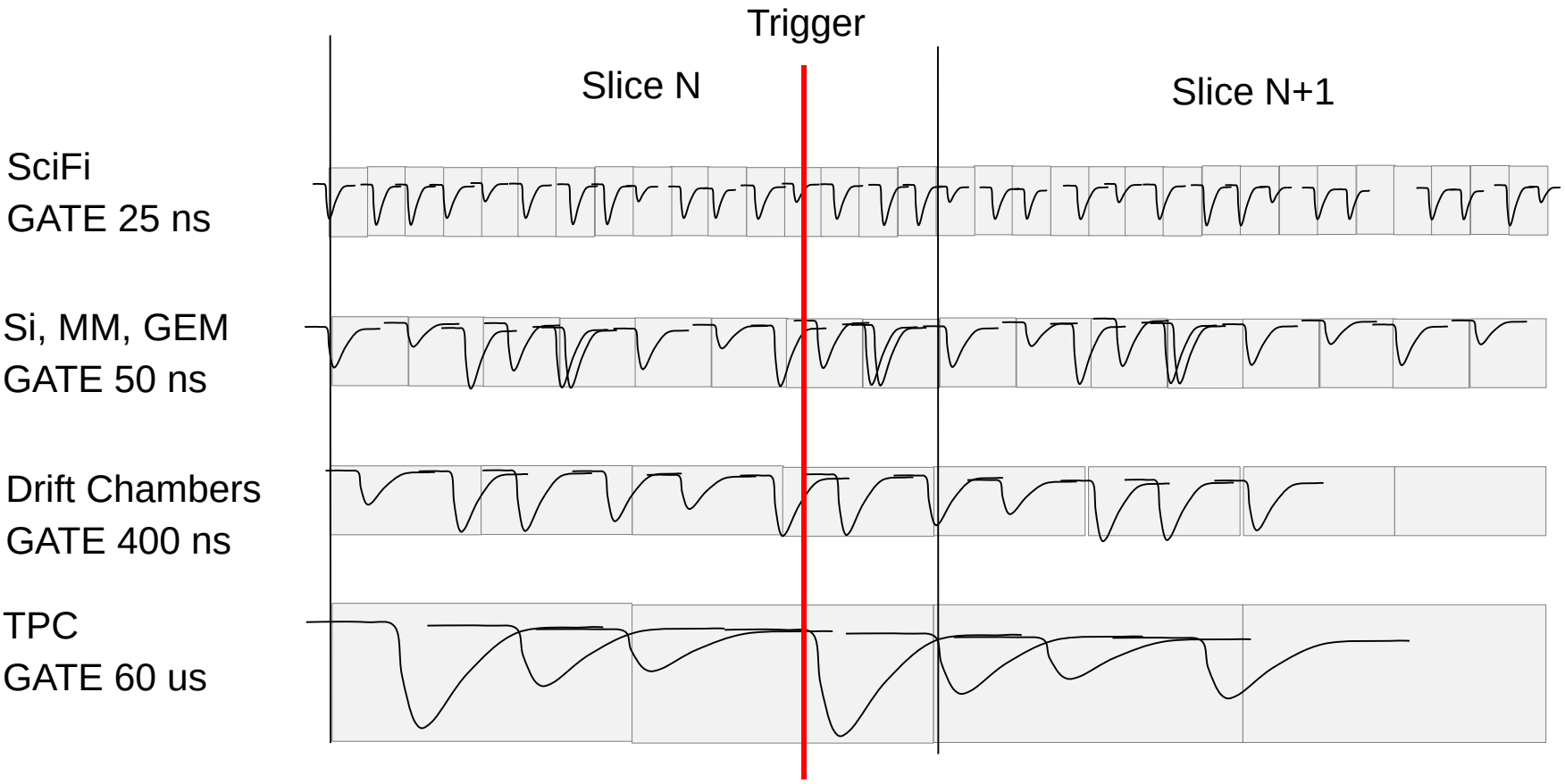
Time Slice => Event

Sustained data rate is limited to 2GB/s by Central Data Recording

Data Structure of Continuous DAQ



Triggering


Trigger
Slice N
Slice N+1
SciFi
GATE 25 ns
Si, MM, GEM
GATE 50 ns
Drift Chambers
GATE 400 ns
TPC
GATE 60 us

Triggering

SciFi
GATE 25 ns

Si, MM, GEM
GATE 50 ns

Drift Chambers
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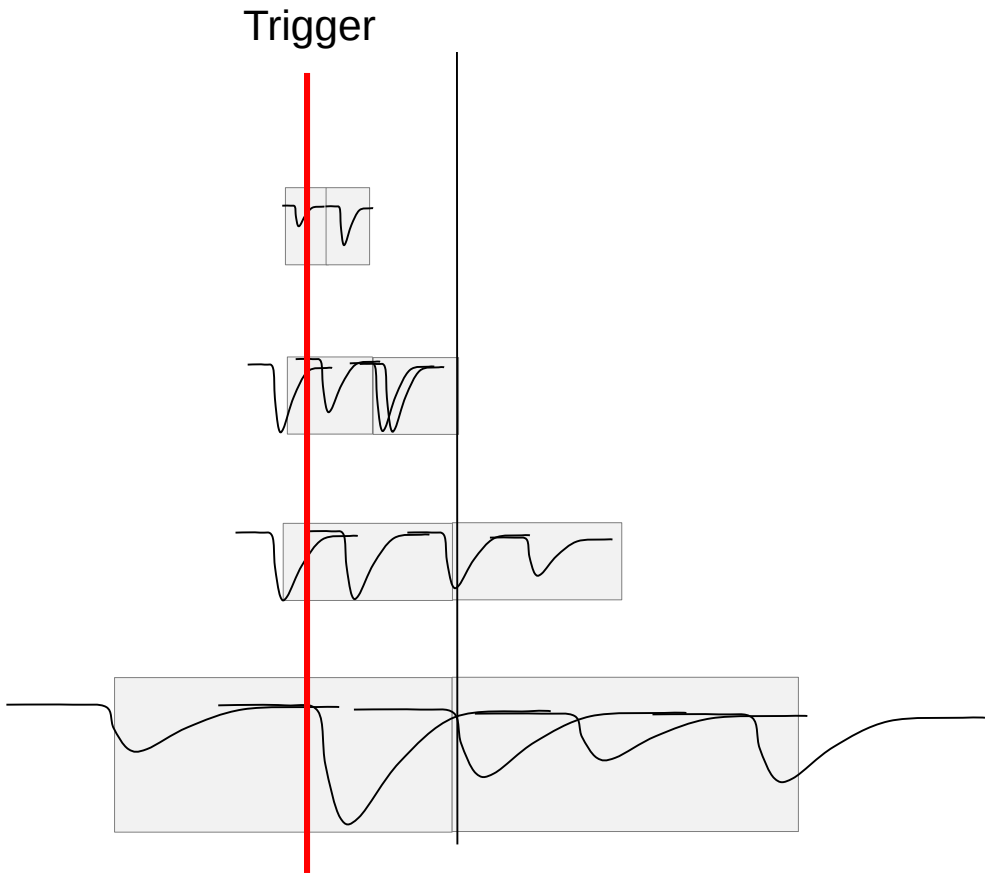
TPC
GATE 60 us



Triggered mode will be employed in 2023

FRONT-END ELECTRONICS

COMPASS++/AMBER Detectors and FEE

Detectors	Front-Ends	Comments
▪ SciFi, BMS, Hodoscopes	iFTDC, 200/400 ps	FW upgrade
▪ CEDAR	iFTDC, 200 ps	FW upgrade
▪ DC, Straw, MWPC, MW	iFTDC, 800 ps	FW upgrade
▪ TPC	FADC, 14 bit 250 MHz	ready
▪ Silicon Pixel	MuPix10	prototype
▪ HCAL, ECAL	MSADC, 12 bit 80 MHz	HW and FW upgrade
▪ RICH, MM, GEM	VVM, SAMPA	performance to be evaluated

iFTDC

- ARTIX7 FPGA
- TDC implemented in FPGA using built-in SERDES(serialized/deserializer) circuit
- Firmware versions
  - 64 channels 0.8/0.4 ns bin, 0.25/0.14 ns resolution
    - 2xSERDES/channel, half bin shift
  - 32 channels 0.2 ns bin, 80 ps resolution, 40% DNL
    - 4xSERDES/channel, ¼ bin shift
  - 4 ns dead time
  - Low hit rate version, maximum 5 MHz/channel
  - High hit rate version, maximum 80 MHz/channel
- Up to 4 UCF interfaces for very high hit rate conditions

- Ethernet interface for lab setups

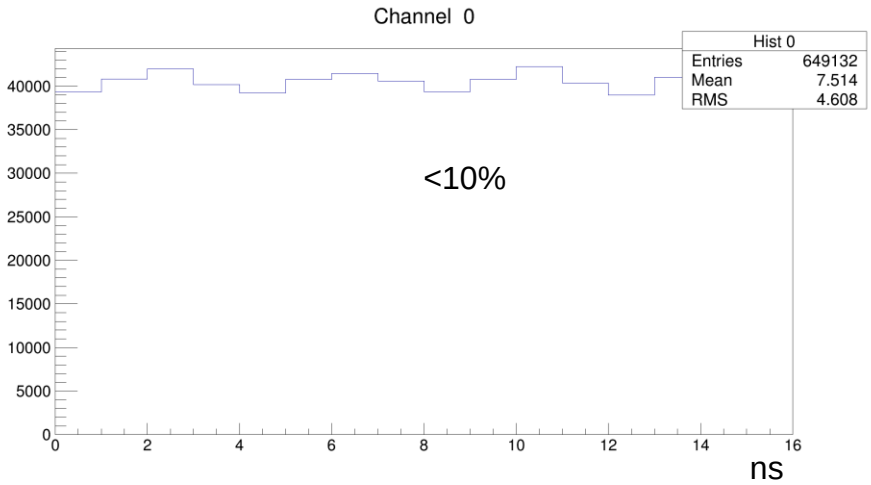
iFTDC

Differential non linearity

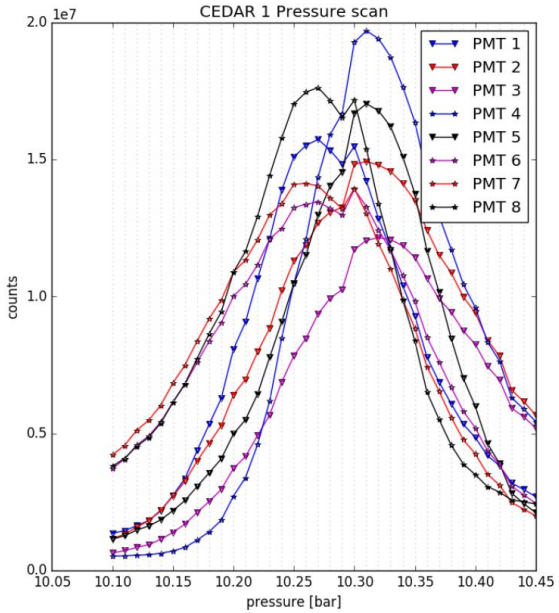
- 1 ns/bin < 10 %
- 0.4 ns/bin < 25%
- 0.2 ns/bin < 50%

Built-in functionality :

- Hit rate counter, accessed via slow control interface
- Data rate measurement with data taking



TDC bin size variation, DNL



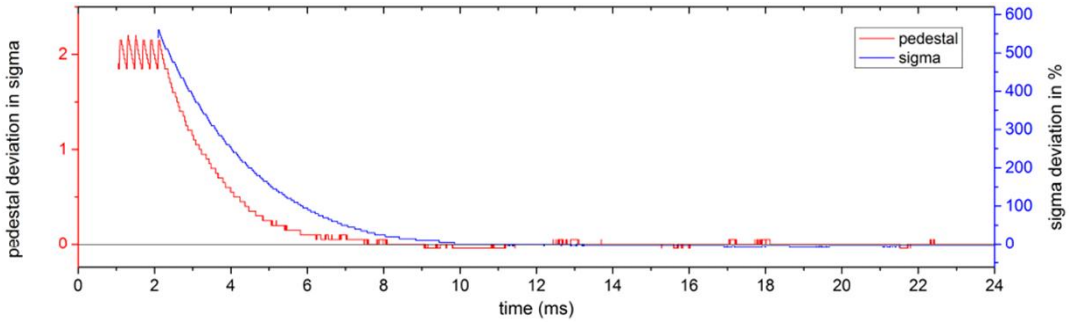
Example of CEDAR pressure scan

MSADC Upgrade

- 16 channel 12 bit @80 MHz
- Upgrade to Kintex/Zink FPGA, 2020
- Baseline follower pedestal and RMS calculation, programmable number of samples

$$\Sigma_{\text{ped}} = \Sigma_{\text{ped}} + s_i - \bar{s}, \qquad \bar{s} = \Sigma_{\text{ped}}/N$$

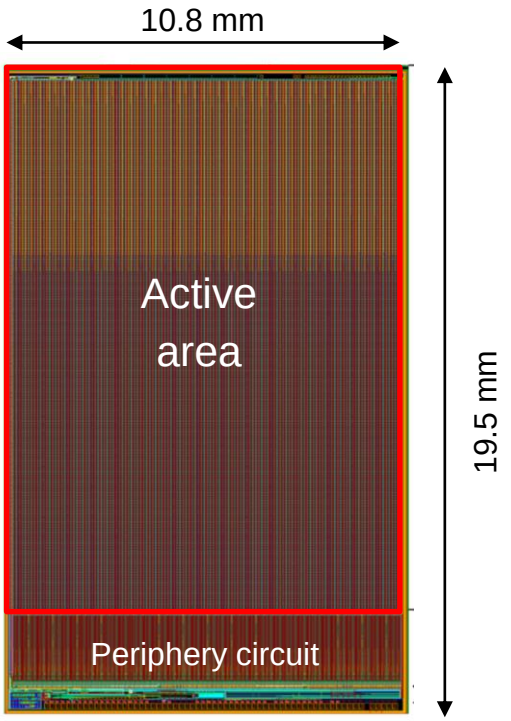
$$\Sigma_{\text{diff}} = \Sigma_{\text{diff}} + (s_i - \bar{s})^2 - \sigma^2, \quad \sigma^2 = \Sigma_{\text{diff}}/N$$



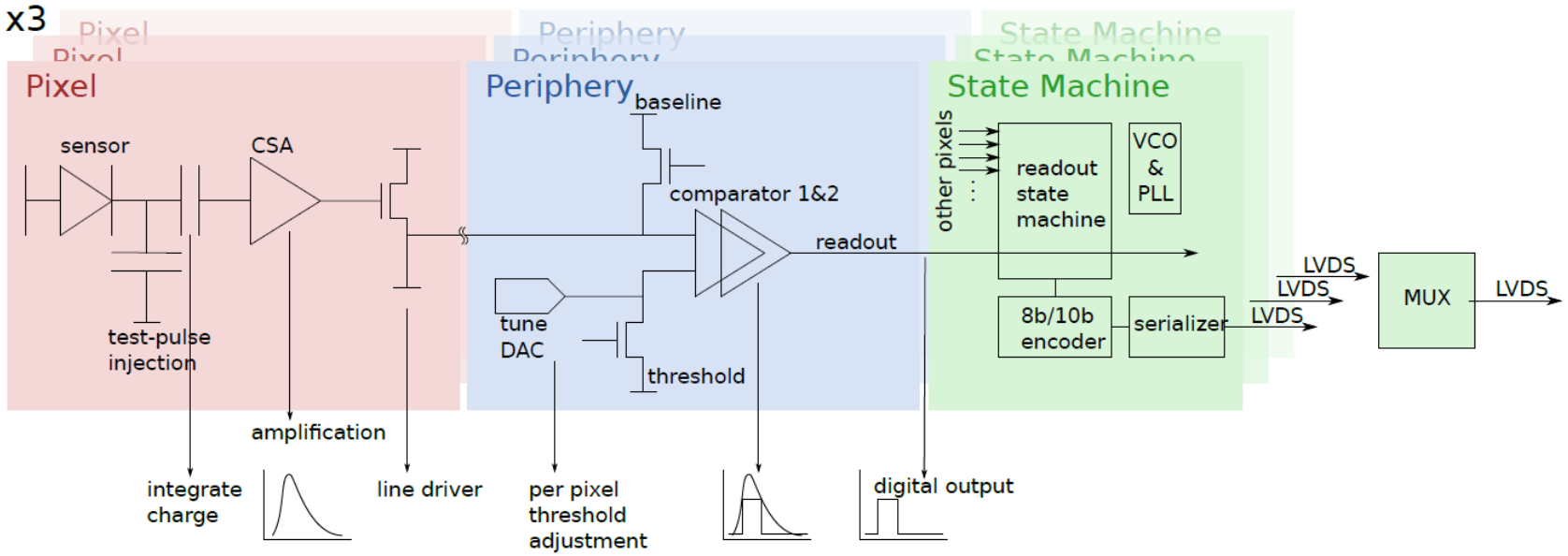
- Advanced Signal processing in FPGA for signal detection and feature extraction down to SNR ~ 3
(Warsaw TU, Trieste INFN/ICTP)

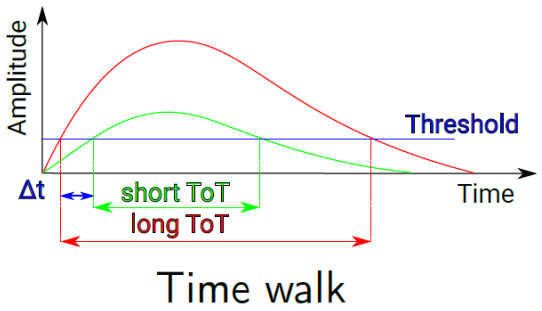
MuPix8 CMOS Monolithic Pixel Detector

- From Heiko Augistin talk, Mu3e collaboration
- Monolithic Silicon pixel detector MuPix8
  - Developed by Karlsruhe IT, Ivan Peric group
  - 80x81 um² pixel size, thinned down to 62.5 µm
  - 1x1.6 cm² active, 128x200 pixels
  - MuPix10 => 2x2 cm²
  - Trigger less read out



MuPix8





2 thresholds

32 bit/hit, row address, column address, Time Tag, ToT

3 high speed links 1.25 Gb/s

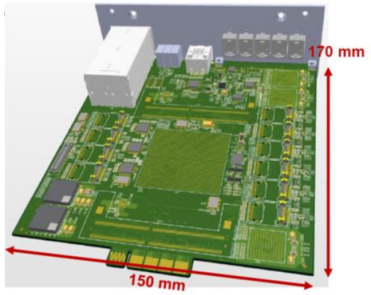
1 us dead time/pixel

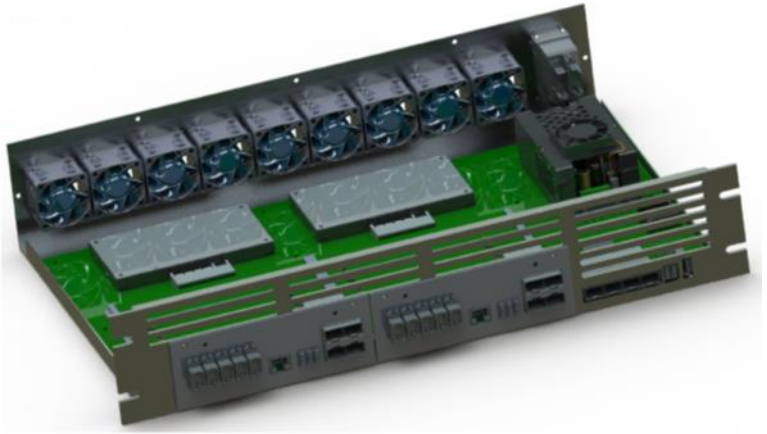
48x200 pixels connected to HS link => 10 Mhits/s

DAQ/Trigger Processor Hardware

New DAQ FPGA Switch

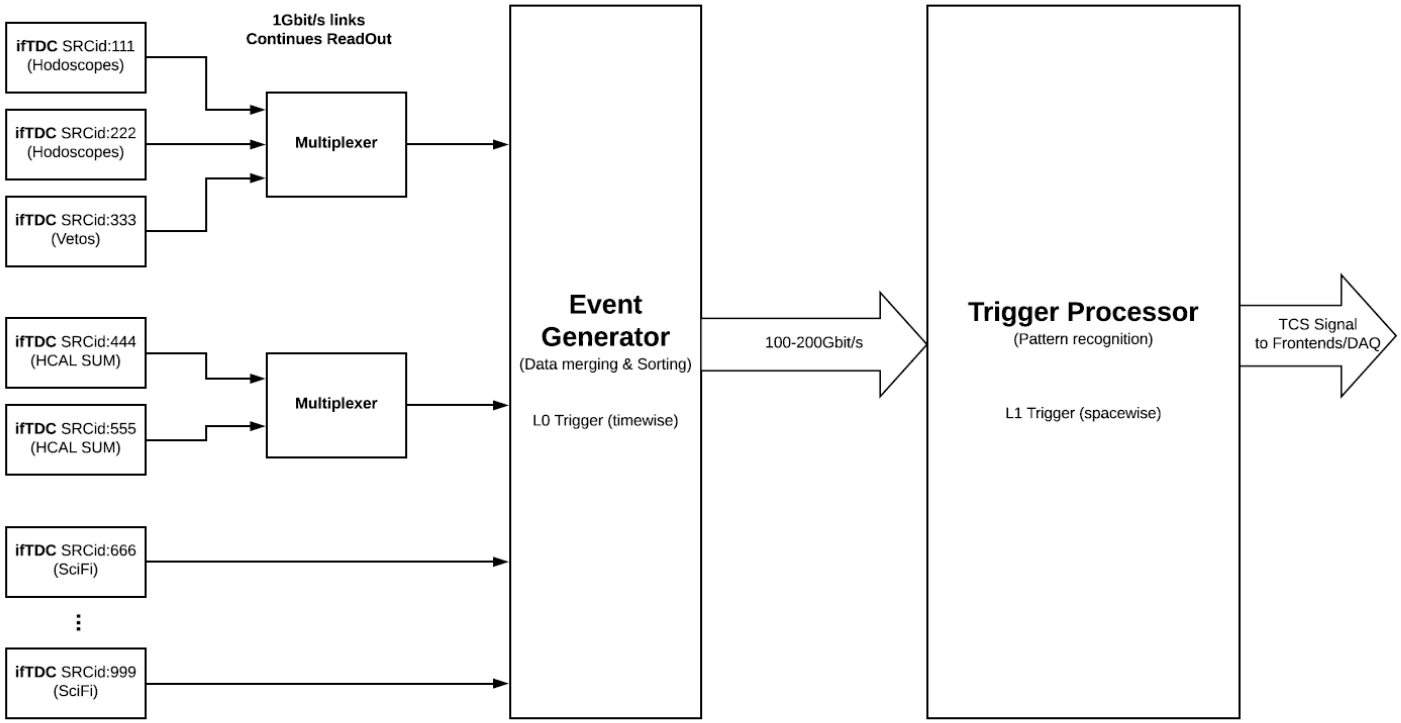
- Xilinx Kintex Ultrascale XCKU095 FPGA
- 32 GB of DDR4 memory
- 60 x 10Gb/s links
- 10 GB/s throughput
- Custom 2U 19” shelf





Trigger Processor

Possible Readout Structure



iFDAQ Framework

Improve efficiency of firmware development

- Standard serial interfaces with corresponding IP cores
  - Unified Communication Framework , first student award in RT2016
  - Time distribution interface
  - IPBUS for slow control, monitoring and diagnostics
- Standard internal interface
  - AXI stream interface, Xilinx standard
- Common front-end data format
- Set of common IP cores
  - Data consistency check
  - Chronological hit sorting
  - Data decoding
  - Diagnostic and debugging tools

Summary

- DAQ architecture : continuous DAQ with integrated trigger processor
- Triggered and non triggered operation modes
- Development of trigger less front-end electronics : iFTDC, Pixel Detector, MSADC
- RICH, MM and GEM : performance of VMM and SAMPA ASICs to be verified
- Developed concept of programmable digital trigger processor
- Scalable DAQ bandwidth from 2 GB/s to 20 GB/s
- iFDAQ FPGA framework

THANK YOU

BACKUP SLIDES

RAID Controller Performance

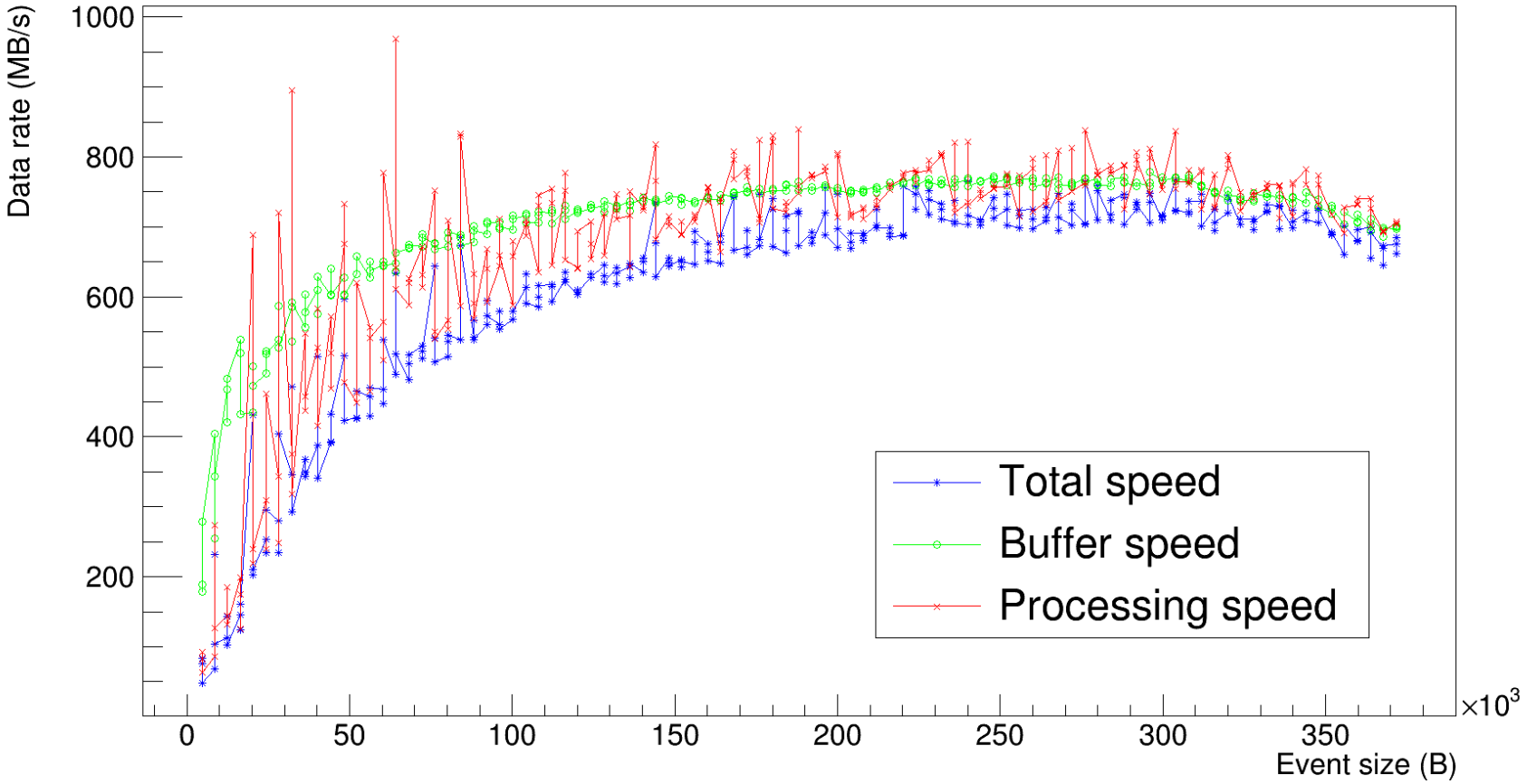
SLC6.9_64bits, 2 x Xeon E5-2620 v2 @2.1GHz, 8 HDDs

RAID Configuration	Write Speed	Read Speed	Copy Speed
RAID10, 7.2TB, ext4	500 MB/s	510 MB/s	230 MB/s
RAID0, 15TB, ext4	724 MB/s	1100 MB/s	342 MB/s
RAID5, 13TB, ext4	681 MB/s	705 MB/s	246 MB/s
RAID6, 10.9TB, ext4	577 MB/s	665 MB/s	243 MB/s
RAID0/1, disks: 0-3, 7.271TB	577 MB/s	576 MB/s	234 MB/s
RAID0/2, disks: 4-7, 7.271TB	568 MB/s	572 MB/s	228 MB/s
RAID0/1 and RAID0/2	560 MB/s	570 MB/s	415 MB/s

Increase performance to 1GB/s

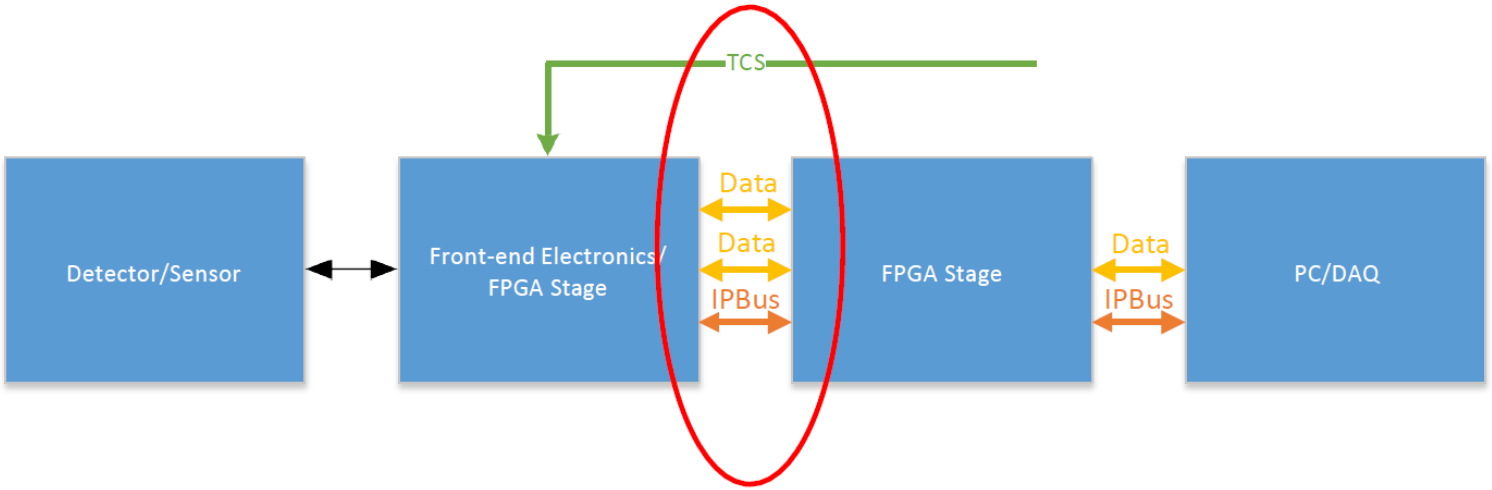
- Increase number of HDDs
- Increase number of RAID controllers

Readout Slave Process Performance



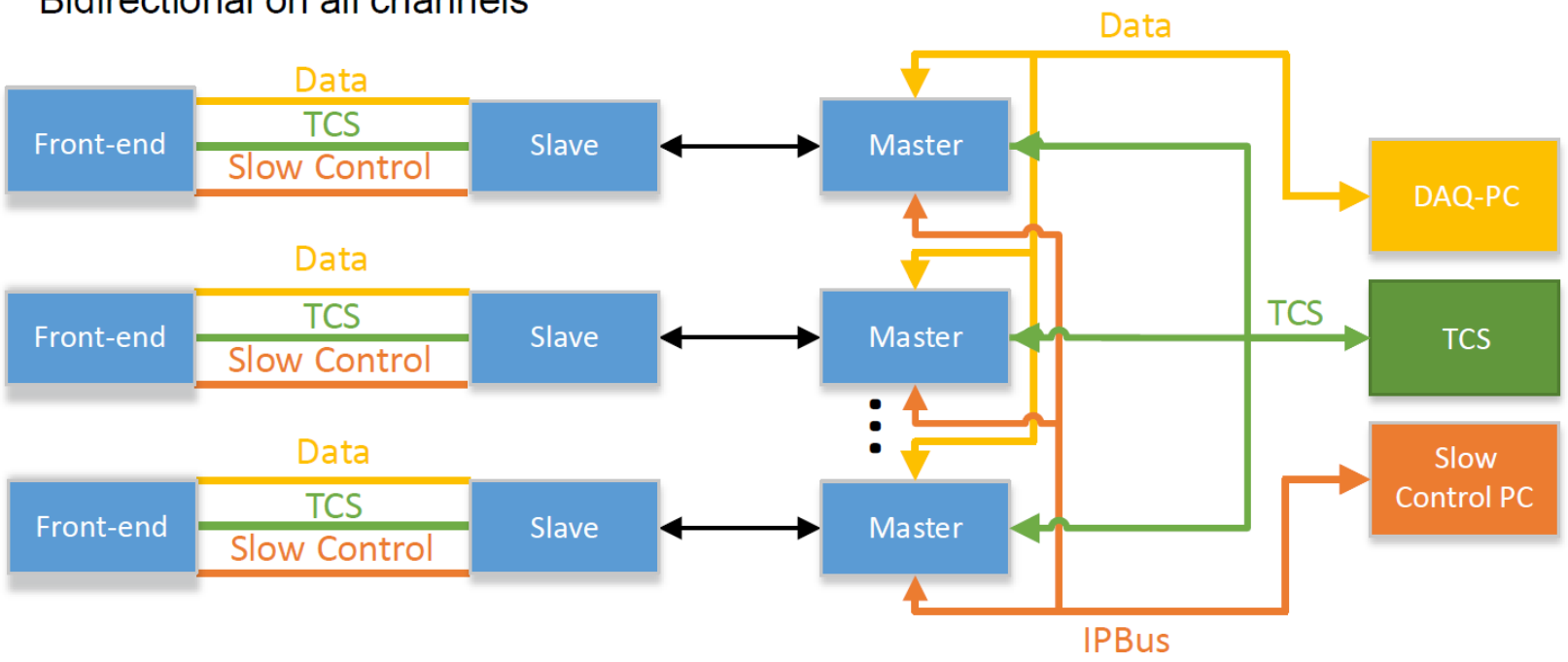
Unified Communication Framework (UCF)

- Single high-speed serial link for data, slow control, trigger, and timing information
- Up to 64 different communication channels (Trigger, Data, Ethernet)
- Fixed latency for one channel
- Priority handling for all channels
- Self recoverable after connection losses
- Independent from physical layer



UCF – Example Topologies

- Point-to-Point topology:
  - Multiple or single 1:1 connections
  - Experiments with high data rates, …
  - Bidirectional on all channels

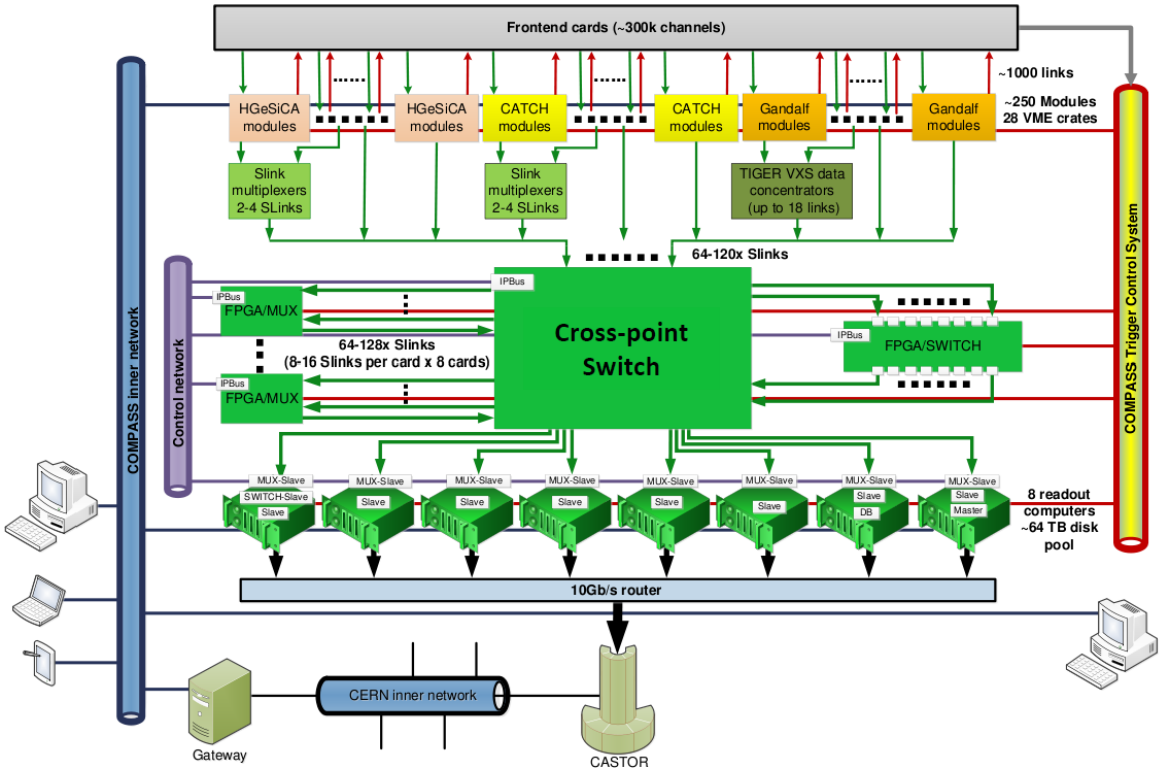


Crosspoint Switch - Integration

Cross-point Switch

- connects:
  - FE electronics
  - DHCmx modules
  - DHCsw module
  - Spillbuffers
- purpose:
  - Ease of load balancing
  - System redundancy to compensate hardware failures

⇒ provides fully customizable network topology



Crosspoint Switch – Hardware Design

Crosspoint Switch Components

- **interfaces:**
  - 12 x 12 channel CXP transceiver (MPO fiber connectors)
  - Ethernet for IPbus
  - JTAG
  - TCS (Trigger Control System) receiver
- **Switching and Control:**
  - **Vitesse VSC3144-02** – fully configurable 144x144, asynchronous, 6.5 Gbps crosspoint switch
  - **Xilinx Artix-7 FPGA** for switch control and monitoring

- **Interface FPGA – Crosswitch:**
  - 90 MHz, 11-bit parallel data bus
  - Multiple program assignments can be queued and issued simultaneously ⇒ fast programming (<< 1us)

DAQ Elements

FPGA

- Front-end electronics, detector specific
  - Conversion of detector analog signal to digital form
  - Derandomization
  - Data processing: signal detection, extraction of signals' parameters **Time** and/or **Amp…**
- Trigger Logic
  - reduce amount of stored data
  - define time of interesting event
- Trigger Distribution system => Time Distribution System
- Slow Control System
  - Control and monitoring of PS, Gas system, Temperature, Humidity,…
  - Programming of Front-ends
- Acquisition System => Event builder
  - Data acquisition – moving data from FE to PCs
  - Data flow control
  - Real time Software
  - Run control