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Overview

- COMPASS iFDAQ
- Evolution of FPGA technology
- COMPASS++/AMBER DAQ requirements
- Continuous DAQ Architecture
- Summary
COMPASS DAQ

FPGA functions
- Glue logic
- Synchronization
- Data processing
- Computer interface

Event Building

Trigger Logic

40kHz, 50kB/event
Intelligent FPGA DAQ, after upgrade 2014

FPGA functions
- Glue logic
- Synchronization
- Data processing
- Computer interface
- Event builder

40kHz, 50kB/event
2 GB/s in spill
FPGA Technology Evolution

Field Programmable Gate Array

- 2-D structure of configurable logical block
- Programmable logic and interconnections
- Allows to create very complex digital circuits, limited by number of CLBs
- Maximum frequencies up to 200-400 MHz

Additional circuits:
- Memory blocks
- DSP for integer multiplication and summation
- High bandwidth of serial links, 10 GB/s for low cost FPGA, 300 GB/s for high end FPGAs
- Support external DRAMs
FPGA Technology Evolution

<table>
<thead>
<tr>
<th>Chip</th>
<th>Manufacturer</th>
<th>Technology</th>
<th>Transistor count</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMD RYZEN 7 3750</td>
<td>AMD</td>
<td>12 nm</td>
<td>19 200 000 000</td>
</tr>
<tr>
<td>Intel XEON GOLD 6154</td>
<td>Intel</td>
<td>14 nm</td>
<td>8 000 000 000</td>
</tr>
<tr>
<td>FPGA Ultra Scale Plus</td>
<td>Xilinx</td>
<td>16 nm</td>
<td>20 000 000 000</td>
</tr>
</tbody>
</table>

- Highly parallel architecture
- Enormous IO bandwidth
- Low cost, low power
- Long development time => Software tools for a moment behind complexity of HW technology
- Intel and Xilinx apply FPGA technology for data centers

FPGA is ideal technology
for development reliable, high performant, low cost DAQ system

iFDAQ (intelligent FPGA DAQ)
Reliability achieved by smart recovery algorithms included in FPGA
Motivation for hardware event builder
- FPGA is real real-time technology
- Minimize number of real-time software processes
- Simplify software functionality \(\Rightarrow\) increase reliability
- Fast recovery time after crash

iFDAQ Framework
- Implementing congestion free Event Builder
- Intelligent data handling
- Unified Interfaces
- Unified FPGA IP Cores

Advantages
- Increased compactness
- Increased reliability
- Reduced cost
iFDAQ Architecture

FPGAs take full responsibility for reliable data transmission from FEEs to PCs

Unified interfaces:
- Slink for data transmission
- TCS for time and trigger distribution
- IPBUS for monitoring and configuration

Intelligence elements in hardware:
- Self synchronized data flow (backpressure and throttling)
- FEE Error diagnostics and handling to prevent DAQ crashes => monitoring ,
- Automatic resynchronization of FEEs
- FEEs can be attached/detached at any time
- Continuous data taking. Stop only in case of problems

DHmx, DHsw
- Virtex6 XC6V75
- 4GB, DDR3
- 16x6.5 Gb/s links
iFDAQ Up Time

Very reliable

Important updates:
- Readout slaves
- Master process
**COMPASS++/AMBER Requirements**

<table>
<thead>
<tr>
<th>Programme</th>
<th>Physics Goals</th>
<th>Beam Energy [GeV]</th>
<th>Beam Intensity [s⁻¹]</th>
<th>Trigger Rate [kHz]</th>
<th>Beam Type</th>
<th>Target</th>
<th>Hardware additions</th>
</tr>
</thead>
<tbody>
<tr>
<td>muon-proton elastic scattering</td>
<td>Precision proton-radius measurement</td>
<td>100</td>
<td>4 \cdot 10⁶</td>
<td>100</td>
<td>(\mu^\pm)</td>
<td>high-pressure H₂</td>
<td>active TPC, SciFi trigger, silicon tracking</td>
</tr>
<tr>
<td>Drell-Yan</td>
<td>Pion PDFs</td>
<td>190</td>
<td>7 \cdot 10⁴</td>
<td>50</td>
<td>(\pi^\pm)</td>
<td>C/W</td>
<td>target modification</td>
</tr>
<tr>
<td>Input for Dark Matter Search</td>
<td>(\overline{p}) production cross section</td>
<td>20-280</td>
<td>5 \cdot 10⁵</td>
<td>25</td>
<td>(p)</td>
<td>LH₂, LHe</td>
<td>liquid helium target, RICH?</td>
</tr>
</tbody>
</table>

**Challenges**

- Precision measurements => high statistics, high data rate
- Variable set of detectors
- Big variation of detector time resolutions from sub nanoseconds to 60 microseconds
- Different and complex trigger algorithms
  - PRM: Recoil proton (TPC, 60 us drift time) and scattered muon trigger (SciFi, Pixel Silicon)
  - Drell-Yan: Target pointing muon trajectories and muon multiplicity
COMPASS++/AMBER DAQ

**DAQ architecture**
- Continuous or trigger less front-end electronics with signal detection and feature extraction
  - HIT : channel ID, amplitude and/or Time Tag
  - Information from any detector can be included in trigger logic
  - Provision of big trigger latency in order of milliseconds or even seconds
  - Programmable Hardware Trigger Processor
  - Configurable DAQ topology by employing cross-switch
  - High data rate capable event builder

**Data rate**

<table>
<thead>
<tr>
<th>Programme 2022-2024</th>
<th>Beam Rate</th>
<th>Trigger rate</th>
<th>Non triggered Data Rate</th>
<th>Final Data rate limited by storage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Proton Radius Measurement</td>
<td>$2 \cdot 10^6 - 10^7$</td>
<td>100 kHz</td>
<td>10 GB/s in spill, 3GB/s sustained</td>
<td>$&lt; 2$ GB/s</td>
</tr>
<tr>
<td>Drell-Yan</td>
<td>$7 \cdot 10^7$</td>
<td>50kHz</td>
<td>30 GB/s in spill 10 GB/s sustained</td>
<td>500 MB/s</td>
</tr>
<tr>
<td>Input for Dark Matter search</td>
<td>$5 \cdot 10^5$</td>
<td>25 kHz</td>
<td>?</td>
<td>250 MB/s</td>
</tr>
</tbody>
</table>
Evolution of COMPASS DAQ Architecture

2014-2021
- ~1000 links
- ~100 SLinks
- 6 SLinks
- Event Builder
- 4 SLinks
- 4 Online WS
- 1x10Gb Eth. links
- Storage/CDR

2022
- Front-End
- Trigger Processor
- ~1000 UCF links
- 10-20 UCF links
- Event Builder
- 2-20 UCF links
- 2 - 20 Online WS
- 2x10Gb Eth. links
- Storage/CDR
Serial link bandwidth is 10 Gb/s (1GB/s)
Event builder is scalable to 20 GB/s sustained data rate
Expected single PC bandwidth 1GB/s
Data Structure of Continuous DAQ

For 2022 it’s foreseen to collect data in untriggered mode
Time Slice => Event
Sustained data rate is limited to 2GB/s by Central Data Recording
Data Structure of Continuous DAQ

<table>
<thead>
<tr>
<th>Very slow Detectors (TPC, ...)</th>
<th>Slow Detectors (DCs, W45, ...)</th>
<th>Fast Detectors (Hodoscopes, SciFi, ...)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Slice 1</strong> 15kHz</td>
<td><strong>Slice 2</strong> 10kHz</td>
<td>*<em>Slice 2^<em>20</em></em> 10kHz</td>
</tr>
<tr>
<td>Image 1 500ns</td>
<td>Image 2 500ns</td>
<td>Image 1 500ns</td>
</tr>
<tr>
<td>Image 200 500ns</td>
<td>Image 200 500ns</td>
<td>Image 200 500ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>Spill</strong></td>
</tr>
</tbody>
</table>
Triggering

SciFi
GATE 25 ns

Si, MM, GEM
GATE 50 ns

Drift Chambers
GATE 400 ns

TPC
GATE 60 us
Triggering

SciFi
GATE 25 ns

Si, MM, GEM
GATE 50 ns

Drift Chambers
GATE 400 ns

TPC
GATE 60 us

Triggered mode will be employed in 2023
FRONT-END ELECTRONICS
## COMPASS++/AMBER Detectors and FEE

<table>
<thead>
<tr>
<th>Detectors</th>
<th>Front-Ends</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SciFi, BMS, Hodoscopes</td>
<td>iFTDC, 200/400 ps</td>
<td>FW upgrade</td>
</tr>
<tr>
<td>CEDAR</td>
<td>iFTDC, 200 ps</td>
<td>FW upgrade</td>
</tr>
<tr>
<td>DC, Straw, MWPC, MW</td>
<td>iFTDC, 800 ps</td>
<td>FW upgrade</td>
</tr>
<tr>
<td>TPC</td>
<td>FADC, 14 bit 250 MHz</td>
<td>ready</td>
</tr>
<tr>
<td>Silicon Pixel</td>
<td>MuPix10</td>
<td>prototype</td>
</tr>
<tr>
<td>HCAL, ECAL</td>
<td>MSADC, 12 bit 80 MHz</td>
<td>HW and FW upgrade</td>
</tr>
<tr>
<td>RICH, MM, GEM</td>
<td>VVM, SAMPA</td>
<td>performance to be evaluated</td>
</tr>
</tbody>
</table>
iFTDC

- ARTIX7 FPGA
- TDC implemented in FPGA using built-in SERDES (serialized/deserializer) circuit
- Firmware versions
  - 64 channels 0.8/0.4 ns bin, 0.25/0.14 ns resolution
    - 2xSERDES/channel, half bin shift
  - 32 channels 0.2 ns bin, 80 ps resolution, 40% DNL
    - 4xSERDES/channel, ¼ bin shift
  - 4 ns dead time
  - Low hit rate version, maximum 5 MHz/channel
  - High hit rate version, maximum 80 MHz/channel
- Up to 4 UCF interfaces for very high hit rate conditions
- Ethernet interface for lab setups
iFTDC

Differential non linearity

- 1 ns/bin < 10%
- 0.4 ns/bin < 25%
- 0.2 ns/bin < 50%

Built-in functionality:

- Hit rate counter, accessed via slow control interface
- Data rate measurement with data taking

TDC bin size variation, DNL

Example of CEDAR pressure scan
MSADC Upgrade

- 16 channel 12 bit @80 MHz
- Upgrade to Kintex/Zink FPGA, 2020
- Baseline follower pedestal and RMS calculation, programmable number of samples

\[ \Sigma_{\text{ped}} = \Sigma_{\text{ped}} + s_i - \bar{s}, \quad \bar{s} = \Sigma_{\text{ped}} / N \]

\[ \Sigma_{\text{diff}} = \Sigma_{\text{diff}} + (s_i - \bar{s})^2 - \sigma^2, \quad \sigma^2 = \Sigma_{\text{diff}} / N \]

- Advanced Signal processing in FPGA for signal detection and feature extraction down to SNR ~ 3
  (Warsaw TU, Trieste INFN/ICTP)
MuPix8 CMOS Monolithic Pixel Detector

- From Heiko Augistin talk, Mu3e collaboration
- Monolithic Silicon pixel detector MuPix8
  - Developed by Karlsruhe IT, Ivan Peric group
  - 80x81 µm² pixel size, thinned down to 62.5 µm
  - 1x1.6 cm² active, 128x200 pixels
  - MuPix10 => 2x2 cm²
  - Trigger less read out
2 thresholds
32 bit/hit, row address, column address, Time Tag, ToT
3 high speed links 1.25 Gb/s
1 us dead time/pixel
48x200 pixels connected to HS link => 10 Mhits/s
DAQ/Trigger Processor Hardware

New DAQ FPGA Switch
- Xilinx Kintex Ultrascale XCKU095 FPGA
- 32 GB of DDR4 memory
- 60 x 10Gb/s links
- 10 GB/s throughput
- Custom 2U 19” shelf
Trigger Processor

Possible Readout Structure

IHTDC SRCid 111 (Hodoscopes)
IHTDC SRCid 222 (Hodoscopes)
IHTDC SRCid 333 (Vetos)
IHTDC SRCid 444 (HCAL SUM)
IHTDC SRCid 555 (HCAL SUM)
IHTDC SRCid 666 (SciFi)
... 
IHTDC SRCid 999 (SciFi)

Event Generator
(Data merging & Sorting)
1.0 Trigger (time wise)

1Gbit/s links
Continues ReadOut

Multiplexer

Trigger Processor
(Pattern recognition)
L1 Trigger (space wise)

100-200Gbit/s

TCS Signal
to Frontends/DAQ
iFDAQ Framework

Improve efficiency of firmware development

- Standard serial interfaces with corresponding IP cores
  - Unified Communication Framework, first student award in RT2016
  - Time distribution interface
  - IPBUS for slow control, monitoring and diagnostics
- Standard internal interface
  - AXI stream interface, Xilinx standard
- Common front-end data format
- Set of common IP cores
  - Data consistency check
  - Chronological hit sorting
  - Data decoding
  - Diagnostic and debugging tools
Summary

- DAQ architecture: continuous DAQ with integrated trigger processor
- Triggered and non-triggered operation modes
- Development of trigger less front-end electronics: iFTDC, Pixel Detector, MSADC
- RICH, MM and GEM: performance of VMM and SAMPA ASICs to be verified
- Developed concept of programmable digital trigger processor
- Scalable DAQ bandwidth from 2 GB/s to 20 GB/s
- iFDAQ FPGA framework
THANK YOU
BACKUP SLIDES
RAID Controller Performance

SLC6.9_64bits, 2 x Xeon E5-2620 v2 @2.1GHz, 8 HDDs

<table>
<thead>
<tr>
<th>RAID Configuration</th>
<th>Write Speed</th>
<th>Read Speed</th>
<th>Copy Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>RAID10, 7.2TB, ext4</td>
<td>500 MB/s</td>
<td>510 MB/s</td>
<td>230 MB/s</td>
</tr>
<tr>
<td>RAID0, 15TB, ext4</td>
<td>724 MB/s</td>
<td>1100 MB/s</td>
<td>342 MB/s</td>
</tr>
<tr>
<td>RAID5, 13TB, ext4</td>
<td>681 MB/s</td>
<td>705 MB/s</td>
<td>246 MB/s</td>
</tr>
<tr>
<td>RAID6, 10.9TB, ext4</td>
<td>577 MB/s</td>
<td>665 MB/s</td>
<td>243 MB/s</td>
</tr>
<tr>
<td>RAID0/1, disks: 0-3, 7.271TB</td>
<td>577 MB/s</td>
<td>576 MB/s</td>
<td>234 MB/s</td>
</tr>
<tr>
<td>RAID0/2, disks: 4-7, 7.271TB</td>
<td>568 MB/s</td>
<td>572 MB/s</td>
<td>228 MB/s</td>
</tr>
<tr>
<td>RAID0/1 and RAID0/2</td>
<td>560 MB/s</td>
<td>570 MB/s</td>
<td>415 MB/s</td>
</tr>
</tbody>
</table>

Increase performance to 1GB/s
- Increase number of HDDs
- Increase number of RAID controllers
Readout Slave Process Performance

![Graph showing data rate (MB/s) vs. event size (B) with different lines representing Total speed, Buffer speed, and Processing speed.]
Unified Communication Framework (UCF)

- Single high-speed serial link for data, slow control, trigger, and timing information
- Up to 64 different communication channels (Trigger, Data, Ethernet)
- Fixed latency for one channel
- Priority handling for all channels
- Self recoverable after connection losses
- Independent from physical layer
UCF – Example Topologies

- Point-to-Point topology:
  - Multiple or single 1:1 connections
  - Experiments with high data rates, …
  - Bidirectional on all channels
Crosspoint Switch - Integration

Cross-point Switch

- **connects:**
  - FE electronics
  - DHCmx modules
  - DHCsw module
  - Spillbuffers

- **purpose:**
  - Ease of load balancing
  - System redundancy to compensate hardware failures

⇒ provides fully customizable network topology
Crosspoint Switch – Hardware Design

Crosspoint Switch Components

- **interfaces:**
  - 12 x 12 channel CXP transceiver (MPO fiber connectors)
  - Ethernet for IPbus
  - JTAG
  - TCS (Trigger Control System) receiver

- **Switching and Control:**
  - Vitesse VSC3144-02 – fully configurable 144x144, asynchronous, 6.5 Gbps crosspoint switch
  - Xilinx Artix-7 FPGA for switch control and monitoring

- **Interface FPGA – Crosswitch:**
  - 90 MHz, 11-bit parallel data bus
  - Multiple program assignments can be queued and issued simultaneously ⇒ fast programming (<< 1us)
DAQ Elements

- Front-end electronics, detector specific
  - Conversion of detector analog signal to digital form
  - Derandomization
  - Data processing: signal detection, extraction of signals' parameters **Time** and/or **Amp**

- Trigger Logic
  - reduce amount of stored data
  - define time of interesting event

- Trigger Distribution system => **Time Distribution System**

- Slow Control System
  - Control and monitoring of PS, Gas system, Temperature, Humidity,…
  - Programming of Front-ends

- Acquisition System => **Event builder**
  - Data acquisition – moving data from FE to PCs
  - Data flow control
  - Real time Software
  - Run control