The iFDAQ of COMPASS -
An intelligent, FPGA-based event builder as an example for the future?

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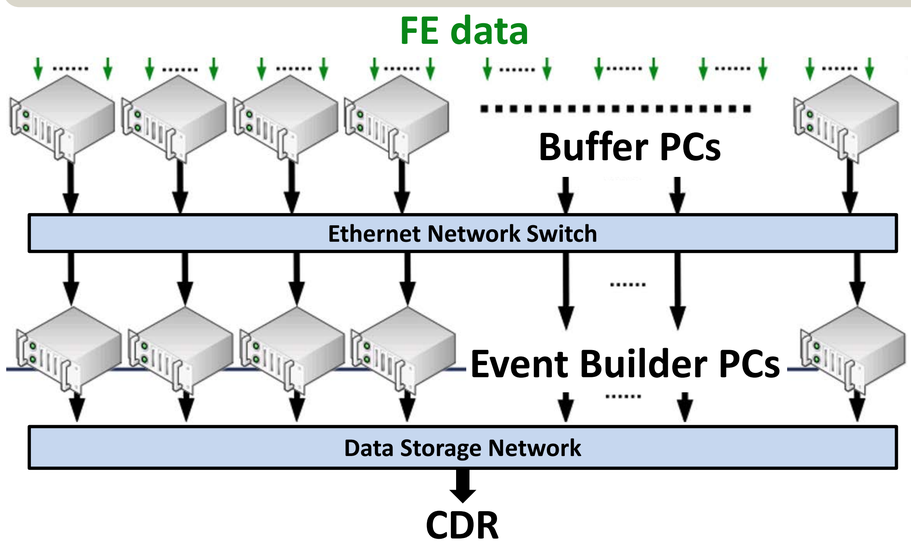
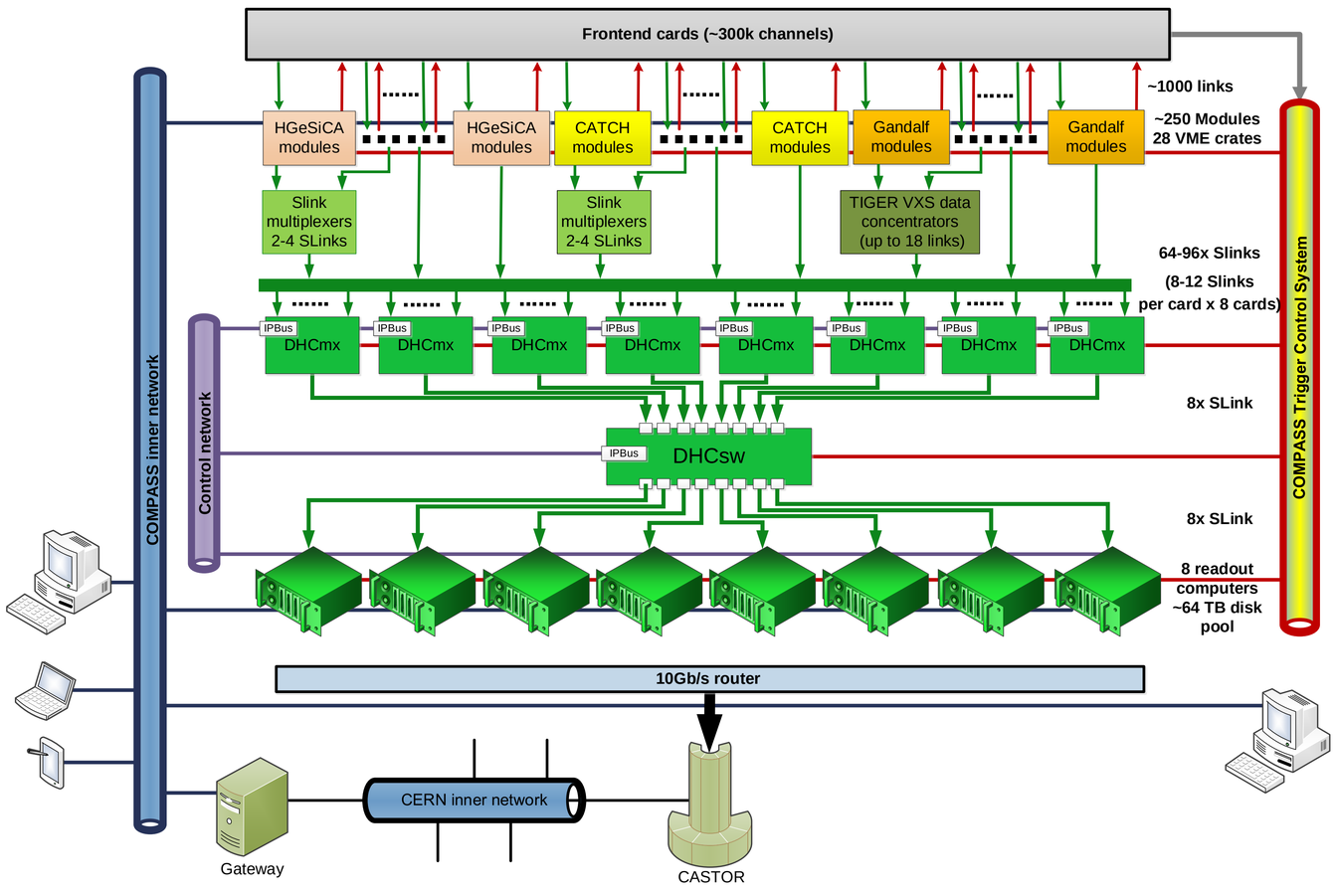
Hardware Event Building

"Traditional" Event Building



Hardware Event Builder of iFDAQ



Properties of iFDAQ

Built-in intelligence:
- Self Diagnostics
- Data check/FE-error handling
- Redundancy & self-reconfiguration (development) => Continuous data taking

- On-spill data rate: 1.5 GB/s
- Buffering on all levels of event buiding
  - ↳ 500 MB/s sustained rate
- 3 independent interfaces:
  - o Time distribution (TCS)
  - o Data flow (SLINK)
  - o Slow control (IPbus)

FPGA Modules of iFDAQ

Data Handling Card (DHC)

form factor: μTCA / AMC standard
6U VME carrier card

FPGA: Xilinx Virtex6

memory: 4GB DDR3 SDRAM

firmware:
- o **DHCmx** (12:1 multiplexer)
- o **DHCsw** (8x8 switch)
- o **DHCsb** (PCIe spillbuffer)

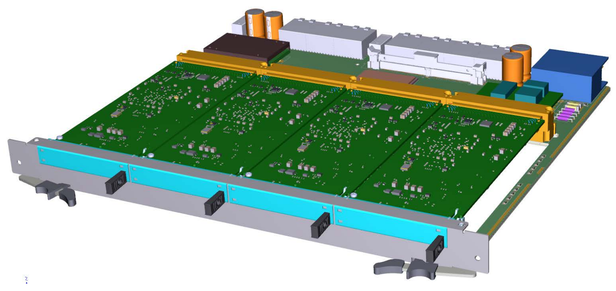
interfaces:
- TCS (Trigger Control System)
- 1 Gb Ethernet control network (IPbus)
- 16 serial data links (SLINK)
- PCIe (for spillbuffer)

throughput: 3 GB/s as DHCsw

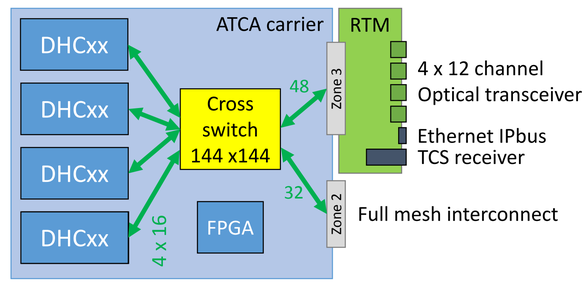
DHC on VME carrier Card as used for DHCmx and DHCsw

DHC as used for DHCsb

Future Upgrades – ATCA and crosspoint switch



- 4 DHC per carrier card
- 3 carrier cards
  => 12 AMC slots
- Interconnection via full mesh
- Integration of spare resources
- IPMC – Intelligent Platform Management Controller (ATLAS, xTCA Interest Group)

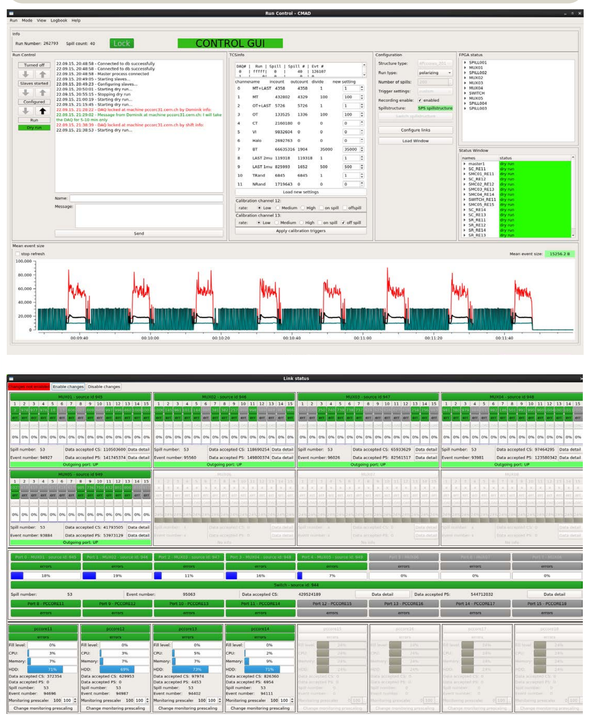


crosspoint switch: Vitesse – VSC3144-02
- fully programmable

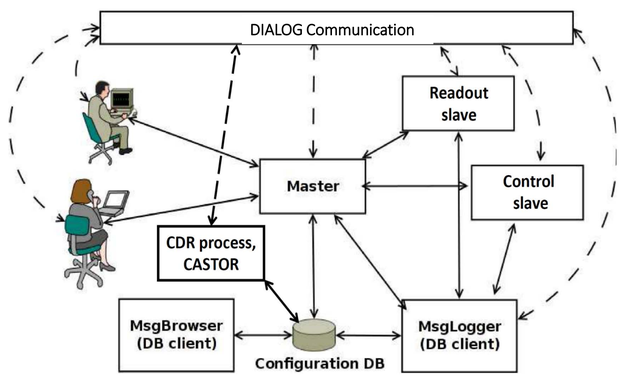
FPGA: Xilinx Artix-7
- cross switch control and monitoring
- Hub to AMC modules

Software Tools

Run Control GUI



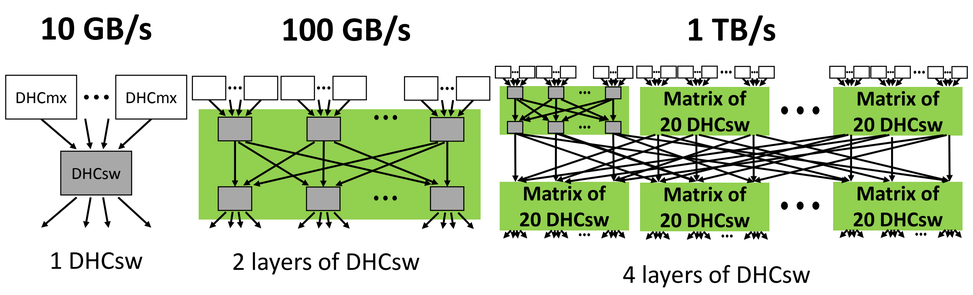
RCCAR-Software

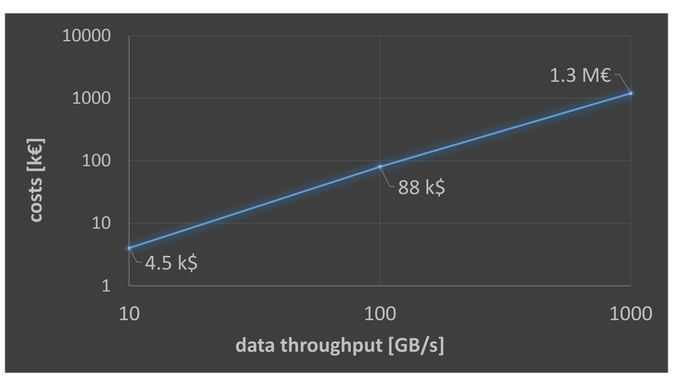


- Control of DAQ configuration through web and C++ GUI
- Multithreaded event processing and error detection
- DAQ status monitoring and system overview

Scaling of Hardware EB

Scaling Possibilities & Costs





Scenario for:
- Xilinx **7-series FPGA**
- SLINK interfaces replaced by **Aurora**

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