

TWEPP 2015:

Overview and Future Developments of the FPGA-based DAQ of COMPASS

Y. Bai, M. Bodlak, V. Frolov, V. Jary, S. Huber, I. Konorov, D. Levit,
J. Novy, R. Salac, D. Steffen and M. Virius

01.10.2015

sponsored by:



Federal Ministry
of Education
and Research



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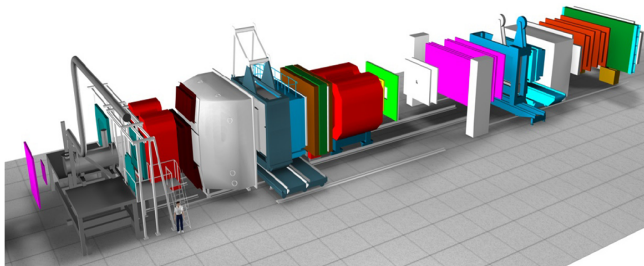
- 1 Introduction**
- 2 Design of the new DAQ**
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- 3 Setup and Performance in 2014/2015**
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COMPASS - Overview



Common
Muon
Proton
Apparatus for
Structure and
Spectroscopy

- ▷ Fixed target experiment at SPS accelerator at CERN (M2 beamline)
- ▷ High intensity beams: $4 \cdot 10^7 \frac{\mu}{s}$; $2 \cdot 10^7 \frac{\text{hadrons}}{s}$
- ▷ Start of data-taking: 2001
- ▷ Since 2012: Upgrade to COMPASS-II
- ▷ Since 2014: New DAQ with hardware event-builder (FDAQ)



Source: [1]

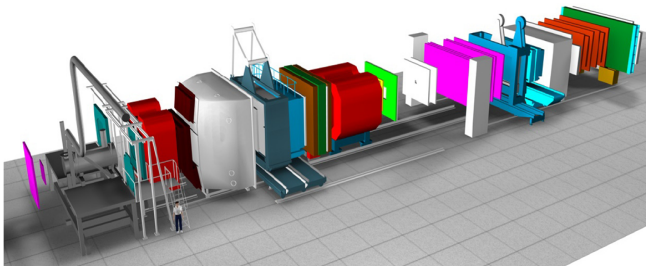
COMPASS - Overview



spectrometer facts:

- ▷ Length: 60m
- ▷ Amount of channels: 300.000
- ▷ Trigger rate: 30 kHz
- ▷ On-spill data rate: 1.5 GB/s
- ▷ Event size: 20-50 kB

- ▷ Fixed target experiment at SPS accelerator at CERN (M2 beamline)
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Design of the new DAQ - Hardware

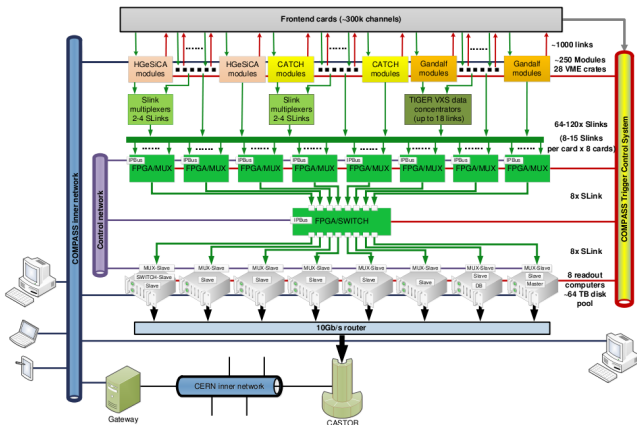


Frontends

- ▷ ~ 100 HOLA SLINKS
- ▷ peak data rate after trigger:
~ 8 GB/s

Hardware event builder

- ▷ consists of:
 - 8 new DHC modules as mux
 - 1 new DHC module as switch
 - 8 spillbuffer cards in readout computers
- ▷ 3 independent networks for
 - synchronization ⇒ (TCS)
 - data flow → event building (SLINK)
 - configuration and data flow control (IPBus)
- ▷ data buffering on different levels: theoretical max. 20 GB/spill ⇒ 1.0 GB/s sustained data rate



Sources: [3, 5, 7]

Hardware Based Event Building

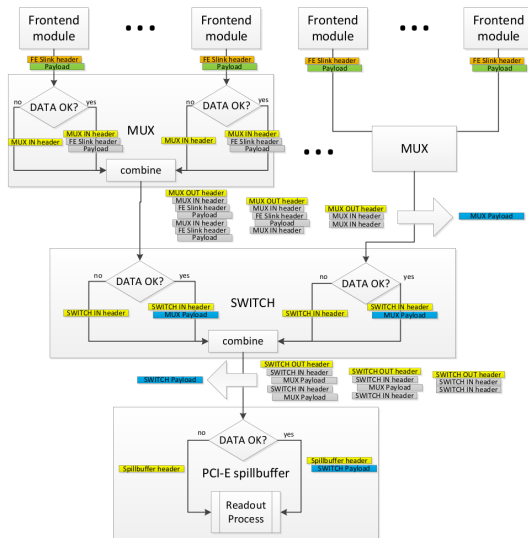


▷ On each layer:

- Verification of data
- Discarding of wrong data
- Adding of layer-specific header

▷ Readout process:

- Decoding of data
- Transformation of data into output format (DATE)



Source: [6]

Data Handling Card (DHC)



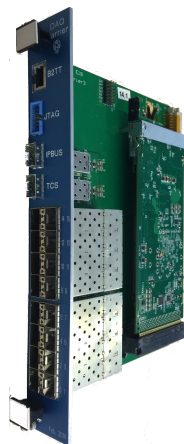
Carrier Card

- ▷ **form factor:** 6 U VME
- ▷ **interfaces:**
 - TCS (Trigger Control System) receiver
 - 1 Gb Ethernet for control network (IPBus)
 - 16 serial data links (SLINK)
 - JTAG for programming FLASH (after via IPBus)

AMC module

- ▷ **form factor:** AMC standard
⇒ compatible to ATCA
- ▷ **FPGA:** Virtex6 XC6VLX130T
- ▷ **memory:** 4 GB DDR3
- ▷ **firmware:** DHCmx 15:1 or DHCsw 8x8
- ▷ **data rate:** 3 GB/s throughput

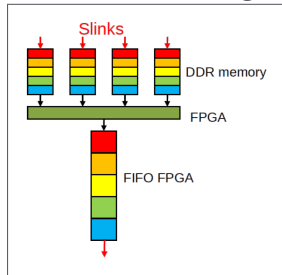
DAQ unit
 ≡
carrier card + DHCxx



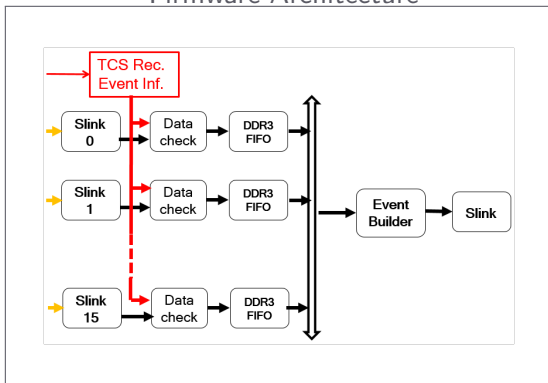
Firmware - DHCmx



Subevent building



Firmware Architecture

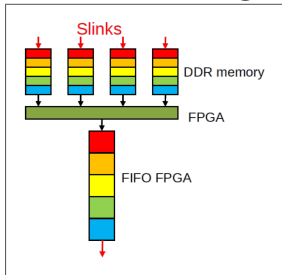


- ▷ memory interface optimized to use full bandwidth of SDRAM (6.4 GB/s)

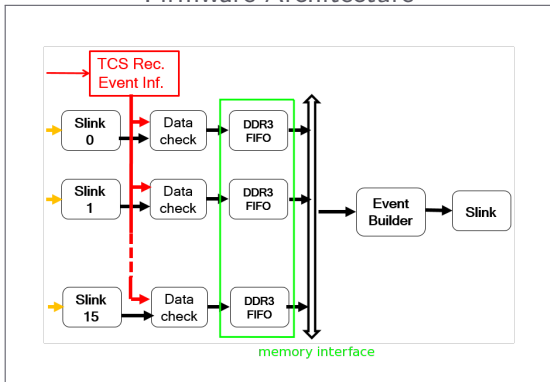
Firmware - DHCmx



Subevent building



Firmware Architecture

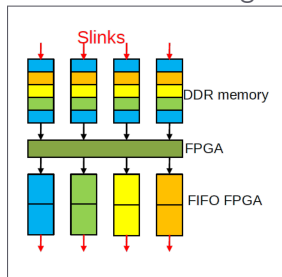


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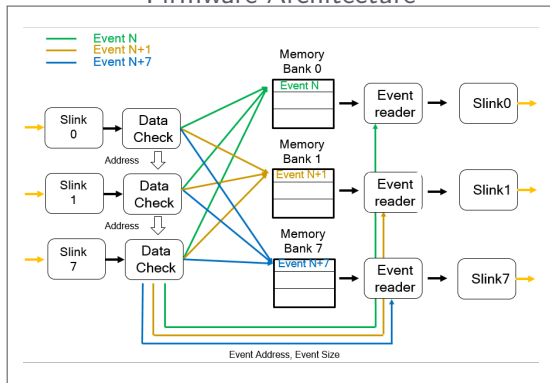
Firmware - DHCsw



Subevent building



Firmware Architecture



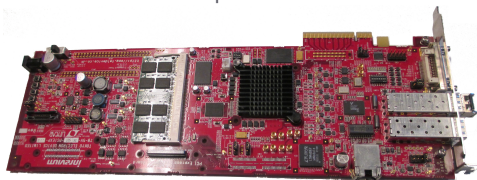
- ▷ size of memory bank: 0.5 MB = max. possible event size in COMPASS

COMPASS FDAQ - Hardware Parts

Hardware Event Builder



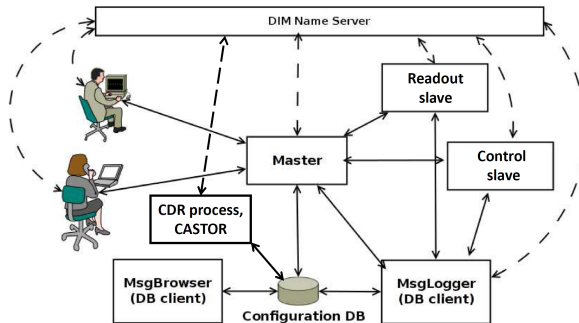
PCI-E spillbuffer card



Readout Computers



Design of the new DAQ - Software



Used Technologies

▷ DIM

server/client communication between processes

▷ Qt5

used for all processes in DAQ - speed up of the development process

▷ MySQL

database management system

▷ PHP and javascript

webconfiguration of DAQ

▷ bash and Python

support scripts

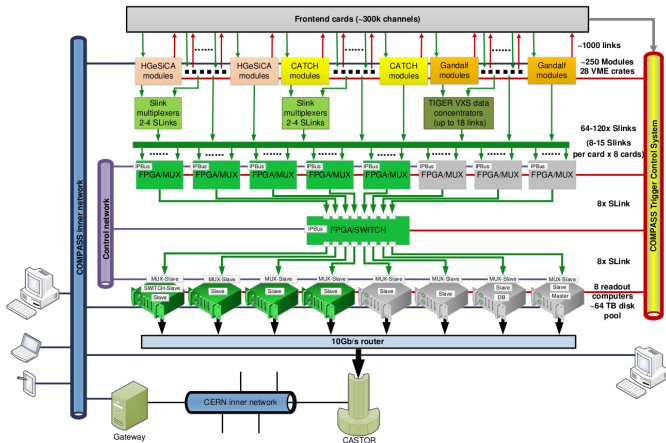
Sources: [2]

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Drell-Yan DAQ Setup (2014/2015)



- ▷ 5 DHCmx
- ▷ 1 DHCsw
- ▷ 4 readout engines



Summary of Run 2015



Accomplished data rates:

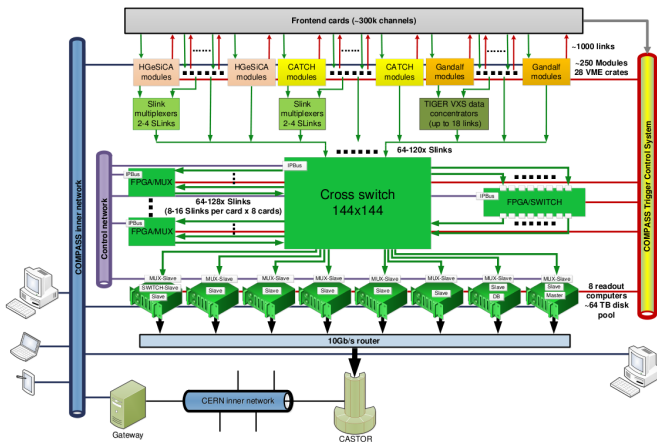
- ▷ **on-spill data rate:** 600 MB/s
- ▷ **sustained data rate:** 200-250 MB/s
- ▷ **input rate to DHCsw:** ~ 1 GB/s
- ▷ **output rate from DHCsw:** 400 MB/s

Conclusion:

- ▷ DAQ system commissioned at nominal conditions for Drell-Yan
- ▷ Run successful \rightarrow quite stable DAQ operation
- ▷ Observed problems: (1-2 times per day)
 - problems caused by certain errors in FE data format
 - wrong subevents merged into one event
 - crash of DAQ process

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Future Developments - Crosspoint Switch



▷ connects:

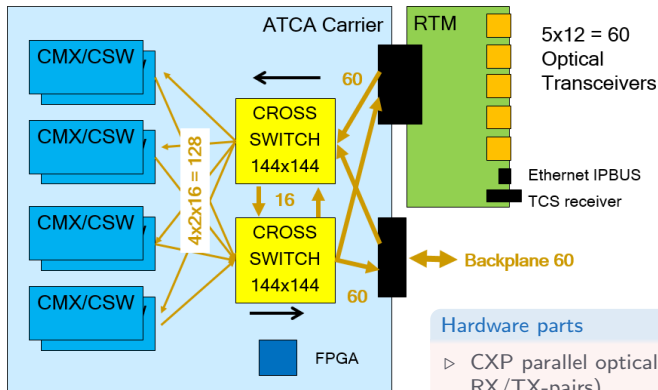
- FE electronics
- DHC MUXs
- DHC SWITCH
- spillbuffers

▷ purpose:

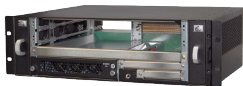
- load balancing
- system redundancy to compensate hardware failures

⇒ provides fully customizable DAQ network topology!

Crosspoint Switch - Schematic



ATCA shelf for two modules



Full mesh interface
 \Rightarrow 60 links between both modules

Hardware parts

- ▷ CXP parallel optical transceiver (12 RX/TX-pairs)
- ▷ Vitesse - VSC3144-02 crosspoint switch
- ▷ Xilinx Artix-7 XC7A200T for crossswitch control and DHC communication
 - UCF = Universal Communication Framework
 - for star-like network topology (1:1,1:n)
 - subchannels: data transmission, IPBus, TCS, JTAG
 - for more information: poster 21 [4]

Sources: [8, 4]

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Comparison with old DAQ



- ▷ More compact hardware → HW EB fits into one VME crate
- ▷ High reliability
- ▷ Tolerates FE errors → actively used by collaborators to debug and test new detectors
- ▷ user friendly Run Control GUI → less experience from shift crew
- ▷ Higher data rate → up to 1 GB/s sustained

Conclusion



- ▷ FDAQ commissioned in 2014
- ▷ FDAQ runs successful in 2015
- ▷ Minor problems to be fixed
- ▷ Long-term plans:
 - development and integration of the crosspoint switch
 - continuously running and self-recovering DAQ

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References I



- [1] P. Abbon et al.
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- [2] Martin Bodlák et al.
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- [3] Martin Bodlák et al.
FPGA based data acquisition system for COMPASS experiment.
volume 02009, page 8, 2013.
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- [5] Alexander B. Mann, Igor Konorov, Florian Goslich, and Stephan Paul.
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References II



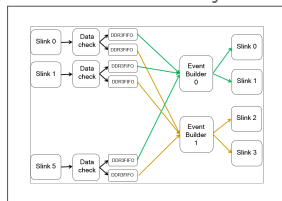
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- [7] Josef Novy et al.
New data acquisition system for the COMPASS experiment.
In *Top. Work. Electron. Part. Phys.*, 2012.
- [8] Vitesse.
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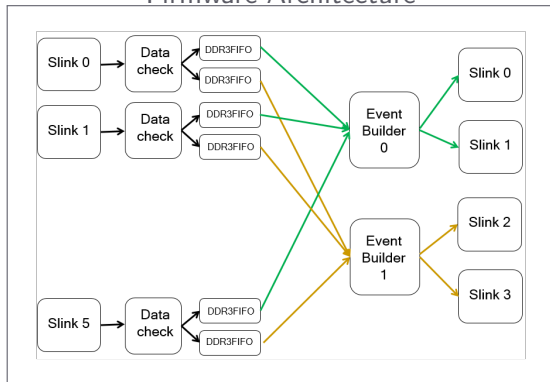
Backup - Current FW for DHCsw



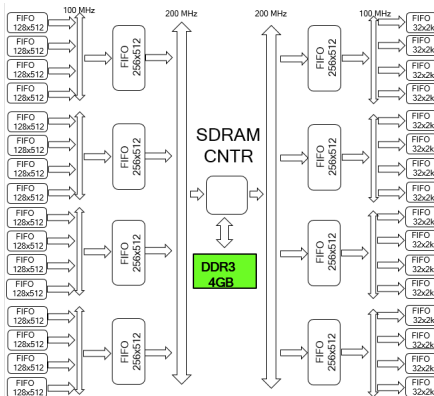
Functionality



Firmware Architecture



DHCmx - Memory Interface



- ▷ design optimized to use full bandwidth of SDRAM (6.4 GB/s)
- ▷ finite logic resources ⇒ double-layer multiplexer
- ▷ priority for incoming streams

Run Control GUI



Run Control - CMAD

Run Mode View Logbook Help

Run Number: 262793 Spill count: 40 **Lock** **CONTROL GUI**

Run Control

Turned off

Slaves started

Configured

Run

Dry run

22.09.15, 20:48:58 - Connected to db successfully
 22.09.15, 20:48:58 - Connected to db successfully
 22.09.15, 20:48:58 - Master process connected
 22.09.15, 20:49:05 - Starting slaves...
 22.09.15, 20:49:23 - Configuring slaves...
 22.09.15, 20:50:01 - Starting dry run...
 22.09.15, 20:55:15 - Stopping dry run...
 22.09.15, 21:00:19 - Starting dry run...
 22.09.15, 21:15:45 - Starting dry run...
 22.09.15, 21:28:22 - DMO locked at machine pccor31.cern.ch by Dominik info:
 the DAQ for 5-10 min only
 22.09.15, 21:29:02 - Message from Dominik at machine pccor31.cern.ch: I will take
 the DAQ for 5-10 min only
 22.09.15, 21:38:59 - DMO locked at machine pccor31.cern.ch by shft info:
 22.09.15, 21:38:53 - Starting dry run...

Name:

Message:

Send

TCInfo

DAQ	Run	Spill	Spill #	Evt #
0	fffff	0	40	126187
1	---	MT	---	---

channelname	incount	outcount	divide	new setting
0	MT+LAST	4358	4358	1
1	MT	432802	4329	100
2	OT+LAST	5726	5726	1
3	OT	133525	1336	100
4	CT	2160180	0	0
5	VI	9832604	0	0
6	Halo	2692763	0	0
7	BT	66635316	1904	35000
8	LAST 2mu	119318	119318	1
9	LAST 1mu	825993	1652	500
10	TRand	6845	6845	1
11	NRand	1739643	0	0

Load new settings

Calibration channel 12:
 rate: Low Medium High on spill off spill

Calibration channel 13:
 rate: Low Medium High on spill off spill

Apply calibration triggers

Configuration

Structure type: **4fcorus_2015**

Run type: **polarizing**

Number of spills: **200**

Trigger settings: **custom**

Recording enabled: enabled

Spillstructure: **SPS.spillstructure**

Switch spillstructure

Configure links

Load Window

FXGA status

- SPILL001
- MUX01
- SPILL002
- MUX02
- MUX03
- MUX04
- SWTCH
- MUX05
- SPILL004
- SPILL003

Status Window

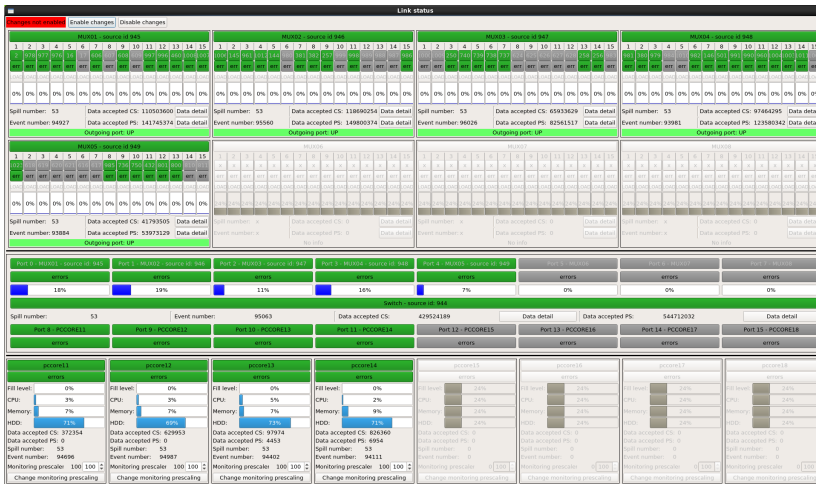
names	status
master3	dry run
SC_RE11	dry run
SMC01_RE11	dry run
SC_RE12	dry run
SMC02_RE12	dry run
SMC03_RE13	dry run
SMC04_RE14	dry run
SWTCH_RE11	dry run
SMC05_RE15	dry run
SC_RE14	dry run
SC_RE13	dry run
SR_RE11	dry run
SR_RE12	dry run
SR_RE14	dry run
SR_RE13	dry run

Mean event size

stop refresh

Mean event size: **15256.2 B**

DAQ overview Window

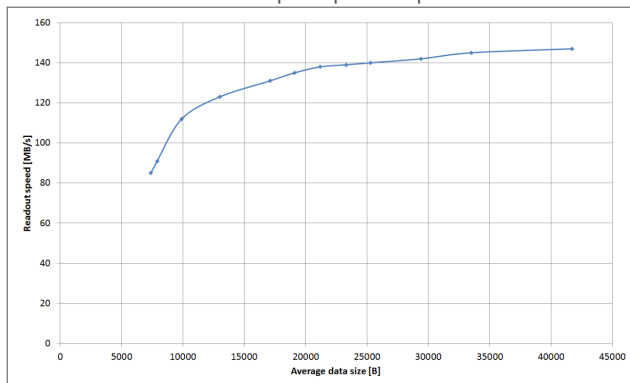


Backup - Speed tests in 2015



- ▷ Readout process only realtime process \Rightarrow limiting readoutspeed
- ▷ Test of readout speed with 2 computer setup:
 - \Rightarrow extrapolated total speed of whole setup: ~ 1.2 GB/s (still needs verification)

Readout speed per computer



Sources: [6]

ATCA-based Event Builder



ATCA shelf



Full mesh interface \Rightarrow 60 links between two modules

ATCA Standard

Zone 1:

Power management

Zone 2:

Data interface (Full mesh)

Zone 3:

Rear Panel Interconnect
(Rear Transition Module)

