TWEPP 2015:

Overview and Future Developments of the FPGA-based DAQ of COMPASS

Y. Bai, M. Bodlak, V. Frolov, V. Jary, S. Huber, I. Konorov, D. Levit, J. Novy, R. Salac, **D. Steffen** and M. Virius

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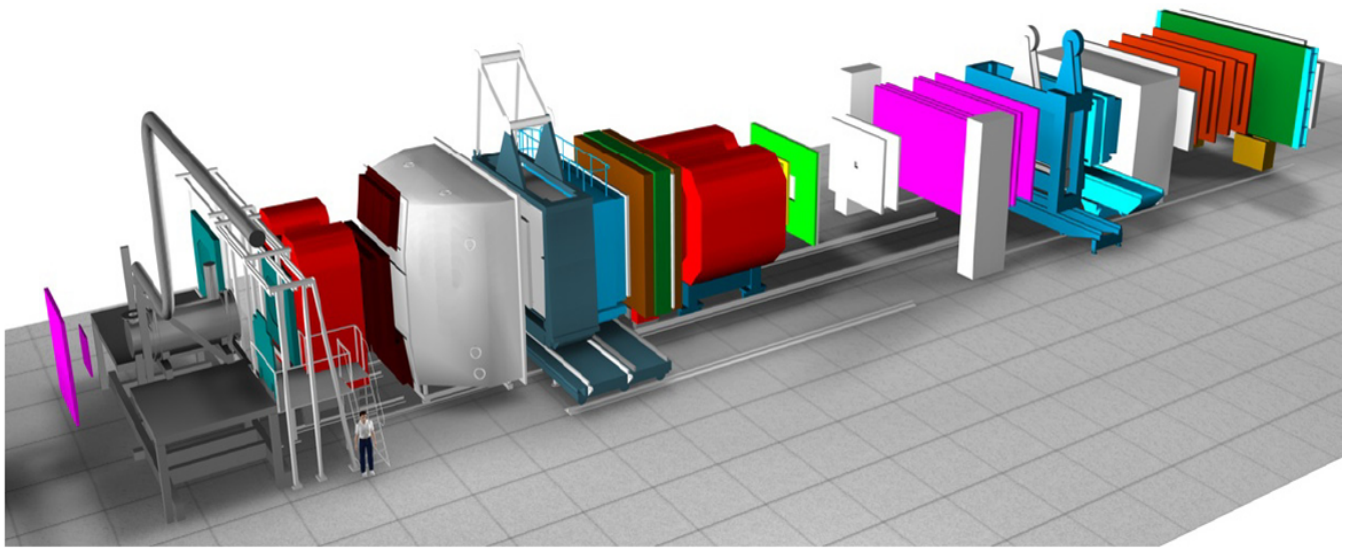
Contents

COMPASS - Overview

COmmon
Muon
Proton
Apparatus for
Structure and
Spectroscopy

- ▷ Fixed target experiment at SPS accelerator at CERN (M2 beamline)
- ▷ High intensity beams: $4 \cdot 10^7 \frac{\mu}{\mathrm{s}}$; $2 \cdot 10^7 \frac{\mathrm{hadrons}}{\mathrm{s}}$
- ▷ Start of data-taking: 2001
- ▷ Since 2012: Upgrade to COMPASS-II
- ▷ Since 2014: New DAQ with hardware event-builder (FDAQ)



Source: [1]

COMPASS - Overview

spectrometer facts:

- Length: 60m
- Amount of channels: 300.000
- Trigger rate: 30 kHz
- On-spill data rate: 1.5 GB/s
- Event size: 20-50 kB

- Fixed target experiment at SPS accelerator at CERN (M2 beamline)
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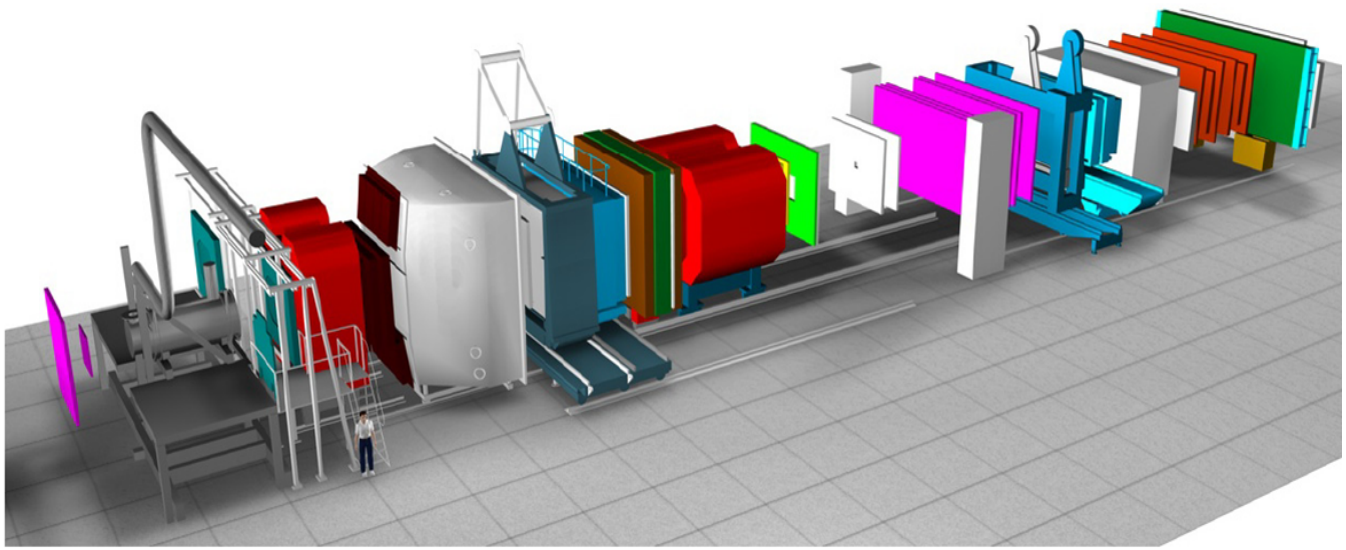


Source: [1]

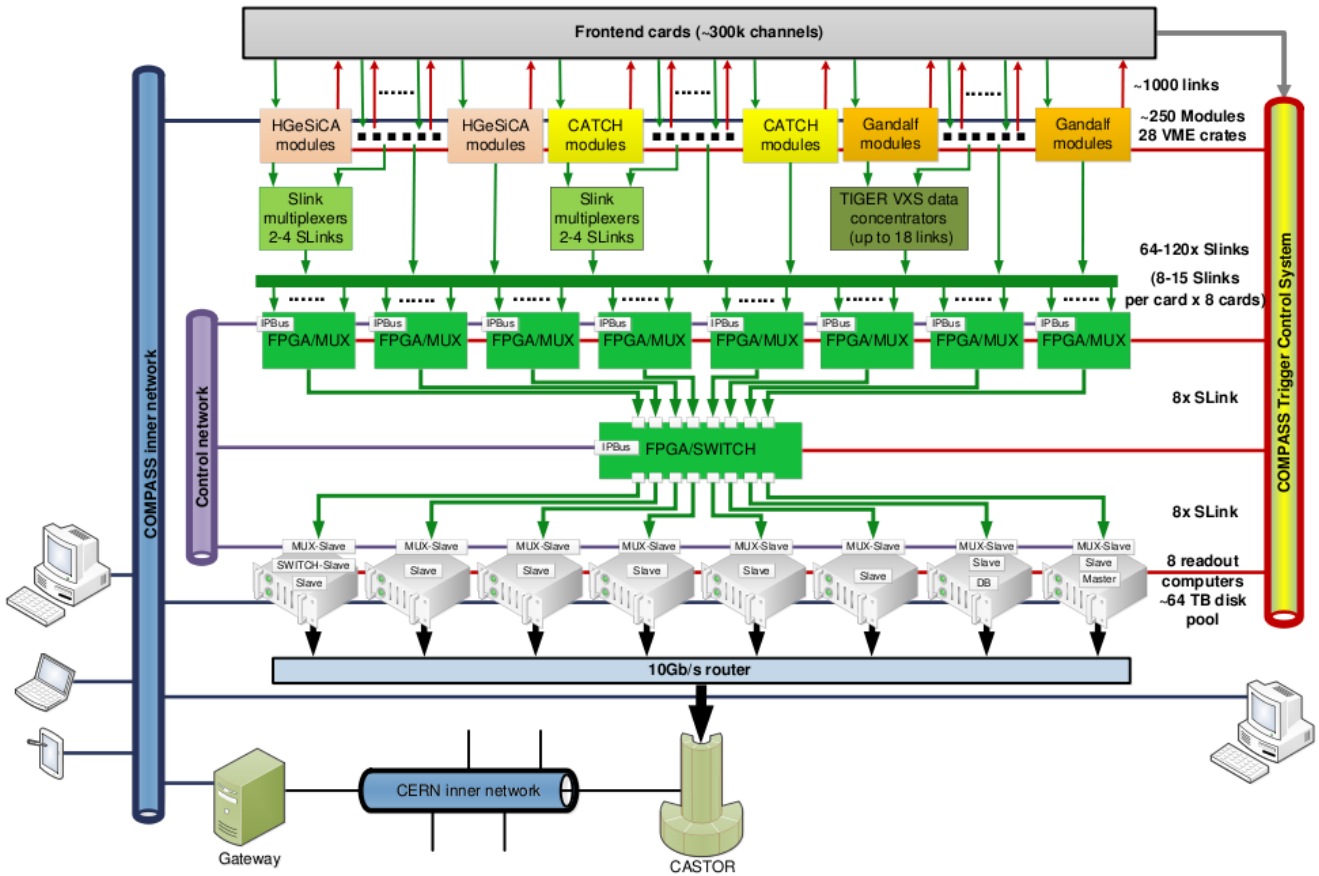
Design of the new DAQ - Hardware

Frontends

- ∼ 100 HOLA SLINKS
- peak data rate after trigger: ∼ 8 GB/s

Hardware event builder

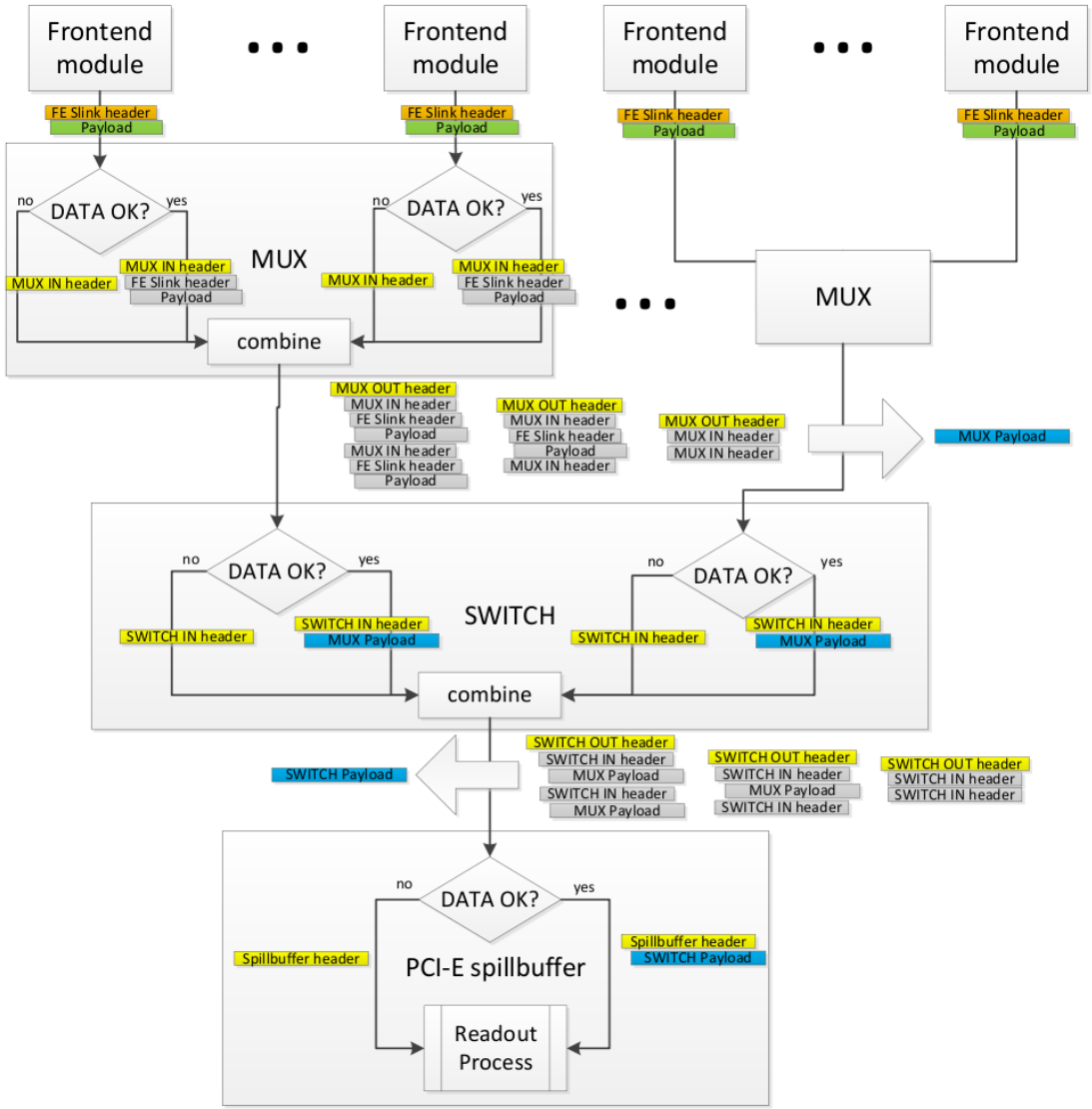
- consists of:
  - 8 new DHC modules as mux
  - 1 new DHC module as switch
  - 8 spillbuffer cards in readout computers
- 3 independent networks for
  - synchronization ⇒ (TCS)
  - data flow → event building (SLINK)
  - configuration and data flow control (IPBus)
- data buffering on different levels: theoretical max. 20 GB/spill ⇒ $1.0\,\mathrm{GB/s}$ sustained data rate



Sources: [3, 5, 7]

Hardware Based Event Building

- **On each layer:**
  - Verification of data
  - Discarding of wrong data
  - Adding of layer-specific header
- **Readout process:**
  - Decoding of data
  - Transformation of data into output format (DATE)



Source: [6]

Data Handling Card (DHC)

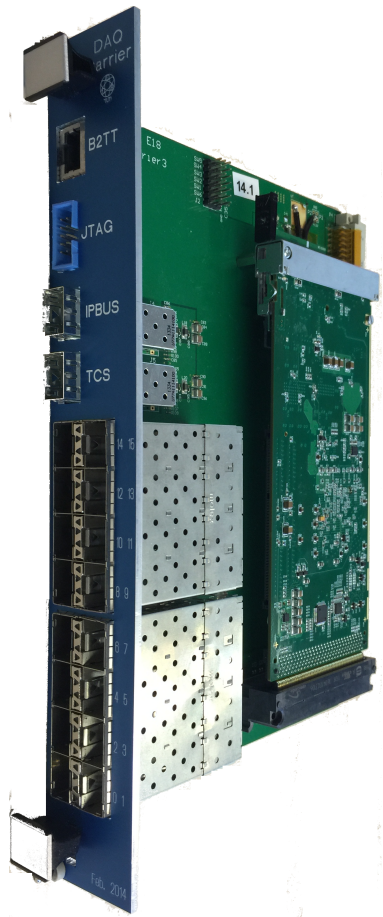
Carrier Card

- **form factor:** 6 U VME
- **interfaces:**
  - TCS (Trigger Control System) receiver
  - 1 Gb Ethernet for control network (IPBus)
  - 16 serial data links (SLINK)
  - JTAG for programming FLASH (after via IPBus)

AMC module

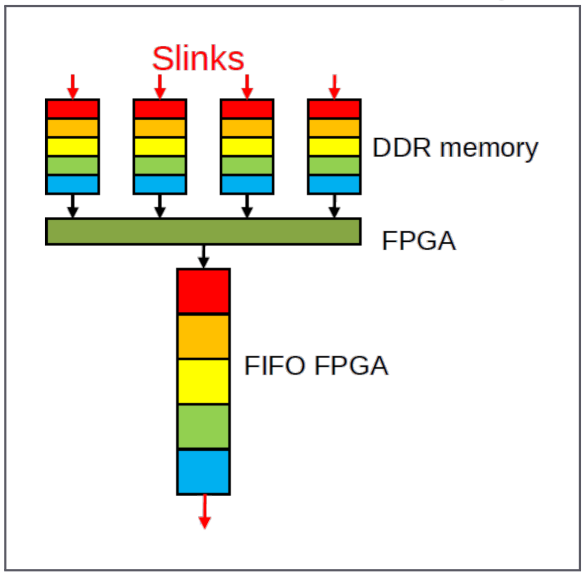
- **form factor:** AMC standard
  ⇒ compatible to ATCA
- **FPGA:** Virtex6 XC6VLX130T
- **memory:** 4 GB DDR3
- **firmware:** DHCmx 15:1 or DHCsw 8x8
- **data rate:** 3 GB/s throughput

DAQ unit
=
carrier card + DHCxx

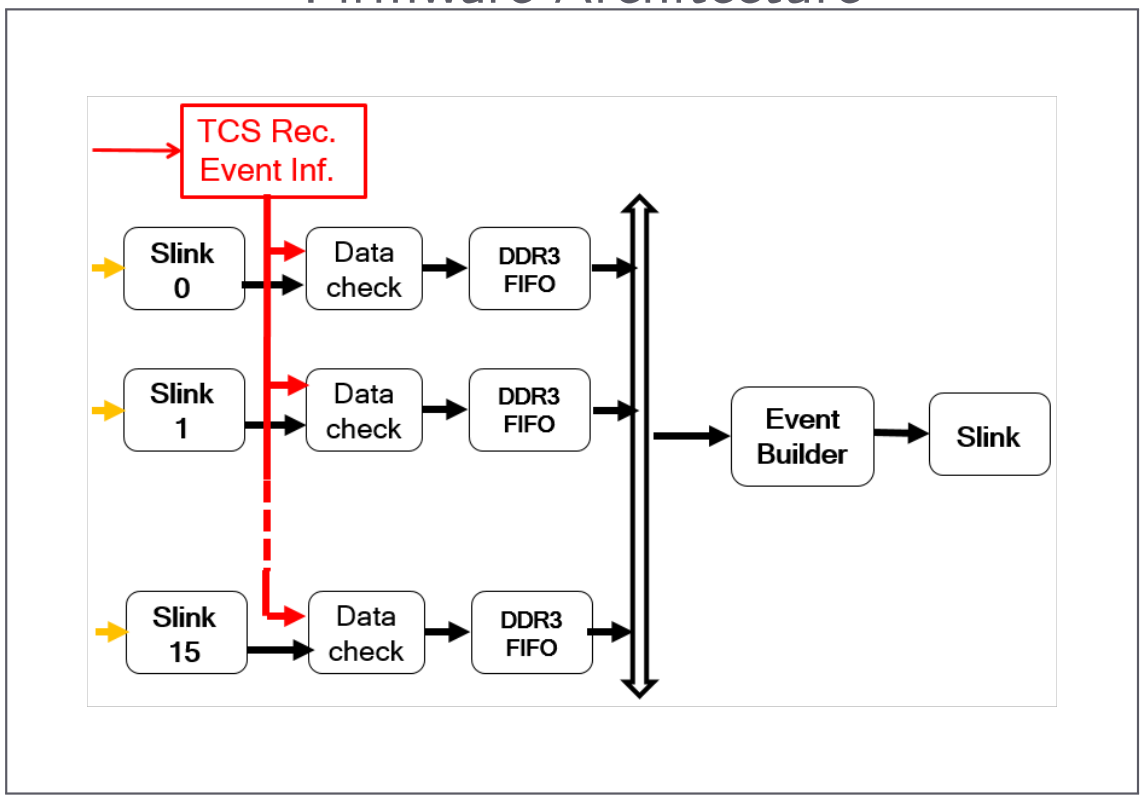


Firmware - DHCmx

Subevent building



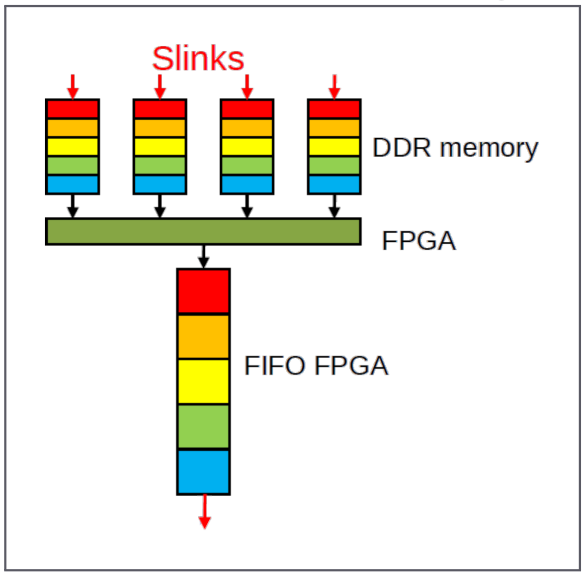
Firmware Architecture



- ▷ memory interface optimized to use full bandwidth of SDRAM (6.4 GB/s)

Firmware - DHCmx

Subevent building



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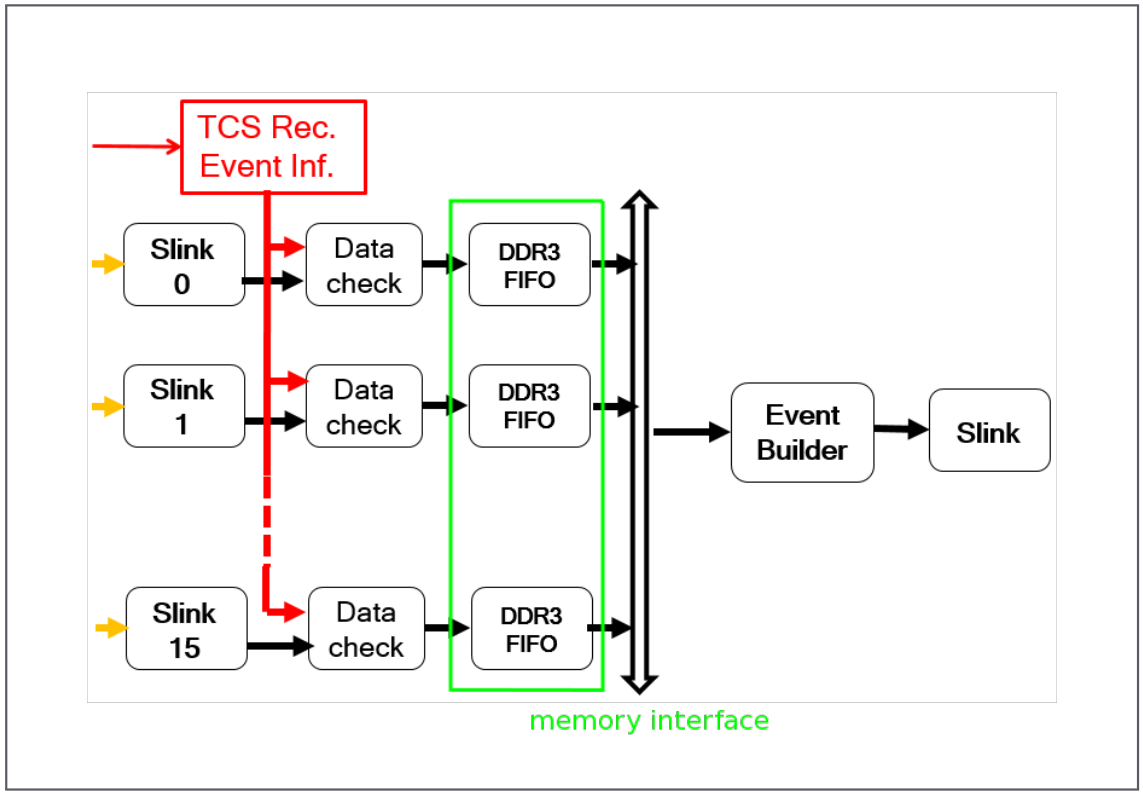
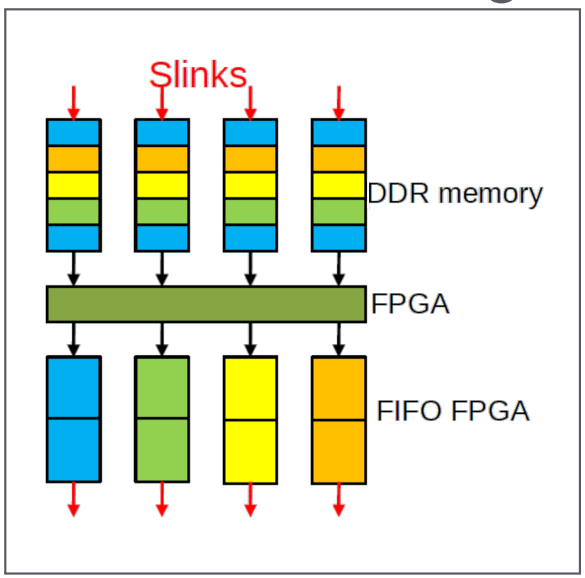


- memory interface optimized to use full bandwidth of SDRAM (6.4 GB/s)

Firmware - DHCsw

Subevent building



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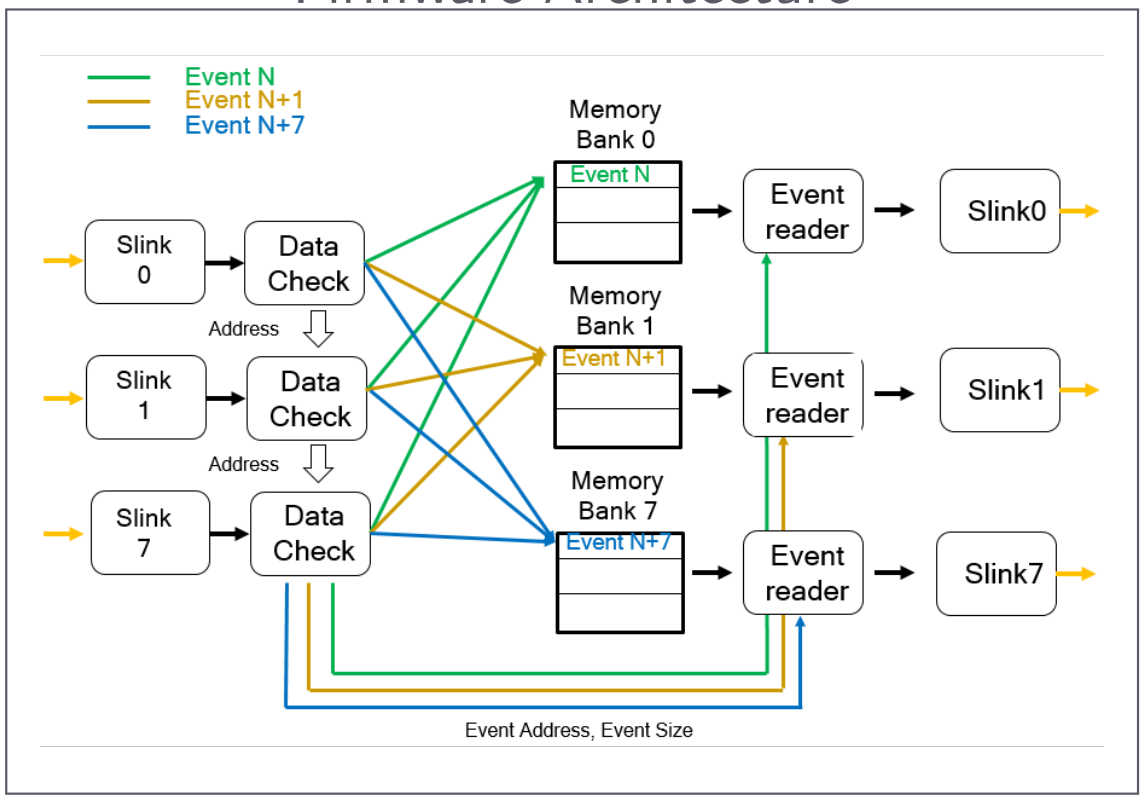
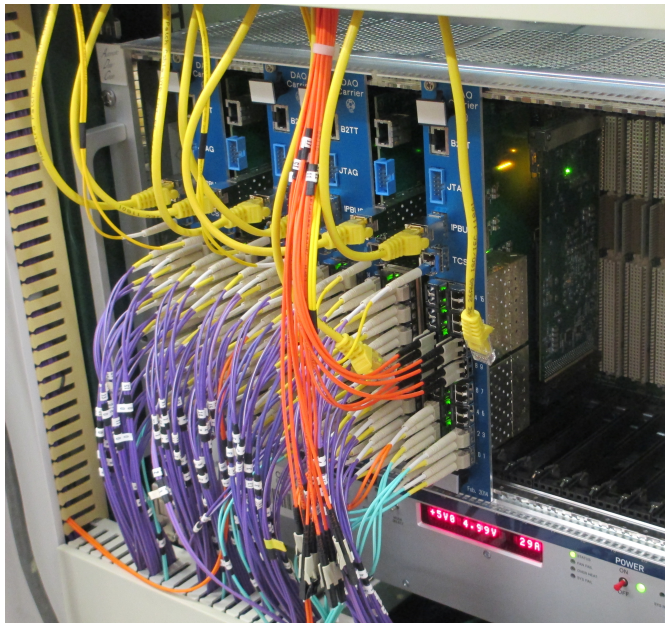


- size of memory bank: 0.5 MB = max. possible event size in COMPASS

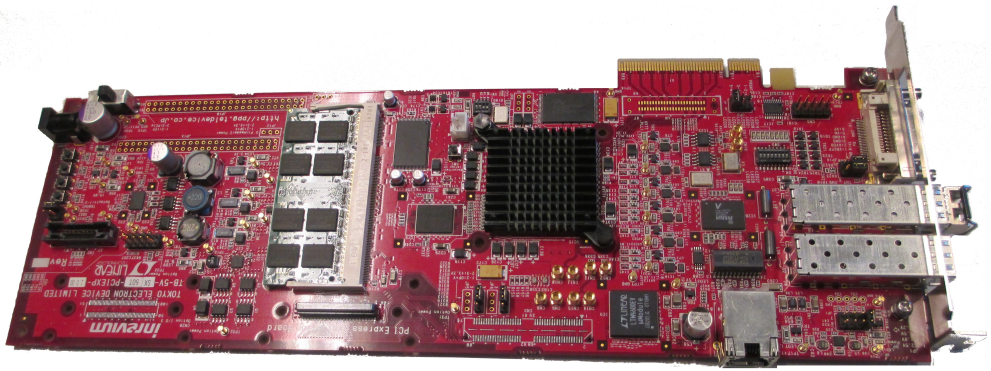
COMPASS FDAQ - Hardware Parts

Hardware Event Builder

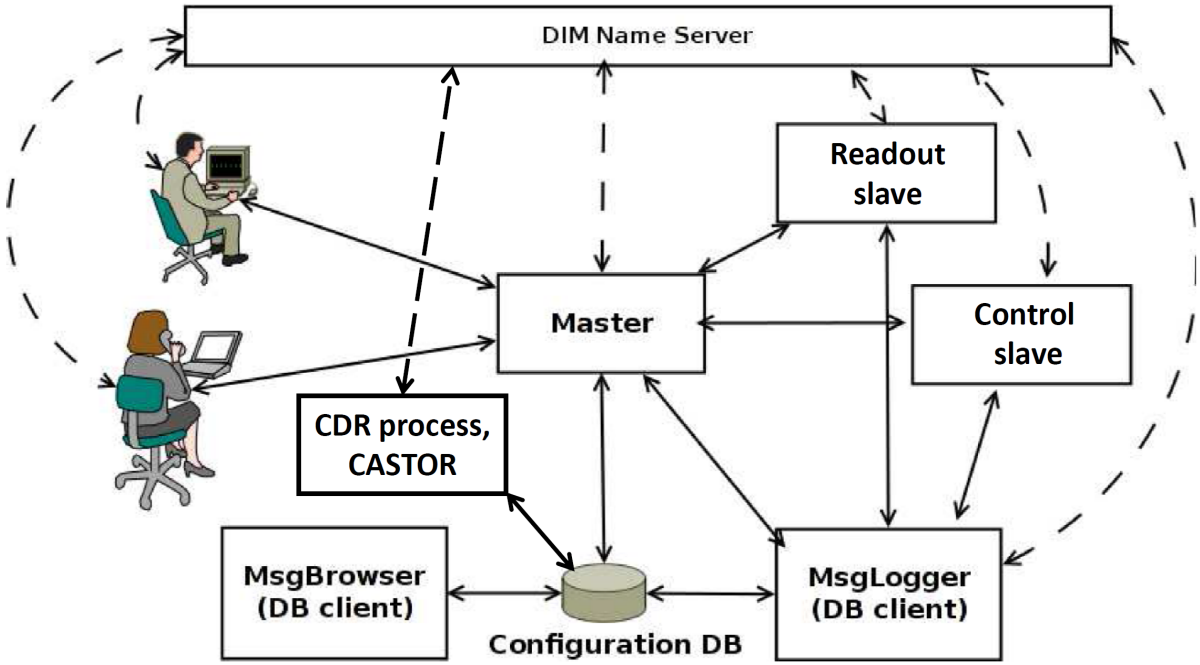


Readout Computers

PCI-E spillbuffer card



Design of the new DAQ - Software



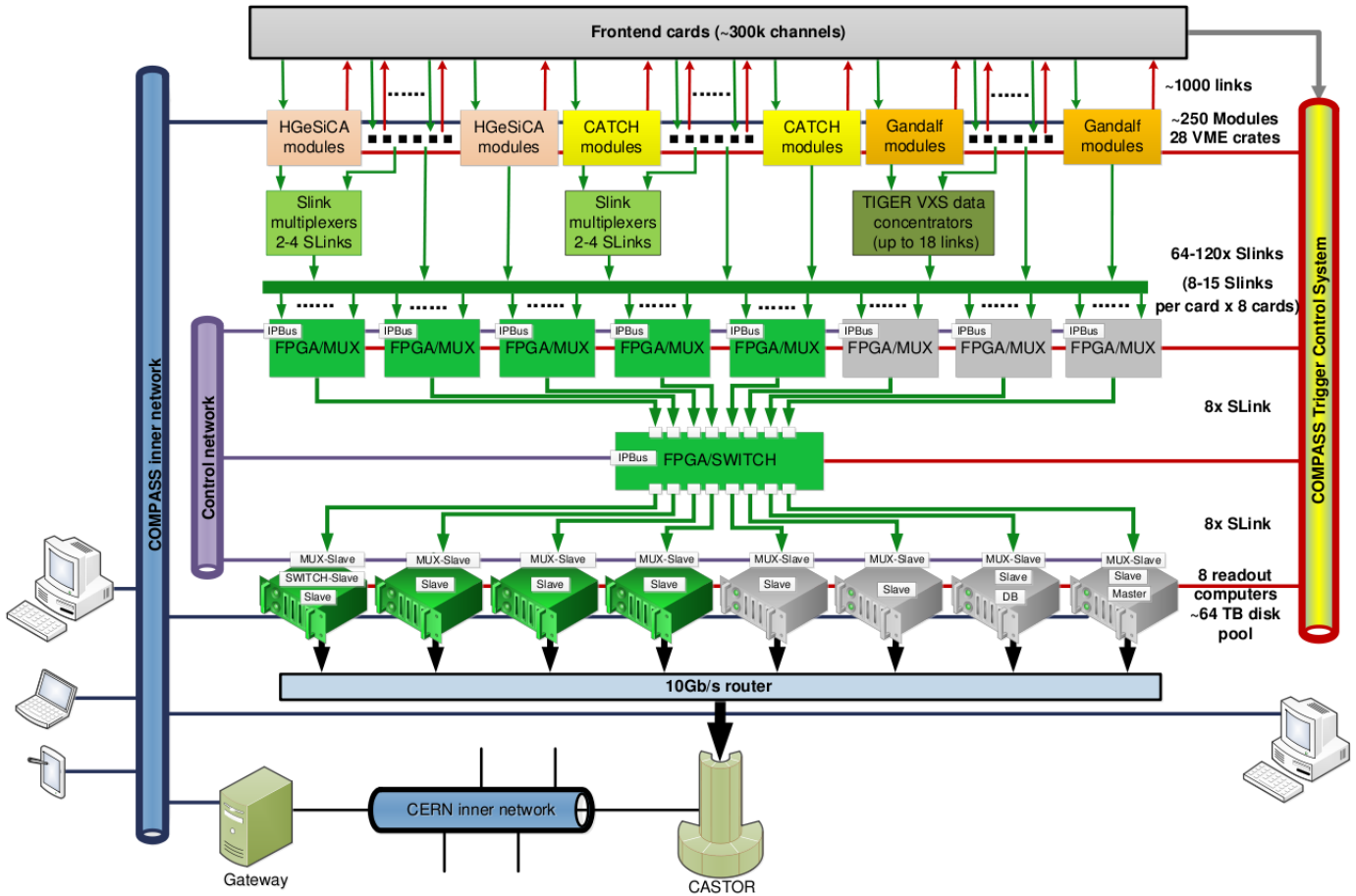
Used Technologies

- **DIM**
  server/client communication between processes
- **Qt5**
  used for all processes in DAQ - speed up of the development process
- **MySQL**
  database management system
- **PHP and javascript**
  webconfiguration of DAQ
- **bash and Python**
  support scripts

Sources: [2]

Drell-Yan DAQ Setup (2014/2015)

- 5 DHCmx
- 1 DHCsw
- 4 readout engines



Summary of Run 2015

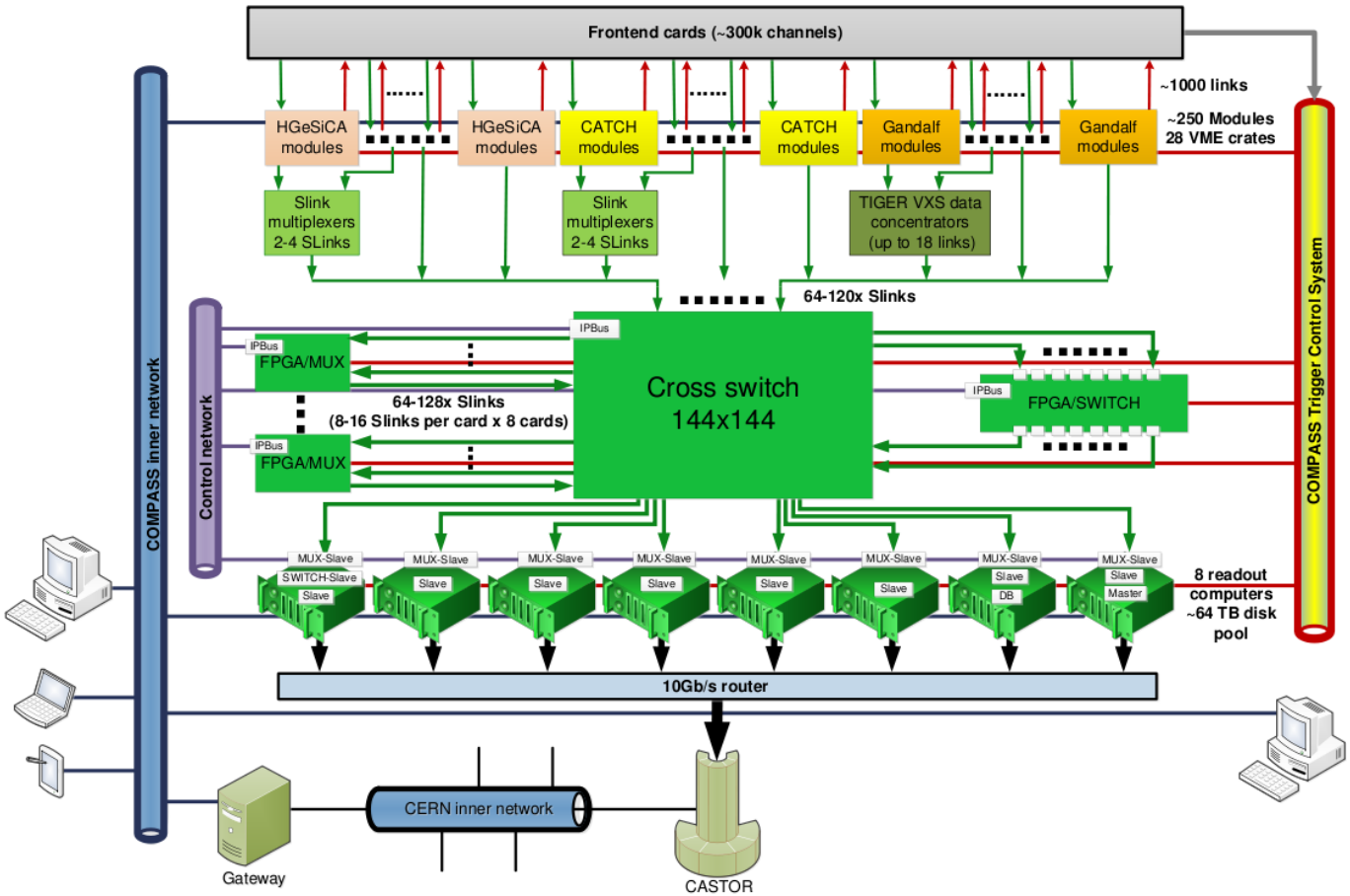
Accomplished data rates:

- **on-spill data rate:** 600 MB/s
- **sustained data rate:** 200-250 MB/s
- **input rate to DHCsw:** $\sim$ 1 GB/s
- **output rate from DHCsw:** 400 MB/s

Conclusion:

- DAQ system commissioned at nominal conditions for Drell-Yan
- Run successful $\rightarrow$ quite stable DAQ operation
- Observed problems: (1-2 times per day)
  - problems caused by certain errors in FE data format
  - wrong subevents merged into one event
  - crash of DAQ process

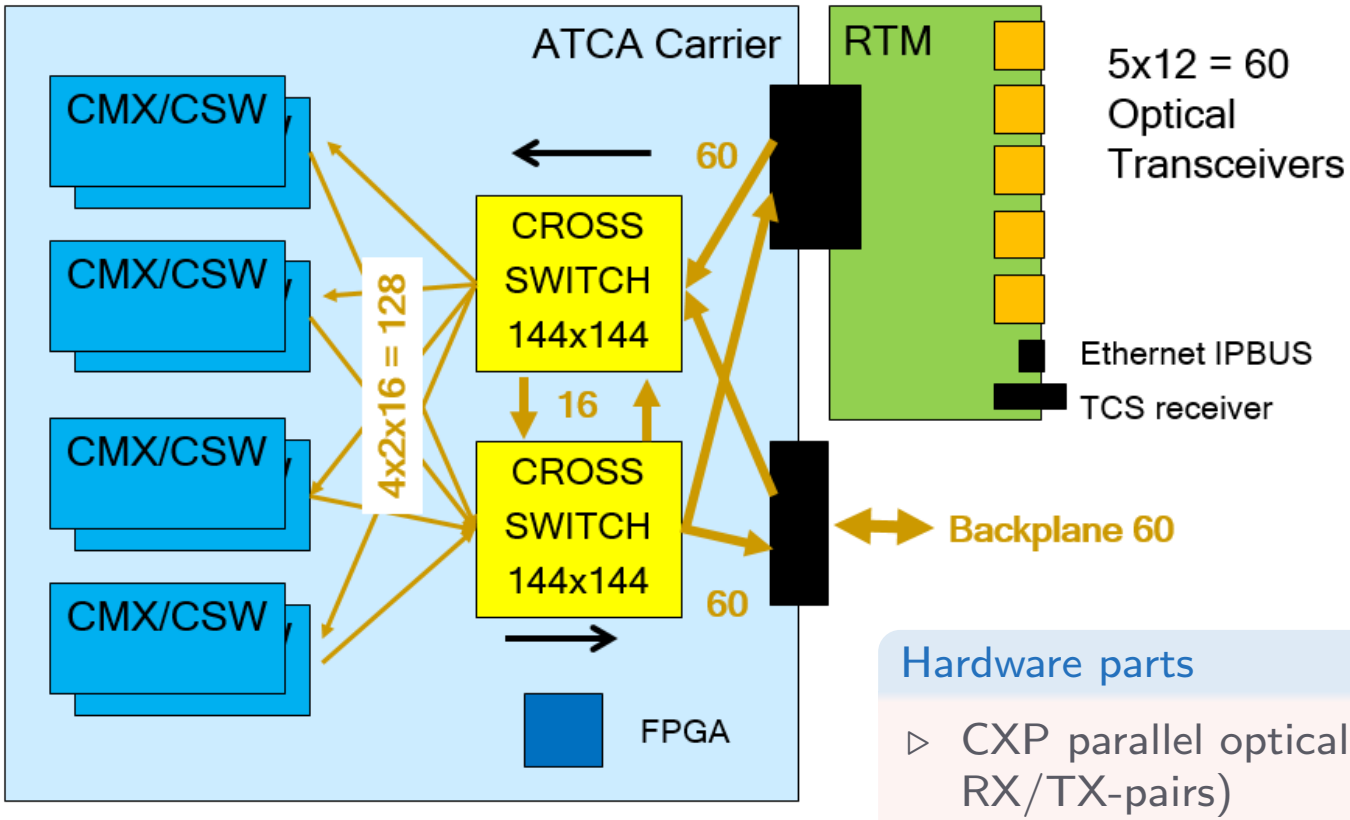
Future Developments - Crosspoint Switch



- connects:
  - FE electronics
  - DHC MUXs
  - DHC SWITCH
  - spillbuffers
- purpose:
  - load balancing
  - system redundancy to compensate hardware failures

⇒ provides fully customizable DAQ network topology!

Crosspoint Switch - Schematic



ATCA shelf for two modules

Full mesh interface
⇒ 60 links between both modules

Hardware parts

- CXP parallel optical transceiver (12 RX/TX-pairs)
- Vitesse - VSC3144-02 crosspoint switch
- Xilinx Artix-7 XC7A200T for crossswitch control and DHC communication
  - UCF = **U**niversal **C**ommunication **F**ramework
  - for star-like network topology (1:1,1:n)
  - subchannels: data transmission, IPBus, TCS, JTAG
  - for more information: poster 21 [4]

Sources: [8, 4]

Comparison with old DAQ

- More compact hardware → HW EB fits into one VME crate
- High reliability
- Tolerates FE errors → actively used by collaborators to debug and test new detectors
- user friendly Run Control GUI → less experience from shift crew
- Higher data rate → up to 1 GB/s sustained

Conclusion

- FDAQ commissioned in 2014
- FDAQ runs successful in 2015
- Minor problems to be fixed
- Long-term plans:
  - development and integration of the crosspoint switch
  - continuously running and self-recovering DAQ

References I

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New data acquisition system for the COMPASS experiment.
In *Top. Work. Electron. Part. Phys.*, 2012.

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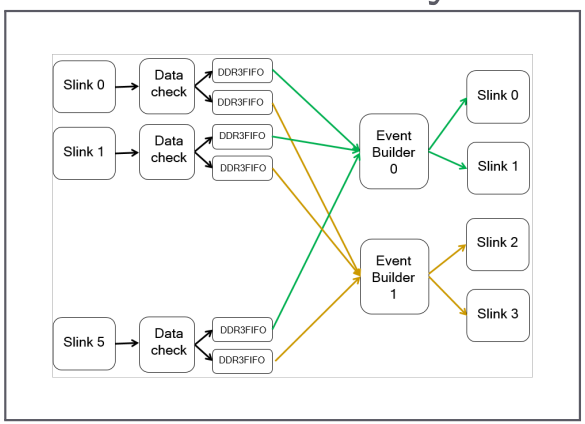
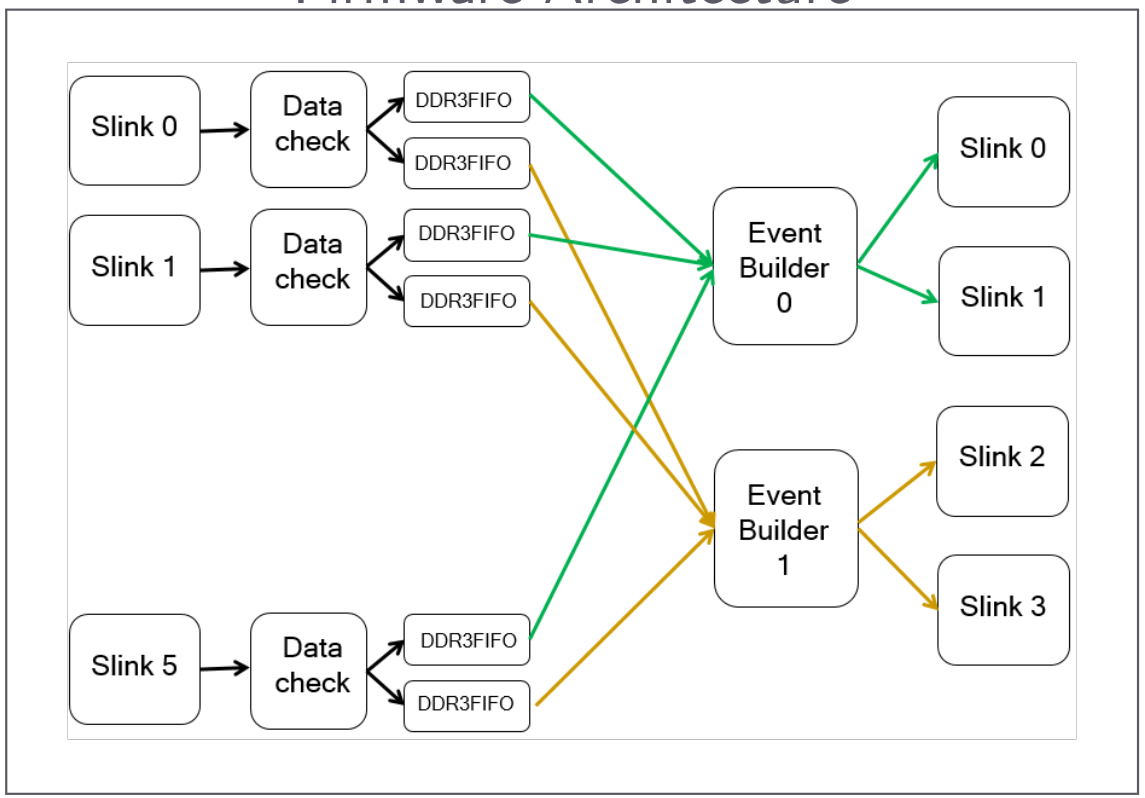
VSC3144-02 Crosspoint Switch.
Technical Report June, 2011.

Backup - Current FW for DHCsw

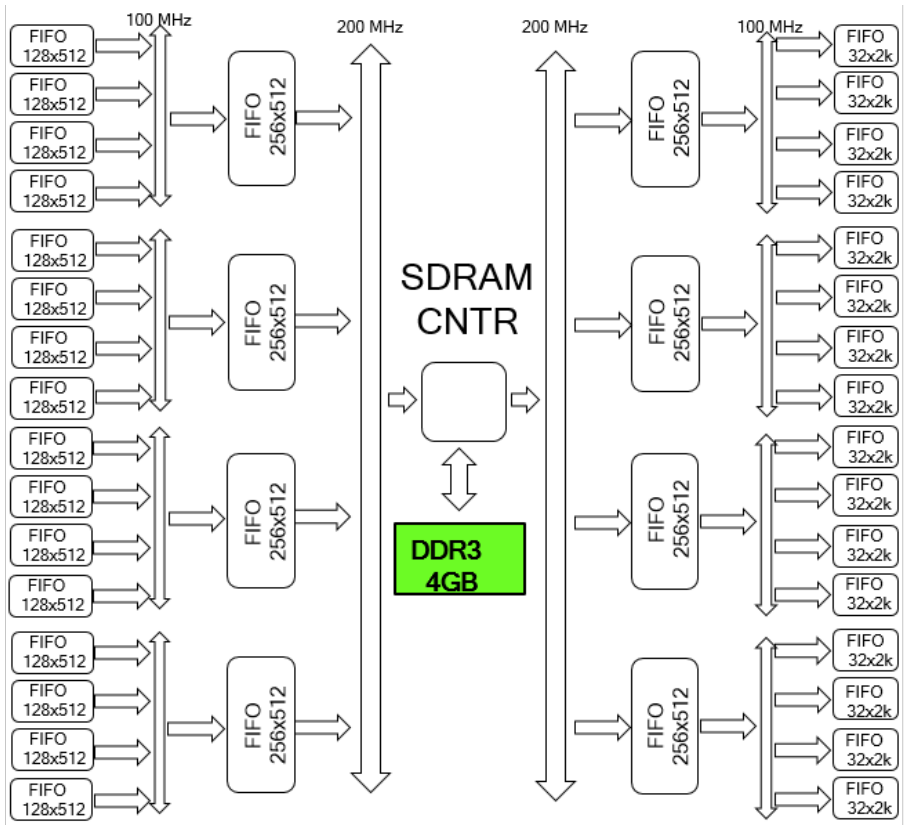
Functionality



Firmware Architecture

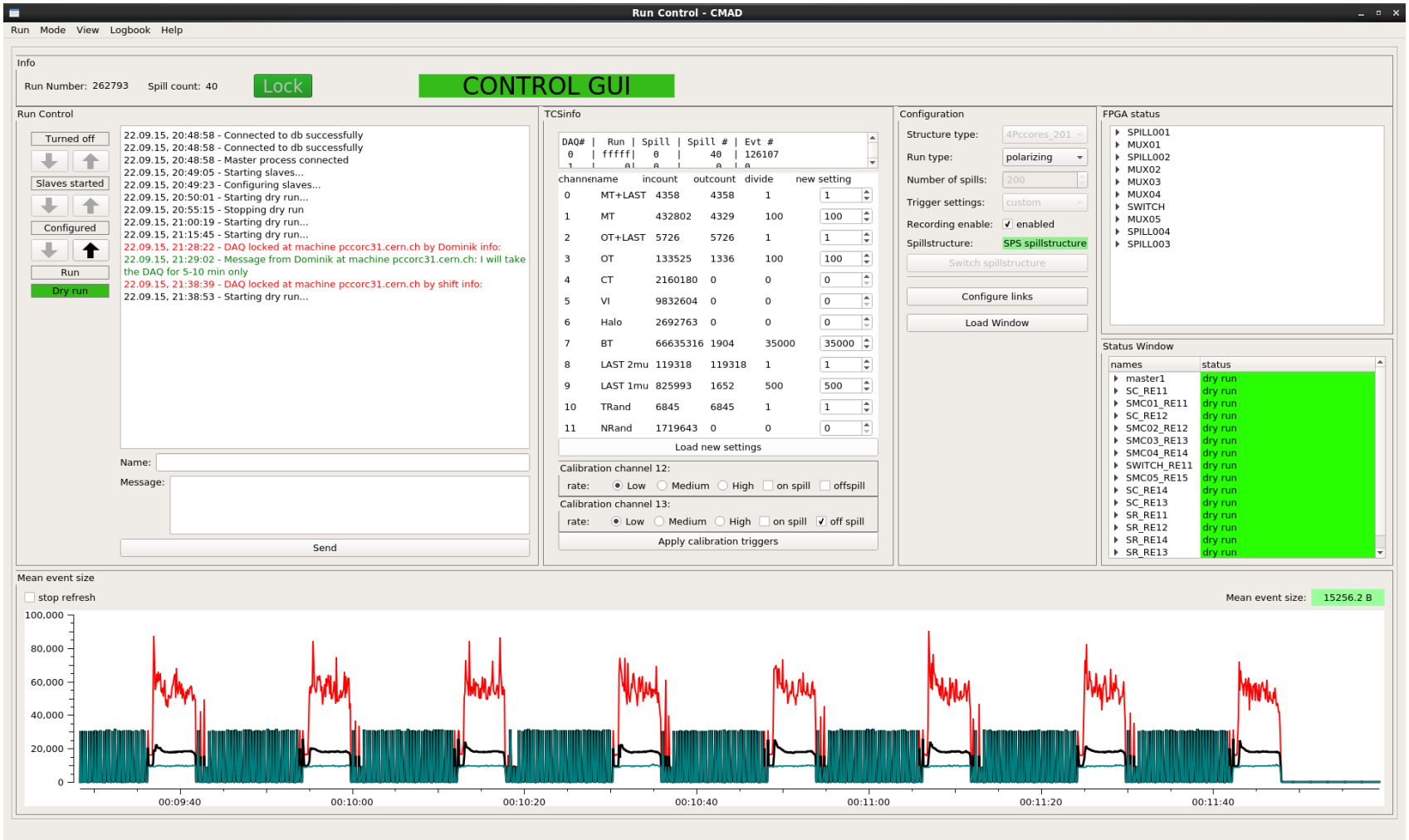


DHCmx - Memory Interface

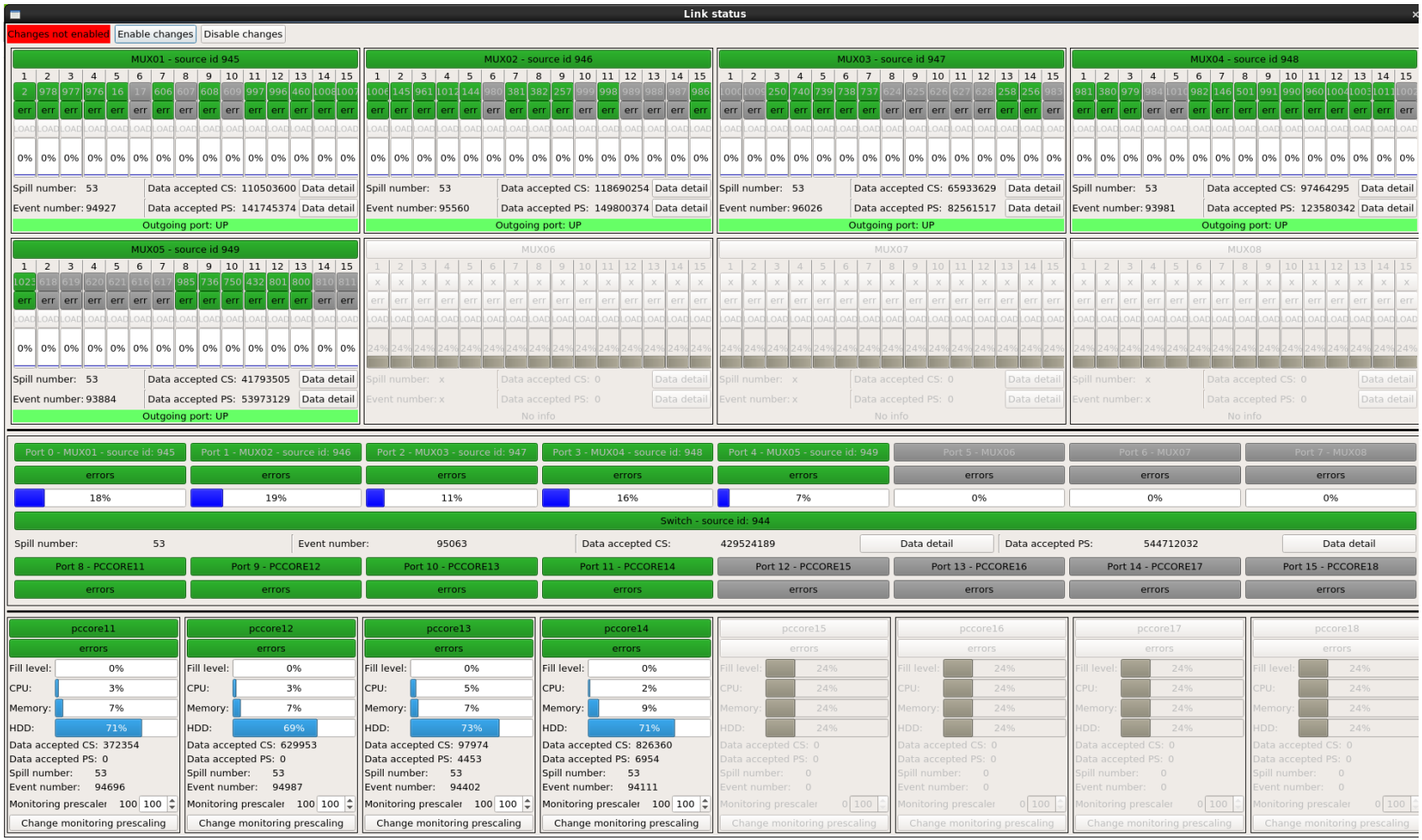


- design optimized to use full bandwidth of SDRAM (6.4 GB/s)
- finite logic resources $\Rightarrow$ double-layer multiplexer
- priority for incoming streams

Run Control GUI



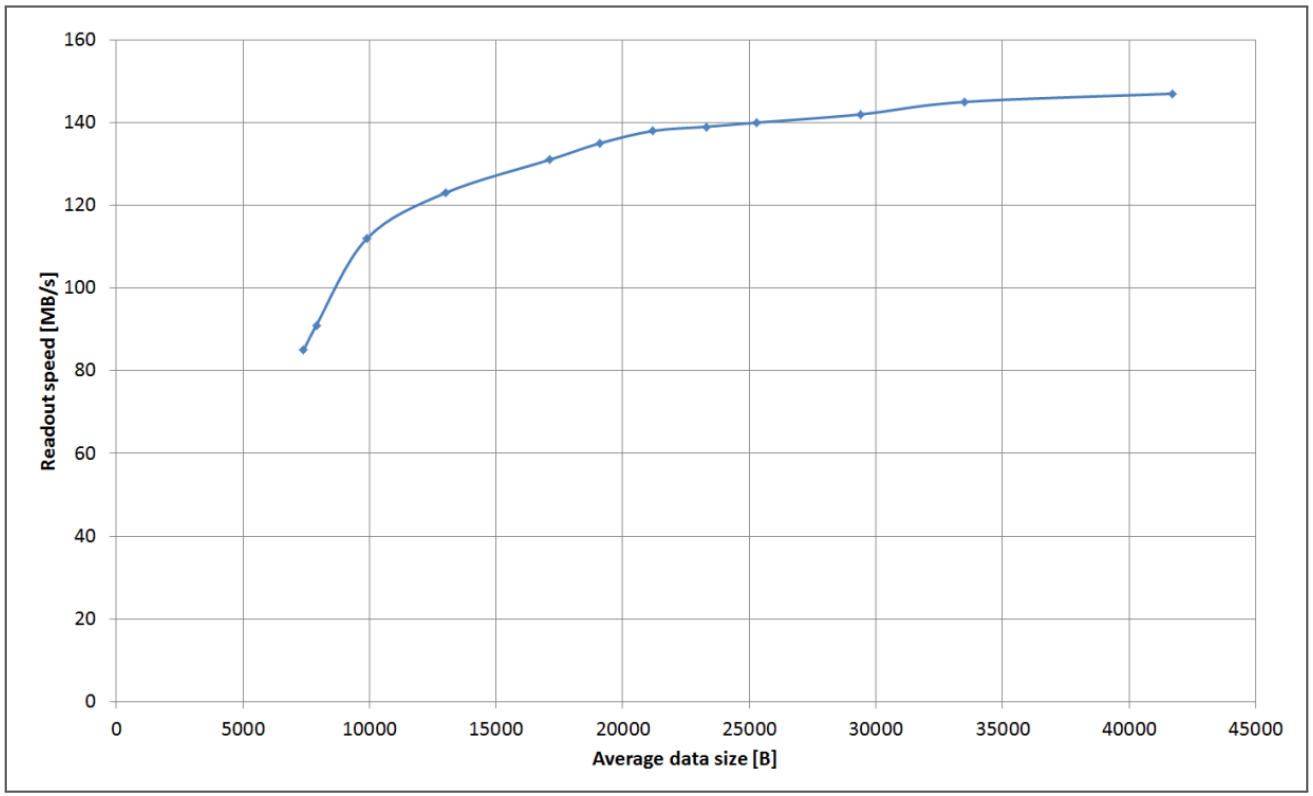
DAQ overview Window



Backup - Speed tests in 2015

- Readout process only realtime process ⇒ limiting readoutspeed
- Test of readout speed with 2 computer setup:
  ⇒ extrapolated total speed of whole setup: ∼ 1.2 GB/s (still needs verification)

Readout speed per computer



Sources: [6]

ATCA-based Event Builder

ATCA shelf

Full mesh interface $\Rightarrow$ 60 links between two modules

ATCA Standard

Zone 1:
Power management

Zone 2:
Data interface (Full mesh)

Zone 3:
Rear Panel Interconnect (Rear Transition Module)