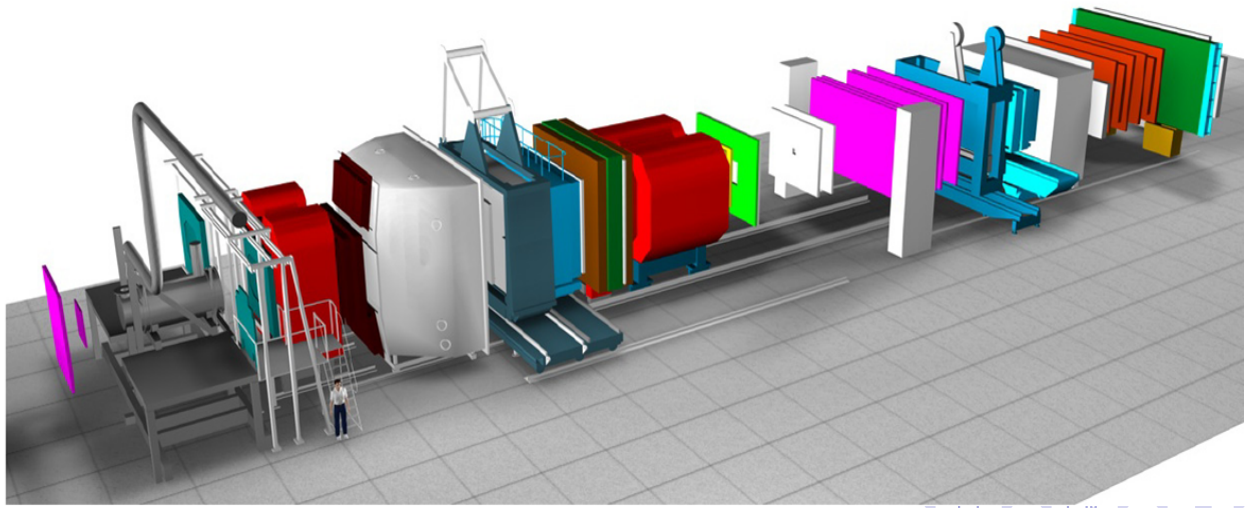
Pilot run of the new DAQ of the COMPASS experiment

M. Bodlak, V. Frolov,V. Jary, S. Huber, I. Konorov, D. Levit,
J. Novy, R. Salac, D. Steffen and M. Virius

Faculty of Nuclear Sciences and Physical Engineering
Czech Technical University in Prague
&
CERN

COMPASS experiment

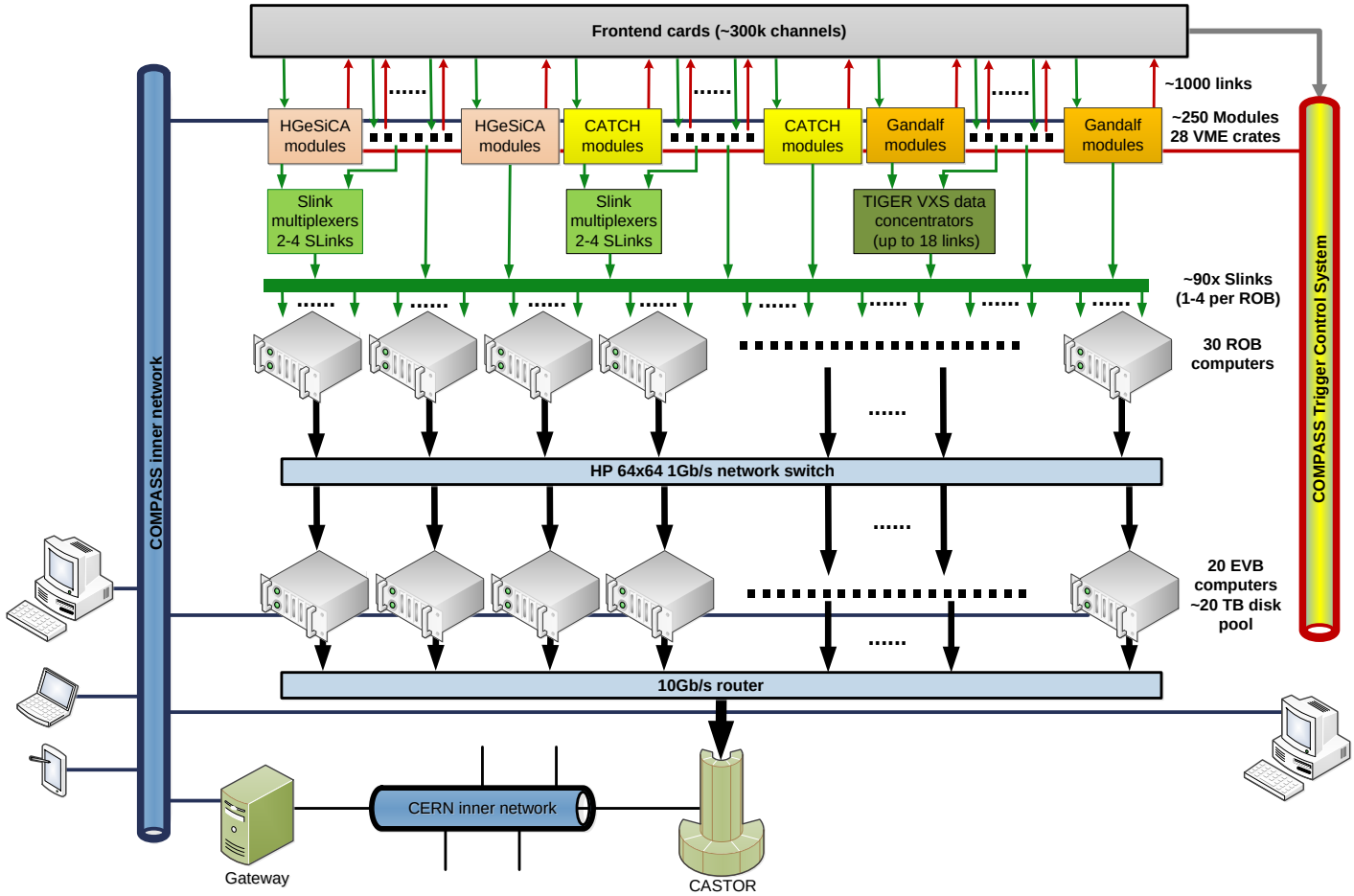
- fixed target experiment at SPS accelerator at CERN
- study of hadron structure and hadron spectroscopy with high intensity muon and hadron beams
- data-taking started in 2002
- trigger rate up to 30 kHz, average event size up to 50 kB
- in spill data rate 1.5 GB/s and sustained data rate 500 MB/s



Hardware/Software structure of the previous DAQ

Network based E.B.

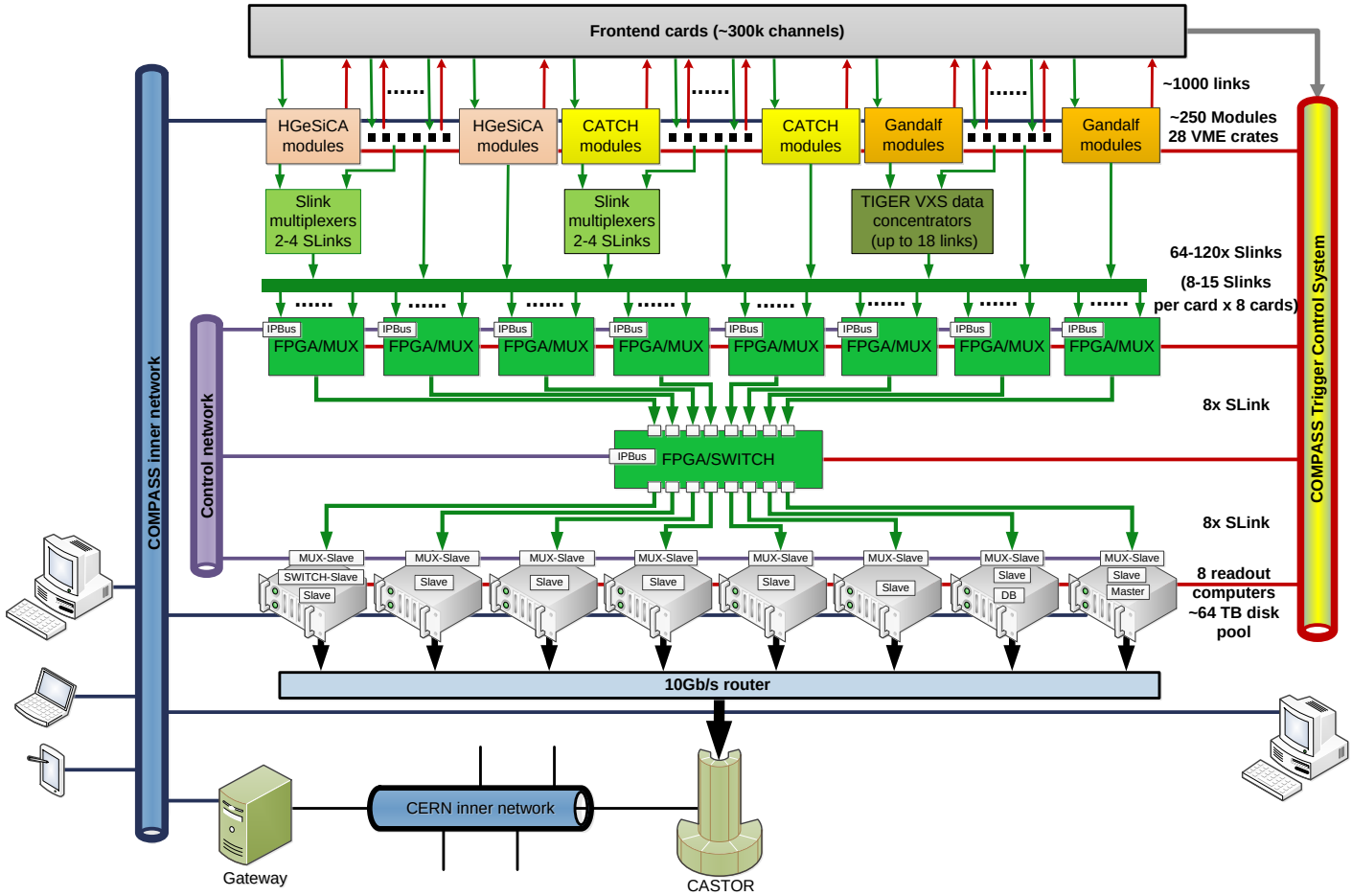
- ∽ 300k channels
- ∽ 1000 links to ∽ 250 modules
- ∽ 90 S-links to 30 ROBs
- **50 online computers** = 30 ROB+ 20 EB
- DAQ built in 2000
- sustained rate only of 500 MB/s
- Software event building



Hardware/Software structure of the new DAQ

Hardware based E.B.

- 8 new DAQ modules as multiplexer
- 1 new DAQ modules as switch
- 8 readout computers
- 64 TB disk pool using RAID 10
- less components
- full events received by servers
- consistency check at many layers



Hardware based event building

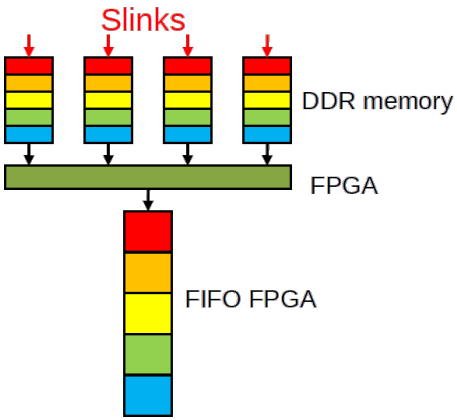
HW event building in history

- CDF - Fermilab [11]
- NA48 - CERN [12],[13]

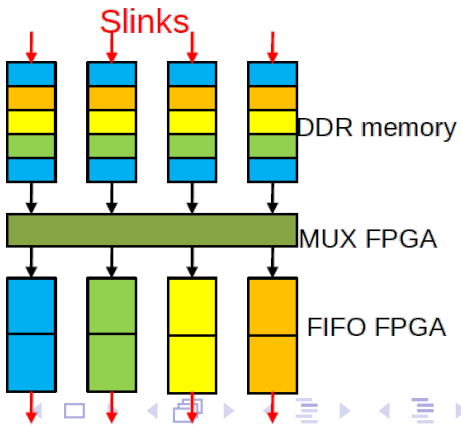
HW event building now with new FPGAs

- faster - high speed serial links
- more flexible
- cheaper and more reliable
  - few components
  - synchronous with trigger system at all levels of event building
  - data consistency check at each stage of data transmission, data flow control
  - software monitoring and software data throttling

FPGA/MUX

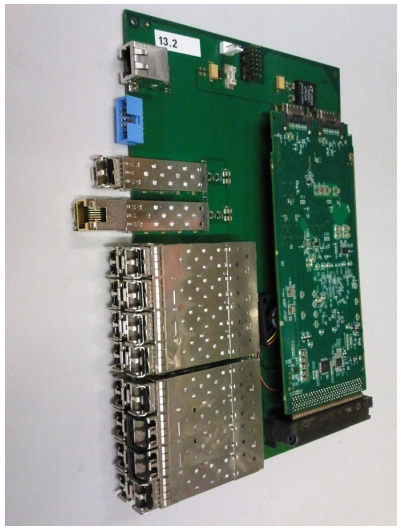


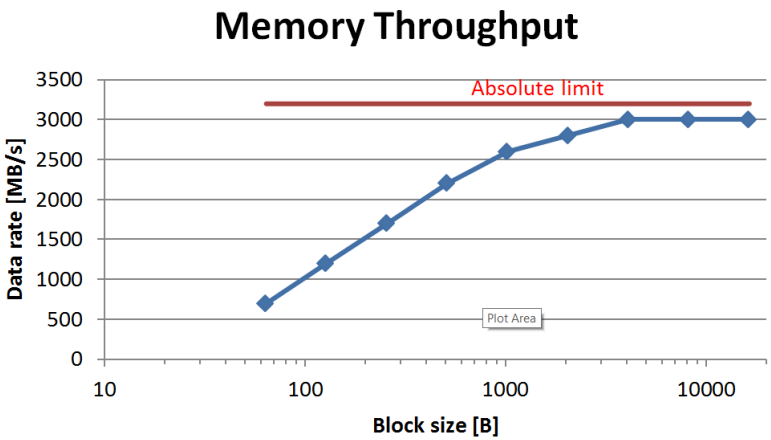
FPGA/SWITCH



DAQ unit

- TCS (Trigger Control System) receiver - synchronization information
- 1 Gb Ethernet - control system link (IPbus)
- 16xSerial links - data links
  - Slink (2 Gbps)
  - Aurora (6.25 Gbps)
- 6 U VME form factor module → New DAQ fits in one 6 U VME crate

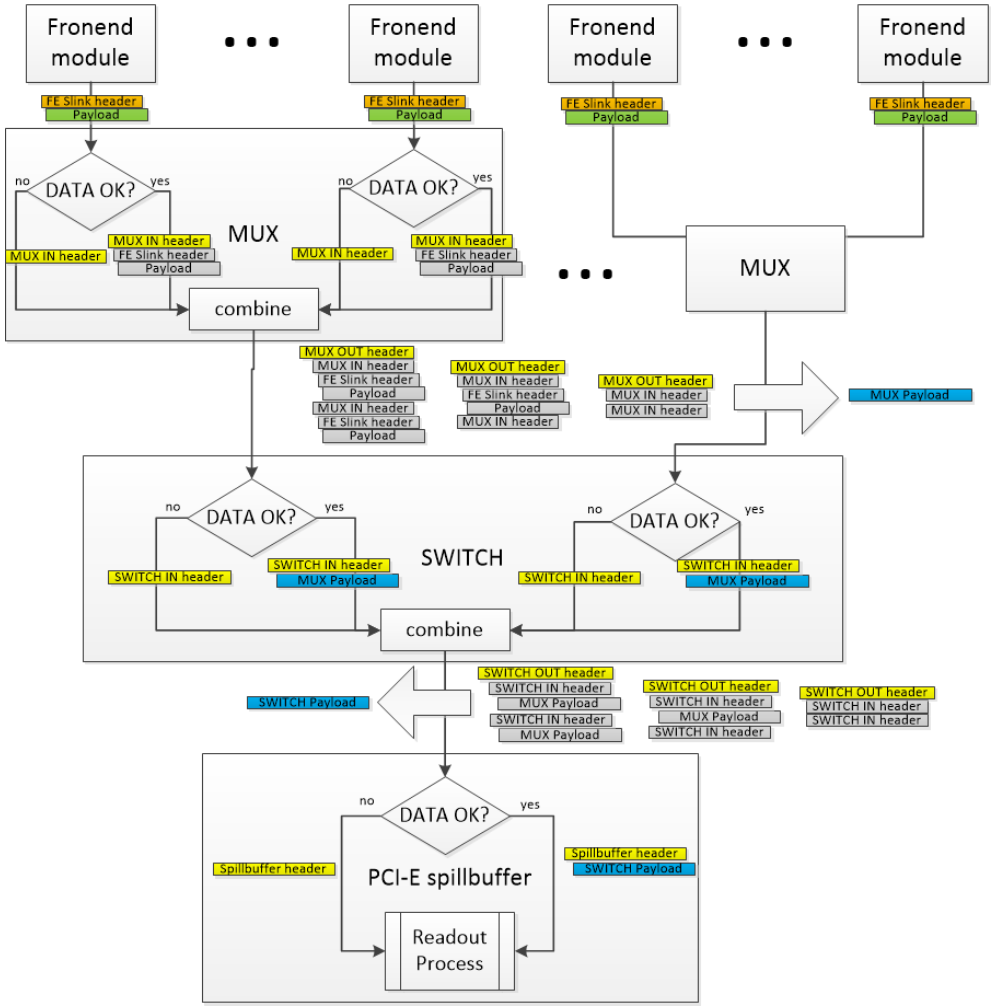




- AMC module, ATCA standard
- VIRTEX6 XC6VLX130T FPGA - middle sized FPGA and relatively cheap (500 Euro/chip)
- 1kEuro/amc module or 2kEuro for VME modue with optical transceivers
- 4 GB DDR3
- 3GB/s sustained → limit of current architecture
- Module programmed as MX 15:1 or SW 8x8 (can be recompiled to any NxM configuration)

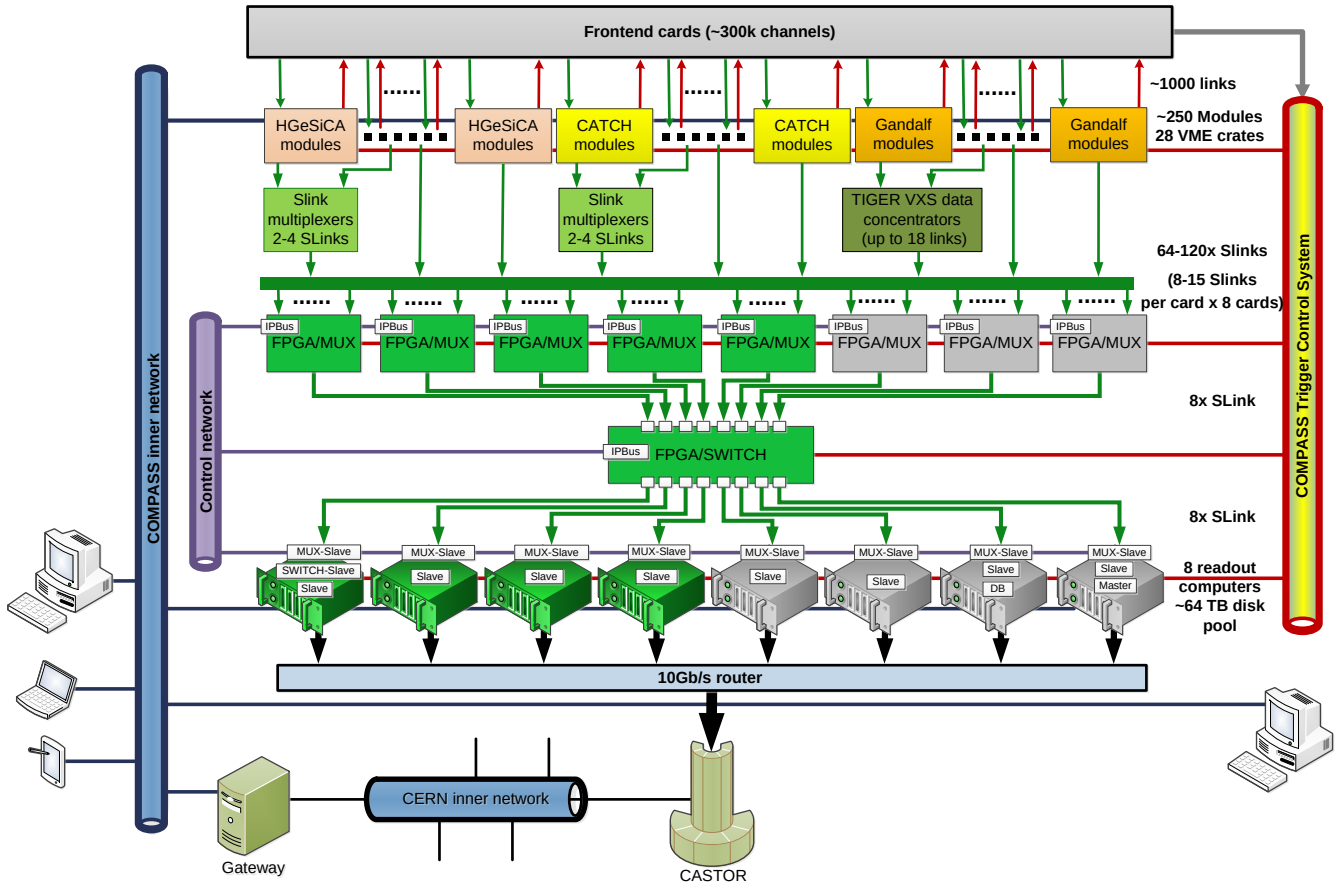
Example of Data Flow and Data encapsulation

- Each layer verify data and adds new header
- Data with errors thrown away and header generated
- Data decoded by readout process and transformed to output format

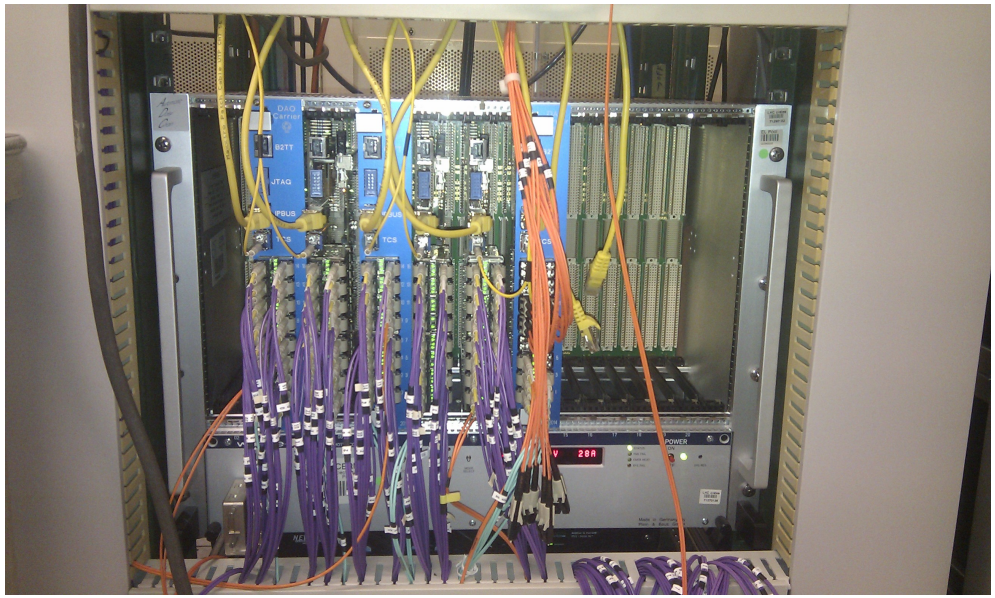


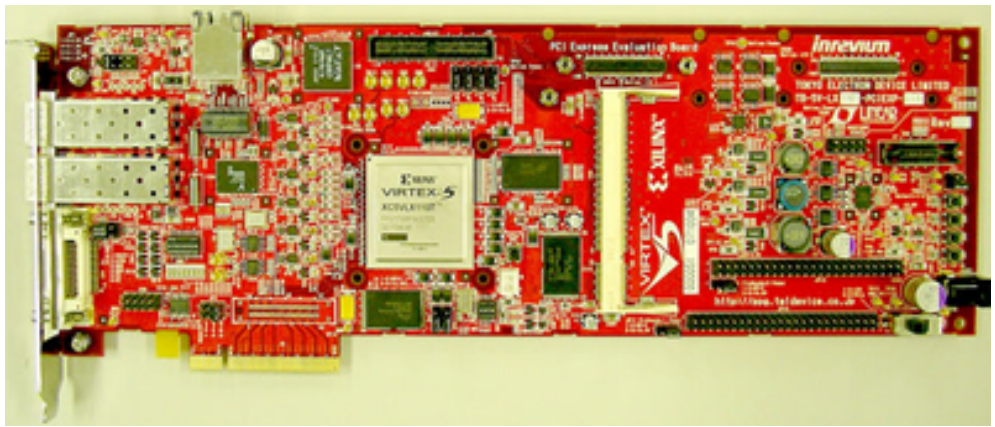
DAQ setup for 2014

- first run of COMPASS experiment with hardware event building
- physics pilot run with many new detectors
- 5x Data Handling Cards (DHC) as MUX
- 1x Data Handling Cards (DHC) with prototype SWITCH firmware
- 4x readout engine computers with PCI-e spillbuffers



New DAQ parts





Performance during run 2014

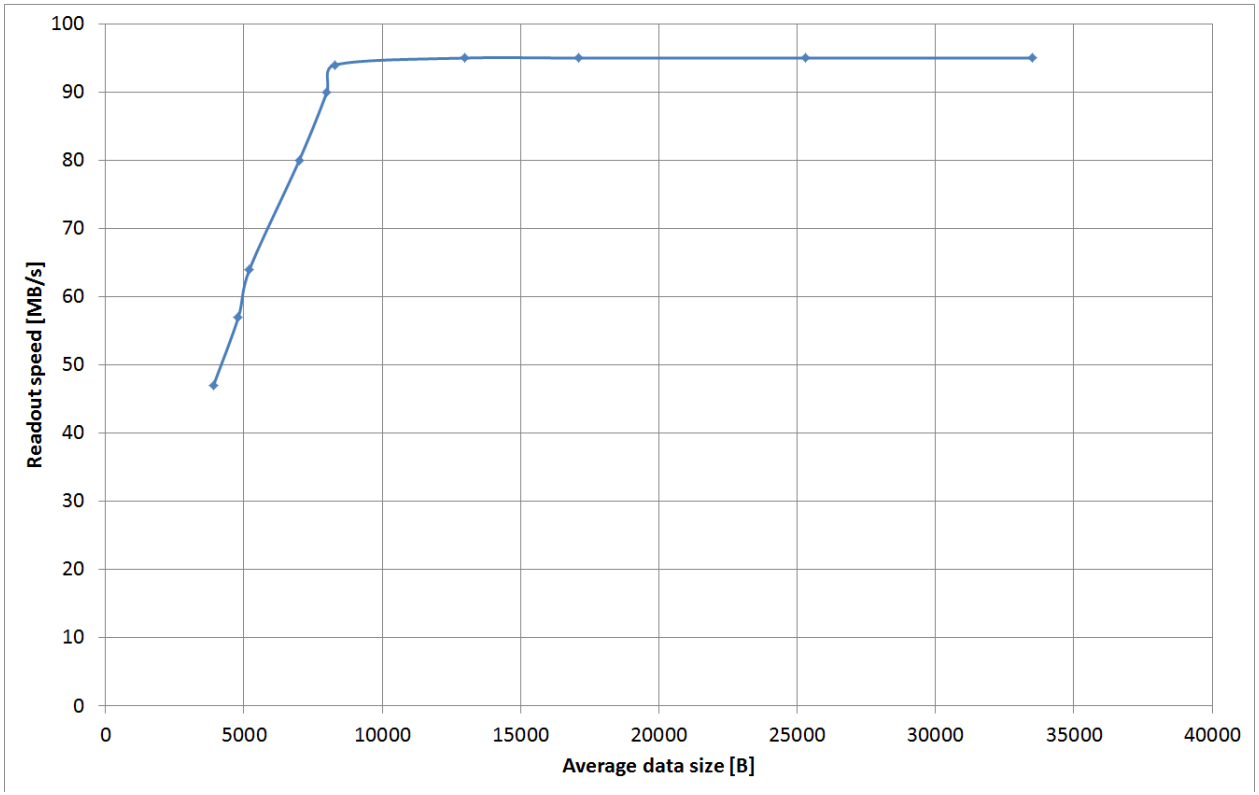
- run at nominal conditions for Drell-Yan run $\rightarrow$ not limited by DAQ
- maximum of readout speed was 80 MB/s per RE computer
- several bugs found
- few problems with frontend errors handling $\rightarrow$ still more stable then previous DAQ
- run was successful
- main GUI and message browser process proved to be user friendly

Performance during in 2015

- improvement of all software parts and new version of firmware developed
- error handling and stability improved (problems with handling of constant flow of error messages fixed)
- speed greatly improved 80MB/s $\rightarrow$ 150MB/s
  - multithreading
  - message handling
- programable buffer sizes to match data rate of attached link introduced $\rightarrow$ synchronous filling of buffers
- firmware update over IPBUS

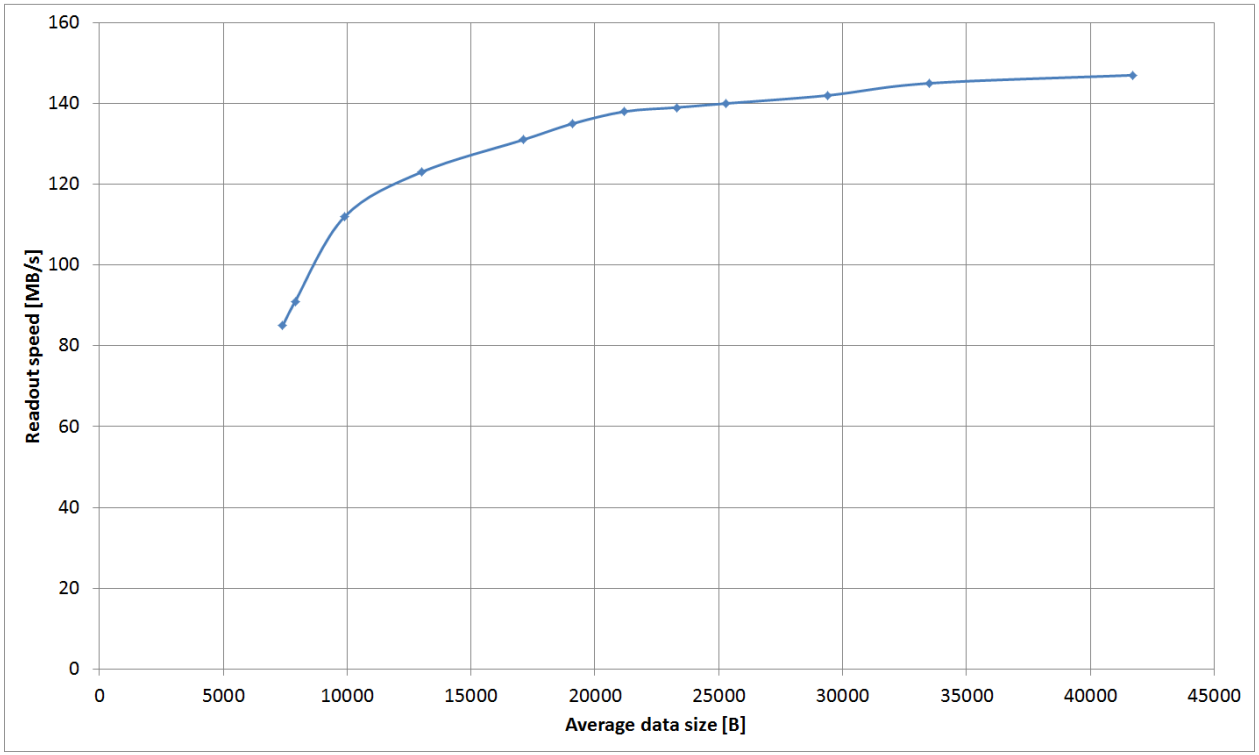
Speed tests after improvements

- setup as in 2014 run - 4 pccore computers
- limit of 95 MB/s per pccore without any filling of spillbuffer



Speed tests after improvements

- setup reduced to two pccore computers
- limit of 150 MB/s per pccore - limited by readout program



Comparison with old DAQ

- More compact hardware
- Software complexity comparable
- Flexible configuration
- Data verification on every step - easier to identify source of error
- Less power demanding
- Easier to control (more time for reaction, auto correction functions)
- Partially finished DAQ already faster

Conclusion

- 2014 run has been successful
- core system commissioned and possible improvements identified
- expected sustainable rate 2.5 GB/s
- on the route to long run in 2015

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