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The COMPASS RICH-1 read-out system

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Abstract

This paper describes the reconfigurable read-out system for the 82944 RICH-1 channels of the COMPASS experiment (NA58) at CERN. The system is based on 192 identical large front-end boards (BORA board). BORA was designed for acquiring, digitizing, threshold subtracting and transmitting event data. The overall operation of the board is controlled and supervised by a DSP tightly interacting with an FPGA that acts as a parallel co-processor. The DSP allows characterizing each analog channel by locally calculating noise and pedestal. Each BORA communicates with the outside world through two optical fibers and through a dedicated DSP network. One optical fiber is used to receive event triggers, and the other one is used to transmit event data to subsequent processing stages of the acquisition system. The DSP network allows reconfiguring and reprogramming the DSPs and FPGAs as well as acquiring sample events to visualize the overall operation of the system. The whole RICH has eight DSP networks working in parallel. These networks are handled by DOLINA, a PC resident multiprocessor board containing eight DSPs. Each network is formed by 24 BORA DSPs and 1 DOLINA DSP. The read-out system can steadily work up to a trigger rate of 75 kHz with maximum pixel occupancy of 20%, reaching a transmission data rate of 5.13 Gbytes/s.

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1. Introduction

The characteristics of new-generation RICH detectors represent challenging requirements for the read-out systems; such as large number of channels, asynchronous triggering, high average trigger rates, average data rates in the order of

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several Gbytes/s, reduced dead time, low power consumption and low noise. Moreover, since the experiment will last for years, the system must be flexible enough in order to adapt itself to new experimental conditions.

COMPASS RICH-1 is a gas radiator RICH employing MWPCs with CsI photocathodes as photon detectors [1–4]. The RICH-1 photon detectors consist of eight identical chambers, and its total active area is about $5.5\,m^2$. The photocathodes are PCBs segmented in $8\,mm \times 8\,mm$ pads, resulting in 82,944 pixels for the total active area [5].

All pixels must be acquired at every trigger. The COMPASS RICH-1 read-out system processes the signals coming from the pixels. These signals are amplified, filtered, digitized in 10 bits, and temporarily stored at every asynchronous trigger. Subsequently, threshold subtraction is performed and all resulting positive values, together with their channel identification, are packed into a data frame and transmitted to the global data acquisition (DAQ) system. The read-out system is also capable of measuring pedestal and noise of every single channel, and setting its corresponding threshold. Sparse sample events can be acquired, independently of the global DAQ system, for monitoring purposes.

The COMPASS experiment foresees an average asynchronous trigger rate of 100 kHz, which implies a DAQ rate of 10368 Gbytes/s for the RICH-1. The maximum expected pixel occupancy for the RICH-1 is 20%, which generates a data transmission rate of about 6.64 Gbytes/s.

In the following sections, we describe the general architecture of the COMPASS RICH-1 read-out system, and we give architectural details of the main boards as well as the functional description of them. A summary of the achieved performance is presented in the conclusions.

2. The general architecture

The COMPASS RICH-1 read-out system is based on 192 identical large front-end boards, called BORA [6], to acquire all the 82,944 channels. These boards are plugged on the external side of the photocathodes and connected to the pixels of the detector. There are 24 BORAs per chamber and each BORA handles 432 analog channels. Each board is identified by setting an 8-bit dip switch, where three bits identify the chamber and the remaining five bits identify the BORA within the chamber. This identification corresponds to a precise geographical position in the RICH-1 [7].

The overall operation of BORA is controlled and supervised by a 32-bit DSP (ADSP-21065L [8]). The board also has an FPGA (VIRTEX XCV100 [9]) that acts as a parallel co-processor of the DSP. The DSP configures the FPGA at reset time, and can reconfigure it at any time.

The BORA board communicates with the outside world through two optical fibers and through a dedicated DSP network. One optical fiber is used to receive event triggers, and the other one is used to transmit data to subsequent processing stages of the acquisition system [10]. The DSP network provides a slow connection with a PC (the RICH_Control PC) where a high-level control application software runs. This application software allows reconfiguring the FPGA and reprogramming the DSP. Programs, commands and data are transmitted through the DSP network between a BORA and the RICH_Control PC.

The whole RICH-1 has eight DSP networks working in parallel, one for each chamber. The RICH_Control PC has a dedicated multiprocessor board, called DOLINA, to handle these networks. DOLINA has eight on-board DSPs. The 24 BORA DSPs of a chamber and 1 DOLINA DSP form each network. All BORAs are optoisolated from DOLINA through eight specific optoisolating boards, one for each DSP network, avoiding this way grounding interference between the PC and the detector.

Fig. 1 shows the general physical architecture of the read-out system. In the RICH-1 box are displayed the eight chambers, each of them with its 24 connections (one per BORA) to an optoisolator board. The optoisolator boards are close to their corresponding chambers in the experimental area, and they are connected to DOLINA completing the eight DSP networks.

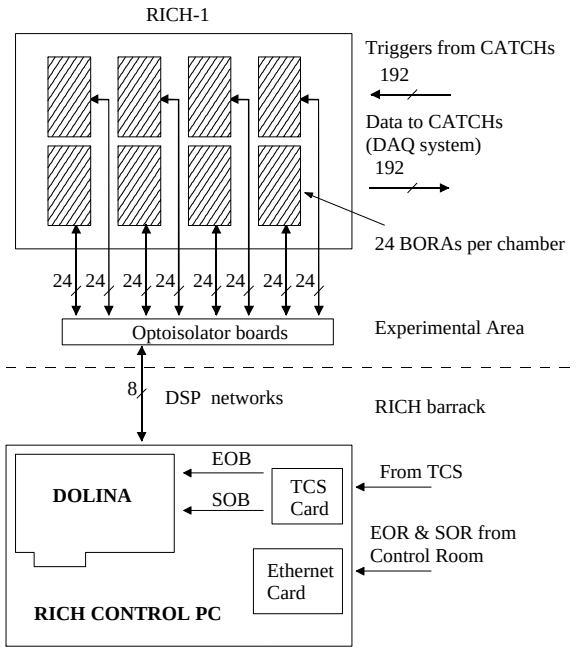

Fig. 1. General physical architecture of the RICH-1 read-out system.

DOLINA also distributes synchronization signals to the BORAs. These signals, with explicit names, are *start of run* (SOR), *end of run* (EOR), *start of burst* (SOB) and *end of burst* (EOB). Signals SOR and EOR come from the COMPASS *run control* room, and signals SOB and EOB come from the *Trigger Control System* (TCS). As soon as these signals arrive to the PC, DOLINA broadcasts them to all BORAs.

3. The BORA board

BORA is the COMPASS RICH-1 432-channel front-end board. Each BORA is connected to the pixels of the detector through a row of nine connectors. Each back-plane connector receives the signal from 48 pixels.

The DAQ in BORA is divided into two independent stages. The first stage corresponds to the sample and hold of all channels at the peaking time, followed by the analog to digital conversion and temporary storage of the digital values into on-board FIFO memories. The second stage corresponds to threshold subtraction and data transmission. The first stage is accomplished automatically after the arrival of every event trigger and takes about 1.2 μs per event; the second stage is carried out later, under the command of the DSP, and requires about 13 μs per event. The difference in processing time between the two stages is absorbed by the FIFO memory capable of buffering 128 events. The duration of the first stage determines the minimum inter-trigger delay time (dead time), while the duration of the second stage determines the maximum achievable trigger rate.

The DAQ in BORA starts automatically at the arrival of each trigger, coming through one of the two optical fibers, or internally generated by the DSP. The signals enter into 27 16-channel COMPASS-GASSIPLEX [11] front-end chips, which perform the analog amplification and filtering. The input pulse needs around 1.16 μs to reach its peak at the output (*peaking time*). As soon as the FPGA receives a trigger, it waits a programmable delay before issuing all necessary signals for the first stage of acquisition. This programmable delay is used to sample the signals at the *peaking time*. When the output analog signals reach the maximum, the GASSIPLEX chips hold the values of the signals, then the signals are converted into 10-bits numbers using 27 ADCs [12] and written into 18 16-bit FIFO memories [13].

During the second stage of the acquisition the FPGA, under the command of the DSP, reads and processes the content of the FIFO memories (three channels at the same time). The FPGA compares the readings of each channel with the corresponding programmable threshold, already stored in the FPGA memory, and only data above threshold are packed into event frames containing 32 bits per hit channel. Each event frame contains the channel values and identifications, plus a header word and a trailer word. The channel identification allows mapping a channel to a precise pixel. The FPGA transmits the event frames through the optical fiber to the global acquisition system at a data transmission rate of 400 Mbit/s [14].

Besides the regular DAQ, the BORA can be reconfigured to perform other tasks such as noise

and pedestal measurement, thresholds setting, and creation of engineering frames containing local temperatures and voltages. BORA has four temperature sensors [15] to monitor the temperature in different points of the board, and a multichannel analog to digital converter [16] to monitor several on-board power supply voltages.

BORA possesses built-in testing facilities in order to check all analog channels. By mean of a digital to analog converter, the DSP can stimulate all analog channels simulating the signals coming from the detector. This allows checking the board independently of the detectors, and this feature can also be used to measure some characteristics like peaking time and linearity.

The DSP configures the BORA to work in different modes. These working modes are called: "event", "noise and pedestal", "DSP to DAQ" and "threshold".

In "event" mode, BORA performs normal DAQ. The DSP sends an event to the RICH_Control PC, once in a while, to visualize the overall operation of the system.

In "noise and pedestal" mode, BORA performs DAQ with internal triggers generated by the DSP. After receiving an internal trigger, the FPGA saves a complete event frame (432 channels) without performing threshold subtraction. The DSP takes the values from the FPGA to calculate noise and pedestal of every channel, and sends the results to the RICH_Control PC or to the global DAQ system.

In "DSP to DAQ" mode, the DSP transmits engineering frames, threshold values, and pedestal and noise measurements directly, through the optical fiber, to the global DAQ system.

In "thresholds" mode, the DSP writes the threshold values, coming from the RICH_Control PC, into the FPGA memory before DAQ. The DSP can also read and send to the RICH_Control PC the current threshold values, if required.

4. The DOLINA board

DOLINA is a PC resident multiprocessor PCI board that allows the communication between the RICH_Control PC and all BORAs.

DOLINA contains eight on-board DSPs identical to those of the BORAS. Each DOLINA DSP handles a local time division multiplexed serial network formed by 24 BORA DSPs and itself. DOLINA communicates with all BORAs through these eight networks, where each network works independently at one Mbit/s. On the other side each DOLINA DSP communicates with the PC by writing to and reading from an on-board dual port memory (DPM) [17]. The DPM is divided into two logical regions. The reading region of the DSP is the writing region of the PC and conversely, the writing region of the DSP is the reading region of the PC. Once the DSPs have written something for the PC, the DSP writes into a DPM mail box to send an interrupt to the PC signaling there is something to read. The PC uses the same mechanism to pass data to the DOLINA DSP.

The two main functions of the DOLINA DSP are passing network packets between the PC and any of the BORA boards, and broadcasting synchronization commands (such as SOB, EOB, etc.) to all BORA boards.

Network packets have been defined for communication amongst PC, DOLINA and BORAs. These packets convey any kind of data: programs, commands, generic data, and error and acknowledge messages. The packet header contains the following information about the packet: source, destination, length, type, and packet number. DOLINA DSP analyses the header to process or pass a packet.

Synchronization commands have timing restrictions because they are used for synchronization with the global DAQ system; hence broadcasting these commands to all BORAs is mandatory. Particularly, commands SOB and EOB have severe timing restrictions; therefore, they come to DOLINA directly from the TCS board [18], and are immediately broadcasted to all BORAs.

5. Conclusions

The reconfigurable RICH-1 read-out system for the COMPASS experiment at CERN (NA58) has

been proved to steadily work up to an asynchronous trigger rate of 75 kHz with 20% maximum pixel occupancy. At these conditions, the DAQ rate is 7.77 Gbytes/s and the data transmission rate is 5.13 Gbytes/s. The maximum achieved trigger rate is enough for the current COMPASS muon program (COMPASS Run 2002). Future upgrades will push the acceptable trigger rate up to 100 kHz, which is the initially foreseen trigger rate for the COMPASS experiment.

The DSP-FPGA combination in the BORA board, with its intrinsic parallelism, largely determines the high performance of the system. The local data processing capability in BORA allows on-line threshold subtraction, as well as carrying out extensive statistical studies on all $\sim 8 \times 10^4$ channels in a reasonable time.

The required flexibility of the system, designed for adaptation to different experimental conditions or requirements has been achieved by the use of reprogrammable elements such as DSPs and FPGAs. The DSP networks allow reconfiguring and reprogramming these elements, as well as providing the communication between BORAs and the RICH_Control PC. These networks handled by DOLINA board provides the mean to manage and monitor the whole RICH-1 readout system.

The use of optical fibers and ad hoc optoisolator boards, has avoided grounding interference allowing to achieve excellent noise figures. The RICH-1 average noise level is about one ADC channel, which is close to the intrinsic ADC noise.

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